cādence[®]

Model Management with AMM User Guide

Product Version 16.6 January 2014

Document Last Updated on: May 23, 2014

© 2014 Cadence Design Systems, Inc. All rights reserved.

Portions © Apache Software Foundation, Sun Microsystems, Free Software Foundation, Inc., Regents of the University of California, Massachusetts Institute of Technology, University of Florida. Used by permission. Printed in the United States of America.

Cadence Design Systems, Inc. (Cadence), 2655 Seely Ave., San Jose, CA 95134, USA.

Allegro SI tools contain technology licensed from, and copyrighted by: Apache Software Foundation, 1901 Munsey Drive Forest Hill, MD 21050, USA © 2000-2005, Apache Software Foundation. Sun Microsystems, 4150 Network Circle, Santa Clara, CA 95054 USA © 1994-2007, Sun Microsystems, Inc. Free Software Foundation, 59 Temple Place, Suite 330, Boston, MA 02111-1307 USA © 1989, 1991, Free Software Foundation, Inc. Regents of the University of California, Sun Microsystems, Inc., Scriptics Corporation, © 2001, Regents of the University of California. Daniel Stenberg, © 1996 - 2006, Daniel Stenberg. UMFPACK © 2005, Timothy A. Davis, University of Florida, (davis@cise.ulf.edu). Ken Martin, Will Schroeder, Bill Lorensen © 1993-2002, Ken Martin, Will Schroeder, Bill Lorensen. Massachusetts Institute of Technology, 77 Massachusetts Avenue, Cambridge, Massachusetts, USA © 2003, the Board of Trustees of Massachusetts Institute of Technology. All rights reserved.

Trademarks: Trademarks and service marks of Cadence Design Systems, Inc. contained in this document are attributed to Cadence with the appropriate symbol. For queries regarding Cadence's trademarks, contact the corporate legal department at the address shown above or call 800.862.4522.

Open SystemC, Open SystemC Initiative, OSCI, SystemC, and SystemC Initiative are trademarks or registered trademarks of Open SystemC Initiative, Inc. in the United States and other countries and are used with permission.

All other trademarks are the property of their respective holders.

Restricted Permission: This publication is protected by copyright law and international treaties and contains trade secrets and proprietary information owned by Cadence. Unauthorized reproduction or distribution of this publication, or any portion of it, may result in civil and criminal penalties. Except as specified in this permission statement, this publication may not be copied, reproduced, modified, published, uploaded, posted, transmitted, or distributed in any way, without prior written permission from Cadence. Unless otherwise agreed to by Cadence in writing, this statement grants Cadence customers permission to print one (1) hard copy of this publication subject to the following conditions:

- 1. The publication may be used only in accordance with a written agreement between Cadence and its customer.
- 2. The publication may not be modified in any way.
- 3. Any authorized copy of the publication or portion thereof must include all original copyright, trademark, and other proprietary notices and this permission statement.
- 4. The information contained in this document cannot be used in the development of like products or software, whether for internal or external use, and shall not be used for the benefit of any other party, whether or not for consideration.

Disclaimer: Information in this publication is subject to change without notice and does not represent a commitment on the part of Cadence. Except as may be explicitly set forth in such agreement, Cadence does not make, and expressly disclaims, any representations or warranties as to the completeness, accuracy or usefulness of the information contained in this document. Cadence does not warrant that use of such information will not infringe any third party rights, nor does Cadence assume any liability for damages or costs of any kind that may result from use of such information.

Restricted Rights: Use, duplication, or disclosure by the Government is subject to restrictions as set forth in FAR52.227-14 and DFAR252.227-7013 et seq. or its successor.

Contents

1

Analysis Model Manager 5
<u>Overview</u>
Launching AMM
The AMM User Interface
Navigation Pane
<u>Library Tabs</u>
Spreadsheet Pane
Editor Pane
<u>AMM Toolbar</u>
AMM Menu
<u>Working with AMM</u>
Managing Libraries in AMM
Types of Libraries in AMM 15
Using Libraries
Setting Preference Options
<u>General</u>
<u>Units</u>
Vendors Plugin

<u>2</u>

Managing and Assigning Models	29
<u>Overview</u>	30
Managing Models in AMM	31
Adding Models	31
Removing Models	33
Copying Models between Libraries	34
Assigning Models using Model Assignment	39
Launching the Model Assignment Window	40

Model Management with AMM User Guide

In PowerSI, SPEED2000, and XtractIM:
Finding Models
Browsing Models
Assigning Models
Assigning by Finding
Assigning by Browsing Models in the Library

<u>3</u>

Working with IBIS and SPICE Models 49
<u>Overview</u>
IBIS Model Management
Launching IBIS Editor
The IBIS Editor User Interface 54
IBIS Editor Workflow Functions
Viewing or Editing IBIS Files
Viewing IBIS Curves
Adding Die and/or PKG Circuits
Generating IBIS Component from Layout
Running Golden Parser Check 67
SPICE Model Management
Launching SPICE Editor
Working with SPICE Editor
Create a New Sub-circuit
Edit Model Definition
Create or Delete a Local Parameter
Edit MCP Header Information
View Whole Text of the Model File
Capacitor Model Management

1

Analysis Model Manager

This chapter covers the following topics:

- Overview
- Launching AMM
- The AMM User Interface
- <u>Working with AMM</u>

Overview

The Analysis Model Manager (AMM) is aimed at providing universal and consistent analysis model management based on industry standards. AMM provides a common module and a uniform way to manage all known models for Sigrity analysis tools, such as SPEED2000, OptimizePI, PowerDC, PowerSI, and XtractIM.

AMM provides a unified library workflow in managing analysis models including creating, editing, examining, validating, and assigning analysis models. AMM supports building and managing model libraries and working with vendor libraries.

You use AMM to manage libraries of models including device, discrete, VRM, and SPICE models. Models contained in AMM libraries can be assigned to components in a design. The Model Assignment functionality has also been integrated into some of the setup wizards.

Regardless of the Sigrity tools from where it is launched, the AMM user interface is the same.

Launching AMM

AMM and its supported modules, Model Assignment, IBIS Editor, and SPICE Editor are available from various Sigrity Analysis tools.

You can launch AMM in one of the following ways:

In PowerSI, PowerDC, XtractIM, or OptimizePI:

1. Choose Tools – Analysis Model Manager.

OR

- 2. From the Model Assignment GUI:
 - □ Choose the *Assign Browse model* menu.

Or

In the Component pane, right-click and choose the *Browse model* menu from the pop-up menu.

In OptimizePI:

You can also launch AMM in OptimizePI from the Workspace menu:

→ Choose Workspace – Capacitor Library – Manager.

In Power DC:

You can also launch AMM from the Workflow pane:

→ Click Launch Analysis Model Manager under the Initial Setup section in the Workflow pane.

Load a New/Different Layout Check Stackup Set up P/G Nets Launch Analysis Model Manager Optional: Import Board Temperature Map

 \sim

The AMM User Interface

The Analysis Model Manager user interface is divided into various sections:



- Navigation pane on the left which presents a tree view of the libraries where you select a model category
- Library tabs
- Spreadsheet pane on the right displaying model data
- Editor pane at the bottom
- AMM Toolbar
- AMM menu

Navigation Pane

This pane lists the categories of models you can manage in AMM, including IC, Discrete (Capacitor, Inductor and Resistor), VRM, Connector, Package and General SPICE. You can also open or import a library file from this pane. When you select an open library under a model category, all the models in the library are displayed in the Spreadsheet pane.

Library Tabs

The Library tabs on top of the Model Data section act as a filter to make certain libraries visible. There are two library tabs:

- **Project Library** Applicable to the current project only.
 - The Project Library table lists all the available models used or which can be used in the current case.
 - □ All the libraries or folders must have the same root path, If you load a file or folder from a disk location, you cannot load another folder from a different location.
- External Library Contains all models including company library, vendor library, or any user-created library.
 - **D** The models in External Library are all available for selection.
 - **External Library may contain unlimited libraries from different locations.**



External Libraries

Project Library

For a librarian, working on a project library is a viable option. For an end user in an application, the project library is intended for local library work. The project library also automatically stores models as you assign them to components. AMM supports a single project library and multiple *External Libraries*. You can determine the structure and the number of external libraries that work best in your environment. External Libraries can be thought of as Master, Corporate, or other Project libraries. You can also control read or write access with OS level permissions on the directories.

For more information on libraries, see Managing Libraries in AMM.

Spreadsheet Pane

The Spreadsheet pane displays detailed information of a library under the selected model category. When you click a top-level model category in the navigation pane, all the models of that category across all of the loaded libraries are displayed.

]	Project Library] Discrete : (Capacitor * [E	xternal Librari	es]IC									
	Model Name	Size	Cap Model	Cnom (nF)	Compc Cost	Moun Cost	BC pe Cc	Upper Tol. (%)	Lower Tol. (%)	Area (mil^	тсс	VOL (V)	Pri
Г	0201_10nF_X5R_10%_10V	0201E	SPICE	10	0.004			10%	-10%	200	X5R	10	5
	0201_22nF_X5R_10%_6.3V	0201E	SPICE	22	0.005			10%	-10%	200	X5R	6.3	5
	0201_33nF_X5R_10%_6.3V	0201E	SPICE	33	0.006			10%	-10%	200	X5R	6.3	5
	0201_100nF_X5R_10%_6	0201E	SPICE	100	0.005			10%	-10%	200	X5R	6.3	5
	0201_220nF_X5R_20%_4V	0201E	SPICE	220	0.017			20%	-20%	200	X5R	4	5
	0402_10nF_X7R_10%_25V	0402E	SPICE	10	0.002			10%	-10%	800	X7R	25	5
	0402_22nF_X7R_10%_50V	0402E	SPICE	22	0.005			10%	-10%	800	X7R	50	5
	0402_33nF_X7R_10%_10V	0402E	SPICE	33	0.006			10%	-10%	800	X7R	10	5
	0402_47nF_X7R_10%_25V	0402E	SPICE	47	0.006			10%	-10%	800	X7R	25	5
	0402_100nF_X5R_10%_10V	0402E	SPICE	100	0.002			10%	-10%	800	X5R	10	5
	0402_220nF_X5R_10%_6	0402E	SPICE	220	0.011			10%	-10%	800	X5R	6.3	5
	0402_330nF_X5R_10%_10V	0402E	SPICE	330	0.015			10%	-10%	800	X5R	10	5

You can also select a specific library and see the models for just that library. Depending on which tab is selected, models are displayed either from the project library or external libraries.

Analysis Model Manager														
i 🖪 🔁 🕞 🛃 📘 🚃 🏦 🖿 🗡	6													
Analysis Models 🗙 🗙	[F	Project Library] Discrete : In	ductor [External Lib	raries] Di	screte	e : Cap	acitor	- CorpLi	ibraries ×				
IC *	Π	Model Name	Size	Cap Model	Cnom (nE)	Con Cost	Mou Cost	BON nen:	Upper Tol.	Lower Tol.	Area (mil^2)	TCC	VOLT 00	Pri
CorpLibraries				model	<i>,</i>			Cost	(%)	(%)	(2)		~~/	
Discrete *		T530Y687M2R5ATE006	73	SPICE	680000	1			20%	-20%	48654.6		2.5	0
Capacitor 🔿		T530Y687M2R5ATE005	73	SPICE	680000	1			20%	-20%	48654.6		2.5	0
Murata Ceramic Capacitors Spara		C_1000nF_0603_X7S	06	SPICE	1000	1			20%	-20%	1800	Х	4	5
CorpLibraries		sample_mod	78	R:20mO	5000	1			10%	-10%	694200		3	5
Inductor	Č					1			10%	-10%				5

In this pane, you can also <u>add a model</u> to the selected model library.

crete : Capacit	or 🎽 [Exte	ernal Librar	ies]			
Size	Cap Model	Cnom (nF)	Compc Cost	Mount Cost	BOM penalty Cost	Upper Tol. (%)
i Model	SPICE	680	1			20%
Delete Models		680	1			20%
			1			10%
y to Library						
rch Models						
	d Model Size ete Models by to Library rch Models	Size Cap Model Size Cap Model SPICE SPICE SPICE SPICE SPICE	Size Cap Model (nF) Model SPICE 680 SPICE 680 SPICE 680 SPICE 680	Size Cap Model (nF) Compc Cost Model SPICE 680 1 SPICE 680 1 SPICE 680 1 SPICE 680 1 rch Models	Size Cap Model (nF) Compc Mount Cost Cost Model SPICE 680 1 SPICE 680 1 SPICE 680 1 rch Models	Size Cap Model (nF) Compc Mount BOM penalty Cost Cost Cost Model SPICE 680 1 SPICE 680 1 sy to Library rch Models

Editor Pane

By default, the Editor pane consists of two panes:

• **Output pane:** This pane shows detailed information about the loaded models.

Output	×
Importing models from "Y:\ASI\Update3\SpeedXP\Library\decap library\Samsung_MLCC_Capacitors\Samsung_MLCC_Capacitors xml". 836 models imported from "Y:\ASI\Update3\SpeedXP\Library\decap library\Samsung_MLCC_Capacitors\Samsung_MLCC_Capacitors xml" [Project Library] 836 models loaded from "Y:\ASI\Update3\SpeedXP\Library\decap library\Samsung_MLCC_Capacitors\"	
Search Models Output	

- **Search Models pane:** This pane is further split into two parts:
 - Library section on the left shows the location of the library to be searched when you are searching in an external library, that is when the External Libraries tab is active.
 When you are searching in the project library, this pane is blank.

□ Search criteria section on the right is used to set the search parameters.

Search Models					×
Library		Search Field	Op.	Value	
V:\ASI\Update3\SpeedXP\Library\decap library\Samsung_MLCC_Capacitors\		Capacitor			
		Model Name	=	*	
		Lookup Keyword	=	*	Ξ
		Size	=		
		Cnom(nF)	=		
		VOLT(V)	=		
		TCC	=		_
		¹⁷			
				Search	
Search Models Output					

Note: You can select the check box for the library location to select the library in which to search for models.

The Library section does not show each location of each library. If the libraries are stored in a shared path, only the location of the parent folder is shown here.

The Editor pane opens the corresponding property pane when a model is selected in the Spreadsheet pane.

Capacitor -> Capacitor Model (CLL5Y105MR3NLN)		×
Capacitor Model Impedances		
O By RLC 20 mOhm 0.4 nH 100 nF Image: By SPICE Edit SPICE		
.PartialCkt CLL5Y105MR3NLN ExtNode = 1 0 S1 1 0 2 0 Model = CLL5Y105MR3NLN.s2p V 2 0 0 .EndPartialCkt		
	ОК	Cancel
Search Models Capacitor -> Capacitor Model (CLL5Y105MR3NLN) Output		

AMM Toolbar

The standard toolbar of the AMM UI provides the common function you can perform in the AMM user interface.



lcon	Description
Open Library	All the libraries within the designated location are loaded into AMM.
Load Library File	The designated library is imported and loaded into AMM.
Opened Library	A drop-down list shows a list of all of the libraries opened for a particular tab— Project Library or External Libraries.
Save Library	Save the currently displayed library.
View Pane Analysis Models	The Navigation pane is hidden. The Spreadsheet pane expands across the upper part of AMM
View Pane Output	Open the Output pane
Search Models	Open the Search Models pane
Add Model	Add a new model
Delete Models	Delete the selected model(s)
Copy to Library	Copy the selected model(s) to target library
Settings	Open the Settings window

The standard toolbar of the AMM UI provides the common function you can perform in the UI.

AMM Menu

Library View Window Tools ΠÊ. Library <u>T</u>ools View Open Library... Toolbar ۲ Options... Load Library File... Pane ۲ Save Exit

Menu Command	Description
Library – Open Library	Open the libraries within the designated location.
Library – Load Library	Import and load the specified library into AMM.
Library – Save	Save the currently displayed library.
View – Toolbar – Standard	Show or hide the standard AMM toolbar
View – Pane – Models/ Output/Search	Show or hide the Output or Search Models panes.
Tools – Options	Opens the <u>Options dialog</u> .

January 2014

Working with AMM

This section covers the following topics:

- Managing Libraries in AMM
- Setting Preference Options

Managing Libraries in AMM

- Types of Libraries in AMM
 - □ <u>AMMP File</u>
 - AMMX Library Flies
 - Decap XML Library Files
 - Vendor Library Files
- <u>Using Libraries</u>
 - Opening a Library
 - □ Importing a Library File
 - <u>Removing Libraries</u>
 - Using External Libraries

Types of Libraries in AMM

AMM supports libraries in various file formats, such as AMMP, AMMX, AMM, and XML.

AMMP File

When AMM launches, it looks into the user preference file (.ammp) to load an existing set of libraries (a configuration). A *preference* file is supplied to specify the loaded library list and whether to load it or not.

```
\u00ed 
\u00ed <
```

A user preferences file can be:

- **Global**, a common preference file for all designs stored at the location of installed tools
- Local, design-specific preference file stored at the same location as the design

If no specific design is open, AMM uses the global preference file to load libraries. If a specific design is open in an analysis tool, and if the design specific preference file exists, AMM uses the design-specific preference file to load the libraries, if such a file exists. If it does not exist, the global preference file is used.

AMMX Library Flies

An AMMX file is an external XML file of library data. You can import an existing .ammx file from the *Load Library File* menu command.

📀 Open AMM Import	Libs		×
AA > 4 - 2	MM_testcase Libraries CorpLibraries	👻 🍫 Search CorpLii	braries 🔎
Organize 🔻 Ne	ew folder	E	= • 🔟 🔞
🔆 Favorites	A Name	Date modified	Туре
🧮 Desktop	🌗 path	1/13/2014 11:42 PM	File folder
鷆 Downloads	CorpLibraries.ammx	1/13/2014 11:50 PM	AMMX File
🔛 Recent Places			
Caller Contents (Caller) Contents (Caller) Contents (Caller) Contents (Caller) Contents (Caller) Content (Caller) (Call			
🛤 Comnuter	▼ <		•
	File <u>n</u> ame: CorpLibraries.ammx	AMM Import Lib <u>Open</u>	s(*.ammp,*.an 💌 Cancel

Decap XML Library Files

These are the old Sigrity library format – a default and several vendor libraries supplied in the installation hierarchy. These libraries can be imported to generate an AMM library. You can load an xml file to load an existing Decap Library.

Vendor Library Files

The following five vendors and the supported file formats are:

Vendor	File Format
Murata	.MOD
Kemet	.CKT
TDK	.MOD

Vendor	File Format
Samsung	.S2P
TaiYoYuDen	.S2P

Using Libraries

In AMM, you can either open a library from a specified location or load a library file.

Opening a Library

To open a library,

- 1. Click the Open Library icon or right-click in the navigation pane and select the *Open Library* command from the pop-up menu.
- 2. In the Open Project Library dialog, select the appropriate model type.



The Model Type field sets the default model category that will be visible after the library is opened. It does not limit the type of models that can be present in the library. You can keep any type of models in a library.

- **3.** Click the ellipsis next to the Location edit box.
- 4. In the resultant Browse for Folder dialog, browse to the location of the library to be added.
- 5. Close the dialog boxes.

The models of the selected model type are populated in the spreadsheet pane of AMM. As you hover the mouse pointer over the library name in the navigation pane, note that the path appears in the tooltip.

Analysis Models		×
IC		\$
<u>CorpLibraries</u>		
Discn D:\samps	\AMM_testcase\Librari	es\CorpLibraries\
Capacitor	$\overline{\mathbf{v}}$	
Inductor	$\overline{\mathbf{e}}$	
Resistor	$\overline{\mathbf{e}}$	

6. View the Output tab for details of the models imported in AMM.

Note that the models are of the type you specified and are imported from the . xml files under the specified root folder.



- When the Project Library tab is active, a library is loaded from the location of the project library.
- When the External Library tab is active, a library is loaded from the location of the external libraries.

Importing a Library File

You can also reuse existing libraries by importing libraries in AMM. You import or load a library file when you need to import data from a specific library file. You can load a library file in AMM regardless of its location in the hierarchy.

To import a library file:

- 1. Click the Load Library File icon or right-click in the navigation pane and select the *Load Library* command from the pop-up menu.
- When the Project Library tab is active, models from the specified library file are loaded into the project library.
- When the External Library tab is active, models are loaded from the specified library file to external libraries.



2. Browse to the path containing the library file.

You can import a library file with one of the following three file extensions:

- AMMP AMM loads the library listed in preferred file location (<u>Tools Options –</u> <u>General page</u>)
- AMMX AMM imports models from the AMMX file

	Decap	XML -	– AMM	imports	models	from	decap	XML	file
--	-------	-------	-------	---------	--------	------	-------	-----	------

- Apply Siz Model Manager													
													1 X
🚺 🔁 🕞 🛃 📕 💼 👬 📑 🗡 🚳 🔜													
Analysis Models X	[Project Library] Discrete :	Capacitor × [External Librar	ries]IC									
IC	Model Name	Size	Cap Model	Cnom (nF)	Compc Cost	Moun Cost	BC pe	Upper Tol.	Lower Tol.	Area (mil^	тсс	VOL (V)	Pri 📥
Discrete *							Ċ¢	(%)	(%)	· ·		1.	
Capacitor 🔿	0201_10nF_X5R_10%_10V	0201E	SPICE	10	0.004			10%	-10%	200	X5R	10	5 =
Sigrity Default Library	0201_22nF_X5R_10%_6.3V	0201E	SPICE	22	0.005			10%	-10%	200	X5R	6.3	5
	0201_33nF_X5R_10%_6.3V	0201E	SPICE	33	0.006			10%	-10%	200	X5R	6.3	5
Inductor	0201_100nF_X5R_10%_6	0201E	SPICE	100	0.005			10%	-10%	200	X5R	6.3	5 🗆
Resistor	0201_220nF_X5R_20%_4V	0201E	SPICE	220	0.017			20%	-20%	200	X5R	4	5
VPM	0402_10nF_X7R_10%_25V	0402E	SPICE	10	0.002			10%	-10%	800	X7R	25	5
	0402_22nF_X7R_10%_50V	0402E	SPICE	22	0.005			10%	-10%	800	X7R	50	5
Connector	0402_33nF_X7R_10%_10V	0402E	SPICE	33	0.006			10%	-10%	800	X7R	10	5
Package	0402_47nF_X7R_10%_25V	0402E	SPICE	47	0.006			10%	-10%	800	X7R	25	5
ruckuge	0402_100nF_X5R_10%_10V	0402E	SPICE	100	0.002			10%	-10%	800	X5R	10	5
General SPICE	0402_220nF_X5R_10%_6	0402E	SPICE	220	0.011			10%	-10%	800	X5R	6.3	5
	0402_330nF_X5R_10%_10V	0402E	SPICE	330	0.015			10%	-10%	800	X5R	10	5 👻
	<				111								
Output													×
Importing models from 'Y:\ASI\Update3\SpeedXP\Library\decap li 28 models imported from 'Y:\ASI\Update3\SpeedXP\Library\decap [Project Library] 28 models loaded from 'Y:\ASI\Update3\SpeedXP	orary\Sigrity_Default_Library\Sigrity bibrary\Sigrity_Default_Library\Sig \Library\decap library\Sigrity_Defa	_Default_Library. ity_Default_Libra ut_Library\'	kml". ry xml"										
Search Models Output													

Models are imported from the selected library into AMM.

Removing Libraries

You can remove a library from the current project. Use one of the following methods to remove a library:

 Right-click the library in the Navigation pane and select *Remove Library* from the popup menu.

Or

→ Click the Opened Libraries icon and then in the list of libraries, click the red cross mark close to the name of the library to be removed.

The selected library is removed.

Using External Libraries

You can work with libraries that are external to the current project. An external library contains all models including company, vendor, or any user-created libraries. An external library can contain any number of libraries from various locations. You need to click the *External Libraries* tab to perform operations on external libraries.

Loading an External Library

You can open or load a library file in the same way as you open or load a project library. You can load a specific library file:

🚸 Open AMM Import Libs					×
yu 🛛 IZA » 📒 🗢 💽	odate3 🕨 SpeedXP 🕨 Library 🕨 decap libr	rary 🕨 Kernet 🕨 🗖	🔸 😽 🛛 Search Kem	et	٩
Organize 👻 New folde	r			i≡ - □	0
★ Favorites ■ Desktop ▶ Downloads > Recent Places ■ Libraries ■ Documents ▶ Music ■ Pictures ■ Videos ** Computer ▲ Local Disk (C:) ■ New Volume (D:)	Name Ceramic_Capacitors Tantalum_Aluminum_Capacitors Kemet_Ceramic Kemet_Tantalum_Aluminum	Date modified 1/9/2014 3:55 PM 1/9/2014 3:55 PM 9/21/2012 8:52 AM Oct Costs of the second Type: XML Document Size: 1.75 MB Date modified: 9/21/2012 8	Type File folder XML Document Cocument	Size 1,800 KB 2,802 KB	
⊊ soniap (\\sjsnap19a\ ⊊ v16-65-1 (\\timing6' ¶ Network File <u>n</u> a	me: Kemet_Ceramic		▼ AMM Import L	ibs(*.ammp,*.am	

IC
Discrete *
Capacitor 📀
decap library
Kemet (Kemet_Ceramic)
Murata_Netlist
Murata_Spara
Samsung_MLCC_Capacitors
Sigrity_Default_Library
TAIYO_YUDEN (TaiYoYuDen)
TUK
Inductor
Resistor
VRM
Connector
Package
General SPICE

You can also open all the external libraries at a specified location:

Searching in External Libraries

To search an external library for a model based on a specified criteria:

- **1.** Select the external library file in the navigation pane or the parent folder containing all the libraries if you want to search in multiple libraries simultaneously.
- 2. Right-click in the Spreadsheet pane and choose the *Search Models* command from the pop-up menu.

	Search Field	Op.	Value
	Capacitor		
	Model Name	=	*
	Lookup Keyword	=	*
	Size	=	
4	Cnom(nF)	<=	100 👻
	VOLT(V)	=	
	TCC	=	
*			
			Search

3. In the Search Models pane, specify the search string and click *Search*.

Search results are displayed in the Search External Libraries tab.

[Project Library] Discrete [Exte	ernal Libr	aries]Disc	rete : Cap	acitor - de	cap library	[Search	: Extern	al Librari	es] Disc	rete : Ca	pacitor ^{>}	\supset
	Model Name	Size	Cap Model	Cnom (nF)	Compi Cost	Mount Cost	BOM penalty Cost	Upper Tol. (%)	Lower Tol. (%)	Area (mil^2)	- TCC	VOLT (V)	Prefer
	CDR35BX823BKSM	18	SPICE	82	1			10%	-10%	45000		100	5
	CDR35BX683BKSM	18	SPICE	68	1			10%	-10%	45000		100	5
	CDR35BX563BKSM	18	SPICE	56	1			10%	-10%	45000		100	5
	CDR35BX104BKSM	18	SPICE	100	1			10%	-10%	45000		100	5
	CDR35BP912BKSM	18	SPICE	9.1	1			10%	-10%	45000		100	5
	CDR35BP822BKSM	18	SPICE	8.2	1			10%	-10%	45000		100	5
	CDR35BP752BKSM	18	SPICE	7.5	1			10%	-10%	45000		100	5
	CDR35BP682BKSM	18	SPICE	6.8	1			10%	-10%	45000		100	5
	CDR35BP622BKSM	18	SPICE	6.2	1			10%	-10%	45000		100	5
	CDR35BP562BKSM	18	SPICE	5.6	1			10%	-10%	45000		100	5
	CDR35BP512BKSM	18	SPICE	5.1	1			10%	-10%	45000		100	5

Setting Preference Options

You can specify a few AMM options in the Options dialog. There are three pages in the Options dialog accessible from the *Tools – Options* menu:

- General
- Units
- Vendors

General

Here you set the general options for opening models and libraries.

🏰 Analysis Model Manager - C)ptions ×
General Units Vendors Plugin	Change the 'General' options in Analysis Model Manager
	General Settings
	Use same directory path as selected library when browsing for source model files
	External Libraries
	Automatically generate preferences file for status and path of external libraries upon exit
	Preference: :::ProgramData/Cadence Design Systems, Inc.\SpeedXP Suite 13.0/PowerSI/PowerSI
	Set default path Save a copy
	Default Apply OK Cancel

General Settings: If you want to use the directory path of the selected library for browsing model files, select the corresponding option in the General Settings section.

External Libraries: To generate a preference file (.ammp) consisting of the path to the currently open external files upon exiting from the tool, select the corresponding option in the External Libraries section.

Set default path – Sets the specified path as the default path to save the . ammp file.

Save a copy – Saves a copy of the . ammp file.

By default, each application generates one . ammp (preference) file which is automatically read when the next time the application is launched. You can prevent this behavior by deselecting the option highlighted in the previous screenshot.

Units

On the Units page, you can change the default units of various parameters of models. For example, you can change the unit of capacitance from nF to F, mF, or uF.

Analysis Model Manager - Options			×
General <u>Units</u> Vendors Plugin	Change the 'Units' op	tions in Analysis Model Manager	
	Default Units		
	Unit 🛆	Default	
	Admittance	S	
	Area	mil^2	
	Capacitance	nF	
	Capacitor Size Unit	English	
	Current	A	=
	Current Density	A/m^2	
	EField	V/m	
	Frequency	MHz	
	Heat Flux	W/m^2	
	HField	A/m	
	Inductance	nH	
	Length	mm	
	Power	W	
	Power Density	W/m^3	T
		Default Apply OK Can	:el

Vendors Plugin

AMM supports capacitor models imported through vendor plugins. In this section, you define how to identify a folder as a vendor library in which the plugin will parse the vendor models. If a folder name matches the keywords under the *Keyword in Folder Name* column, the vendor plugin will parse models in the folder. For example, if there are two folders with vendor plugins, *Murata_Netlist* and *Murata_Spara*, and the keyword in the folder name is specified as **Murata**, AMM will use the plugin specified in the corresponding *Vendor Plugin* column to parse models in both the folders.

Analysis Model Manager - Option	15	X					
General Units Vendors Plugin	Change the 'Vendors P	'lugin' options in Analysis Model M					
	Options Change the 'Vendors Plugin' options in Analysis Model M Plugins to parse analysis models of vendors Keyword in Folder Name Vendor Plugin *Kemet* D:\Cadence\SPB_16.6\ASI\Update3\SpeedXP\SpeedXP\SpeedXP Suite *Murata* D:\Cadence\SPB_16.6\ASI\Update3\SpeedXP\SpeedXP\SpeedXP Suite *TAIYO_YUDEN* D:\Cadence\SPB_16.6\ASI\Update3\SpeedXP\SpeedXP Suite *TDK* D:\Cadence\SPB_16.6\ASI\Update3\SpeedXP\SpeedXP Suite amv_Kemet Ver: 1, 0, 0, 1 Kemet Dynamic Link Library Eink Library						
	Keyword in Folder Name	Vendor Plugin					
	Kemet *Murata* *Samsung* *TAIYO_YUDEN* *TDK*	D:\Cadence\SPB_16.6\ASI\Update3\SpeedXP\SpeedXP Suite D:\Cadence\SPB_16.6\ASI\Update3\SpeedXP\SpeedXP Suite D:\Cadence\SPB_16.6\ASI\Update3\SpeedXP\SpeedXP Suite D:\Cadence\SPB_16.6\ASI\Update3\SpeedXP\SpeedXP Suite D:\Cadence\SPB_16.6\ASI\Update3\SpeedXP\SpeedXP Suite					
	amv_Kemet ver: 1, 0, 0, 1 Kemet Dynamic Link Library						
	И	Default Apply OK Cancel					

Managing and Assigning Models

This chapter covers the following topics:

- Overview
- Managing Models in AMM
 - □ <u>Adding Models</u>
 - <u>Removing Models</u>
 - <u>Copying Models between Libraries</u>
- Assigning Models using Model Assignment
 - Launching the Model Assignment Window
 - □ <u>Finding Models</u>
 - Browsing Models
 - □ <u>Assigning Models</u>

Overview

Many organizations have their own tools to manage central libraries. The Analysis Model Manager provides support to manage internal and external (central) libraries. AMM also integrates a model assignment user interface that facilitates faster assignment of models.

This chapter covers the following topics:

- Managing Models in AMM
- Assigning Models using Model Assignment

Managing Models in AMM

This section covers how to manage models in AMM:

- Adding Models
- Removing Models
- <u>Copying Models between Libraries</u>

Adding Models

You can add a model to a library in AMM.

To add a model:

1. Click the Add Model icon from the toolbar

Or

1. Right-click in the Spreadsheet pane and select *Add Model* from the pop-up menu.

[F	Project Libra	ary]Discrete:	Capaci	tor × [Exte	ernal Librar	ies]			
	Model Nar	ne	Size	Cap Model	Cnom (nF)	Compc Cost	Mount Cost	BOM penalty Cost	Upper Tol. (%)
	T530Y687N	Add Mode		SPICE	680	1			20%
	T530Y687N	Delete Mor	اماد	SPICE	680	1			20%
**		Delete Wot	1015			1			10%
		Copy to Lik	orary						
F		Search Mo	dels						

A blank model item is automatically added at the end of the list.

[P	[Project Library] Discrete : Capacitor × [External Libraries]								
	Model Name	Size	Cap Model	Cnom (nF)	Compc Cost	Mount Cost	BOM pena Cost		
	T530Y687M2R5ATE006	73	SPICE	680	1				
	T530Y687M2R5ATE005	73	SPICE	680	1				
20					1				

The Model Editing view opens at the bottom of AMM. The view changes based on the model type you select in the navigation pane on the left.

IC -> DC Mod	LL (COORDER AND 1043										
	iel (2001/JewiMod01)										×
DC Model	hermal Model										
By Power I	Rail 🔘 By SPICE Model										
Net Name	Nominal Volt.(V)	Upper Tol.(%)	Lower Tol.(%)	Current Type	Current(A)		PWI Pin	Current(A)	5	GNI Pin	Current(A)
20									*	n	
									C	ж	Cancel
Search Mode	Is IC -> DC Model (S001M	lewMod01) Output					_				
Capacitor ->	Capacitor Model (sample	_mod)									×
Capacitor I	Impedances										
By RLC	20 mOhm 0.4	nH 100	nF OB	y SPICE Edit SPI	CE						
	[·							
										OK	Cancel
Search Mod	ale Canacitor - N Canacite	w Model (cample, m	ad) Output							UK	
Scarchimou	capacitor -> capacito	n model (sumple_m	output								
VRM -> VRM	Model (acme2)										×
• By Power	Rail 🔘 By SPICE Model										
Net Name	Nominal Vol.(V)	Output Tol.(%)	Output Current(A) Pin Res	istance(mOhm)		Pin Name	△ Net Nan	ne	Resistar	ice(mOhm)
<u>۳</u>						ž	0				
						ě.					
		20 0 0 0 0 0						[(ЭК	Cancel
Search Mod	els VRM -> VRM Model (a	icme2) Output						[(ЭК	Cancel
Search Mode	els VRM -> VRM Model (3 -> SPICE Model (55)	icme2) Output						((ЭК	Cancel
Search Mod General SPICE SPICE File:	els VRM -> VRM Model (a -> SPICE Model (ss) 9:\kits\DDR4_TC6_kit_1\Hard	icme2) Output	t_bench\TC4_([Model: TC4_CFG	2_R1_2013 V			[(OK	Cancel
Search Mod General SPICE SPICE File: [] .SUBCKT	 > VRM -> VRM Model (s) -> SPICE Model (ss) :\kits\DDR4_TC6_kit_1\Hard TC4_CF62_R1_201304 	icme2) Output	t_bench\TC4_)	Model: TC4_CFG	2_R1_2013 V			((эк	Cancel
Search Mode General SPICE SPICE File: [] .SUBCKT + +	els VRM -> VRM Model (; -> SPICE Model (ss));{kts\DDR4_TC6_kit_1\Hard TC4_CFG2_R1_201304 U2_W18 U2_A2 U2_A2_	icme2) Output	t_bench\TC4_)	Model: TC4_CFG	2_R1_2013 V				(OK	Cancel
Search Mod General SPICE SPICE File: [] .SUBCKT + + + +	els VRM -> VRM Model (s -> SPICE Model (ss) v:\kts\DDR4_TC6_kt_1\Har TC4_CFG2_R1_201304 U2_W18 U2_A2 U2_W17 U2_A816	icme2) Output	t_bench\TC4_(Model: TC4_CFG	2_R1_2013 V				(ЭК	Cancel
Search Mod General SPICE SPICE File: [.SUBCKT + + + +	els VRM -> VRM Model (s -> SPICE Model (ss) >:\kits\DDR4_TC6_kit_1\Hara TC4_CFG2_R1_201304 U2_W18 U2_A2 U2_W17 U2_AB16	ucme2) Output	t_bench\TC4_()	Model: TC4_CFG	2_R1_2013 V				(OK	Cancel
Search Mod General SPICE SPICE File: [.SUBCKT + + + + +	els VRM -> VRM Model (3 -> SPICE Model (ss) 2:\kits\DDR4_TC6_kit_1\Hard TC4_CFG2_R1_201304 U2_W18 U2_A2 U2_W17 U2_AB16	icme2) Output ware_correlation_tes 29_x1_BB5_Foster	t_bench\TC4_(Model: TC4_CFG	2_R1_2013 V				0	ок Г	Cancel

For example, you can switch to the Thermal Model pane by either using the *Thermal Model* tab in the Model Editing section or by selecting the Thermal Model cell back in

the Model Data section in the Spreadsheet pane. You can then specify a value for Power in the Thermal Model fields and save the model.

IC -> Thermal Model	(cpu-124)			×
DC Model Thermal M	lodel			
Power Dissipation:	40] w		
Thickness:	0	mm		
Theta-JB:	0	c/w		
Theta-JC:	0	c/w		
MaxDieTemperature:	0	c		
		-		
			OK	Cancel
Saawah Madala IC	Thorney Model	(anu 124) Output		
Search Wodels IC ->	Thermal Model	(cpu-124) Output		

2. Specify the required parameters to complete the creation of the new model.

The new model is added to the list.

[Project Library] Discrete : Capacitor × [External Libraries]									
	Model Name	Size	Cap Mode	Cnom (nF)	Comp Cost	Mount Cost	BOM penalt Cost	Upper Tol. (%)	Lower Tol. (%)	Area (mil^
	T530Y687M2R5ATE006	7343M	SPICE	680	1			20%	-20%	486
	T530Y687M2R5ATE005	7343M	SPICE	680	1			20%	-20%	486
	S001NEWMOD01	4231M	R:20	6800	1			10%	-10%	201
*)				1			10%	-10%	

Removing Models

You can also remove existing models from a library.

To remove a model:

1. Select the desired model(s) and click the Delete Models icon from the toolbar,

Or

1. Right-click and select *Delete Models* from the pop-up menu.

]	[P	roject Lib	rary] Discrete :	Capaci	tor × [Exte	rnal Libra	ries]		
		Model Name					Cap Mode	Cnom (nF)	Comp Cost	Moun Cost
		T530Y687	M2I	R5ATE006	73431	м	SPICE	680	1	
		T530Y687	M2I	R5ATE005	7343M		SPICE	680	1	
		S001NEW	<u> </u>	D01	40011	М	R:20	6800	1	
	20			Add Model					1	
				Delete Mode	ls					
				Copy to Libra	ary					
				Search Mode	ls					

2. Click Yes to confirm deletion.

Analysis Model Manager
Delete selected models?
Yes No

The selected model is removed from the library.

Copying Models between Libraries

You can copy models between libraries. For example, you can copy a model from an external library to the project library.

To copy a model between libraries:

1. Select the desired model(s) and click the Copy to Library icon from the toolbar.

Or

1. Right-click and select *Copy to Library* from the pop-up menu.

]	[F	Project Libra	ry][Discrete : Capa	citor [E:	xternal Li	braries]	Discrete	: Capaci	itor - Cor	pLibrarie	s ×
	Model Name Size				Cap Mod∠	Cnom (nF)	Compc Cost	Mount Cost	BOM penalty Cost	Upper Tol. (%)	Lowe Tol. (%)	
		sample_n	•	0 dd Model		R:20	5000	1			10%	-10%
		T530Y687		Dalata Mada	ما	SPICE	680	1			20%	-20%
		T530Y687		Delete Moue	:15	SPICE	680	1			20%	-20%
		C_1000nF		Copy to Libr	ary	SPICE	1000	1			20%	-20%
	20			Search Mode	els			1			10%	-10%

The Copy to Library dialog opens.

Copy to Library	×
 Library 	Project Library
O Library Location:	
Model Name	
No Change	
O Create Model Nar	ne
Conflict Resolution	
• Keep existed mod	del OReplace with new model
	OK Cancel

2. To copy the selected model to the current project library, proceed with the default selection, *Library - Project Library*.

If you want to copy to a specific library, browse the location of the library to which you want to copy the selected model.

Browse For Folder	×
Library path	
🛛 🍌 samps	*
🛛 🌗 AMM_testcase	
🔺 🍌 Libraries	
CorpLibraries	
🍑 path	
DecapLibrary	
🥼 PowerSI	
Dircuit	
🐌 images	
🖻 🍌 signoise.run	=
🖻 🍌 sipbatut	
Þ 🍌 ssla	
🖻 🍌 Working	
▷ 🚑 CD Drive (E:)	-
Eolder: D:\samps\AMM_testcase\Libraries\CorpLibraries	
Make New Folder OK Car	ncel

3. To proceed with the same model name, proceed with the default option, *No Change*.
If you want to rename the copied model, select the Create Model Name option. You can add or delete the parameters you want to include or exclude from the model name.

Copy to Library	X					
OLibrary	Project Library					
Library Location:	D:\samps\AMM_testcase\Libraries\CorpLit					
Model Name						
O No Change						
Create Model Nan	ne					
C_[CNOM]_[SIZE]_[TCC]					
Column						
Cnom						
TCC						
쐰						
Conflict Resolution						
• Keep existed mod	el OReplace with new model					
	OK Cancel					

4. Select the *Keep existing model* option so that the existing model in the library is retained when there is a conflict, that is when a model of the same name already exists in the library.

If you want the selected model to replace an existing model in the library with the new model when there is conflict, select the *Replace with new model* option.

5. Click *OK* to complete the operation.

[Project Library] Discrete : Capacitor * [External Libraries] Discrete : Capacitor - CorpLibraries											
	Model Name	Siz	ze	Cap Model	Cnom (nF)	Compc Cost	Mount Cost	BOM penalty Cost	Upper Tol. (%)	(
	T530Y687M2R5ATE006	73	3	SPICE	680	1			20%	Ŀ	
	T530Y687M2R5ATE005	73	3	SPICE	680	1			20%	•	
	C_1000nF_0603_X7S	06	5	SPICE	1000	1			20%	•	
	sample_mod	78	3	R:20	5000	1			10%	-	
*						1			10%		

The selected model is copied to the project library.

Assigning Models using Model Assignment

Model assignment is a key function of Analysis Model Manager. The Model Assignment and AMM functionality are integrated. As you use AMM to manage model libraries, use the Model Assignment dialog to assign models to components.

You can configure External Libraries as required and control read / write capabilities with OS permissions. Model assignment requests search all available libraries. When a model is found and assigned, it is automatically copied to the Project Library. If no Project Library is defined, a placeholder library is retained which can then be saved or discarded.

You can also edit a library and pass those updates to another library.

This section covers:

- Launching the Model Assignment Window
- Finding Models
- Browsing Models
- Assigning Models

Launching the Model Assignment Window

You can launch the Model Assignment window from the Circuit/Linkage Manager in most of the tools, such as PowerSI, SPEED2000, and XtractIM.

In PowerSI, SPEED2000, and XtractIM:

- → Choose Tools Model Assignment.
 - Or
- → Choose Setup Circuit/Linkage Manager and click the Assign button.

Circuit/Linkage Manager 🛛 🗙									
			- 9						
< A	Ckt Name \square	Model Name	Tags						
 ✓ ☑ 	cap1	🥔 Decap							
🗸 🖂	cap2	Decap							
🗸 🗚	cap3	Decap							
🗸 🖪	cap4	Decap							
🗸 🖪	cap5	Decap							
 ✓ ▲ 	cap6	Decap							
🗸 🖪	Redge	🧼 Edge Term							
	111								
	New Del Edit	Load Assign F	ilter 🍸						

Analysis Model Manager - Model	Assignment								
Assign View Help		cādence							
i A 🕒 🚮									
Component	Model Type	Assigned Models							
🗄 Decap									

The Analysis Model Manager - Model Assigned window appears.



You can also launch the window from the *Assign Capacitor Models* command which is accessible from the Workflow pane and also from the right-click pop-up menu in Circuit/Linkage Manager.

Note: In PowerDC, you can launch the window from the Component wizard and from the *Assign* button in the Editor pane.

Finding Models

You can choose find models for assignment either automatically or manually from the Model Assignment user interface. To automatically find models based on a pre-defined criteria, you use the *Final Model* functionality.

You can use one of the following ways to run the *Find model* functionality:

- Choose the Assign Find Models menu command.
- Right-click and select the *Find Models* command from the pop-up menu.

■ Click the *Find Models* button.

Browsing Models

Use the following ways to manually browse models in libraries loaded in AMM:

- Choose the Assign Browse Models menu command.
- Right-click and select the *Browse Models* command from the pop-up menu.
- Click the *Browse Models* button.

Assigning Models

When assigning models, you can select models from the project library or an external library loaded in AMM. Models assigned from external libraries are automatically copied to the project library.

Models can be assigned at the device or instance level. You must assign a device model to each component that you simulate because device models are used during simulation to create circuit simulation models for the nets in your design.

To assign a model from the Model Assignment GUI, you first need to locate the model either using the find model or browse model functionality.

Assigning by Finding

The final model functionality is an automatic model lookup mechanism. The models are matched in the configured libraries by the Lookup Keyword, Model Name, or Manufacturing Part No fields.

To automatically find and assign a model, do the following:

- **1.** In the Model Assignment window, select a component or an instance.
- 2. Specify the Model Type.

This field is required for automatically finding the matching model for a component.

3. Click the *Find Model* button.

The Analysis Model Manager – Find Model window appears with the search results. The title bar of the dialog displays the matching criteria used to find the results:

- Lookup Keyword
- Model Name
- Manufacturer Part Number

You define the *Lookup Keyword* field when you add a model to a library. You can use model names that match device file names, part numbers, or any other field. It is an optional mechanism to Index the library and to automatically match models with components.

Analysis Model Manager - Find Model (Based on Lookup Keyw	ord, Model Name or Manufacturer PartNo.) 🛛 🗆 🗙
Find Based on Lookup Keyword, Model Name or Manufacturer PartNo. Based on Model Name Naming Schema	Decap (matched results: 2) decap_123 decap_0012
	OK Cancel

The *Find Model* window contains two panes:

- □ The left pane lists the rules available to select for finding models
- **D** The right pane shows the search results

Note: When the model type is *Capacitor*, the Find Model window provides an additional search mechanism to find models based on the naming schema of model names. The options to search are displayed on the left pane and the search results on the right pane. For any other model type, only the search results pane is displayed.

Table 2-1 Find Model

Option	Description			
Based on Lookup	You can choose the rule to be used to find models.			
Keyword, Model Name or Manufacture PartNo.	If this rule is selected, a wildcard match is applied to search models from the AMM library.			
	For example, if the name of the component is ABC123, the following model names containing the string, ABC123, will be listed in the right pane of the window:			
	■ INTEL-ABC123-AAA			
	■ ABC-U980-123890			
	■ IED980ABC123			
Based on Model Naming Schema	If this rule is selected, the models which satisfy the specified naming schema are located.			
	For example, if the name of the component is CAP_0402_4uf_1.5v and the naming schema is CAP_[SIZE]_[CNOM]_[VOLT], all the models satisfying the following criteria are listed in the right pane of the window:			
	■ SIZE = 0402			
	■ Cnom = 4uf			
	■ Voltage = 1.5v			
4. Click the Based on M	odel Naming Schema option.			

- 5. Click Search.
- 6. Select the desired model from the list in the right pane and click OK.

The model is assigned:

Analysis Model Manager - Model Assignment							
<u>A</u> ssign <u>V</u> iew <u>H</u> elp			cādence				
A 🕒 🖬							
Component	Model Type	Assigned Models					
😑 Decap	Capacitor	decap_123@"CorpLibraries";					
cap1	Capacitor	GRM0222C0J101JD05@"0402_01005";					
cap2	Capacitor	GRM0222C0J101GD05@"0402_01005";					
cap3							
cap4							
cap5							
сарб	Capacitor	GRM3192C1H562JA01@"3216_1206";					
😑 EdgeTerm							
Redge	VRM	acme-V-1200@"CorpLibraries";					
		F					
Find Model Browse N	1odel		OK Cancel				

When a model is assigned to a component or an instance, the Assigned Models column displays a string which comprises the model name and the name of the library in which the model resides. As you click the name of an assigned model, a table pops-up displaying the model name, the library name, and the path to the library.

ľ	Assigne	1				
h	MyVRN	1@"Corp_Master	_Lib";	Ē		
	Mod	elName.	Library	Location		
	MyV	RM	Corp_Master_Lib	D:\samps\AE_trg\ASI_16.63	1_A№	1M_AE_Tr
ł						
ł						
t						

Assigning by Browsing Models in the Library

You can also assign models to components manually by browsing the libraries loaded in AMM. You can select the models from either the project library or the external library. If the model is selected from the external library, the model is copied to the project library automatically after assignment.

- 1. Select a component in the Model Assignment window.
- 2. Click the *Browse* button.
- **3.** In the AMM window, select the desired model.

* •		
Library View Tools Window	(ādence
🖥 🔁 🕞 🐱 📕 🚺 📾 👫 📑 🗙 🍯		
Analysis Models 🛛 🗙	[Project Library] [External Libraries] Discrete : Capacitor ×	
IC *	Model Name Ca C C M B' U Lc A T' V Pi C Pi I	M M La
CorpLibraries		N KI
Discrete *	LLR185C70G105ME07 se S. 1. 1 2 1. X. 4 5	L. M
Capacitor	LLR185C70G105ME05_se S 1. 1 2 1. X. 4 5	L. M
Murata Ceramic Capacitors Spara	LLR185C70G105ME03_se S., 1, 1 2, -, 1, X, 4 5 1	L. M
CorpLibraries	LLR185C70G105ME01_se S. 1. 1 2 1. X. 4 5	L. M
Inductor 🕑	LLL31MR71H104MA01_s S. 1. 1 2 7. X. 5. 5	
Resistor 🔍	Capacitor -> Capacitor Model (LLR185C70G105ME03_series)	×
VPM	Capacitor Model Impedances	
VKW V		
Connector		Edit SPICE.
Package	.PartialCkt: LLR185C70G105ME03_series ExtNode= 1 2 51 1 2 3 2 Model=LLR185C70G105ME03_series.s2p	
General SPICE	V 3 2 0 EndDartialCkt	
	, churai daich.	
		Cancel
		Cancer
[Discrete : Capacitor] Models: 1. @"D:\Cadence\SP library\Murata_Spara\Murata_Ceramic_Capacitors	B_16.6\ASI\Update3\SpeedXP\Library\decap OK	Cancel

The detailed information of the selected model is displayed in the Editor pane. At this point, you can even create a new model and assign it to the selected component or instance in the Model Assignment window.

4. Click *OK*.

The selected model is assigned to the component selected in the Model Assignment window. The assigned model and its parent library are saved as a reference.

	Analysis Model Manager - Model Assignment										
Ass	<u>A</u> ssign ⊻iew Cādence										
i da											
Com	nponent	Model Type	Assigned Models	-							
Ð	NCAP_402-1UF,10%,6.3V_1UF										
٠	NCAP_402-1UF,10%,10V,402										
Ð	CAP-P_3528-10,10%,20V,35			Ξ							
	CAP_X2Y-47NF_47NF										
	C58	Capacitor	LLR185C70G105ME07_series@"Murata_Ceramic_Capacitors_Spara";								
	C59	Capacitor	LLL31MR71E224MA01_series@"Murata_Ceramic_Capacitors_Spara";								
	C60										
	C61										
Ð	CAP-P_2626-100,20%,6.3V,2										
٠	CAP-P_7343-470,20%,6.3V,7										
ŧ	CAP_X2Y-220NF_220NF										
Ð	CAP_X2Y-180NF_180NF			+							

Working with IBIS and SPICE Models

This chapter covers the following topics:

- Overview
- IBIS Model Management
- SPICE Model Management
- Capacitor Model Management

Overview

Analysis Model Management provides a common module and a uniform way to facilitate the management of IBIS, SPICE, and Discrete models.

This chapter covers the following topics:

- IBIS Model Management
 - Launching IBIS Editor
 - <u>The IBIS Editor User Interface</u>
 - IBIS Editor Workflow Functions
- <u>SPICE Model Management</u>
 - □ Launching SPICE Editor
 - Working with SPICE Editor
- <u>Capacitor Model Management</u>

IBIS Model Management

IBIS Editor facilitates management of and IBIS model files. IBIS Editor is an editing tool that helps you ensure the integrity of the model data circuit simulations. It provides you an easy-to-use editing environment to create, manipulate, and validate models quickly.

Launching IBIS Editor

You can launch IBIS Editor using one of the following methods:

- From the Tools Menu in SPEED2000
- From the Property dialog of SystemSI

From the Tools Menu in SPEED2000

1. Choose the *Tools – IBIS Editor* menu command.



2. Select the IBIS file to open and click *Open*.



From the Property dialog of SystemSI

1. In a SystemSI design double-click a controller or memory block.

2. Click Load IBIS.



ck Name: Contr	oler1				Controller OnDie Parasitics Package Parasitics Ignore VT Curv
Conn. Port	Connect To	Block Name	Conn. Port		File Name: Controller 1_ddr3.sp Sub-circuit Name: Controller 1_TSMC28HPM
to_PCB		Package	DIE	Edit Layout Linkage	IBIS File: D:/work/DDR3/DDR3_Design-In-Kit_v60/DDR3kit/Post_rov Component: TSMC28HPM
					.subckt Controller I_TSMC28HPM +1 2 3 4 5 6 7 8 9 10 11 12
					*[MCP Begin] *[MCP Veril 1:2
					[MCP Source] Cadence Design Systems, Inc. MCP Editor
					*[RBM]**(Connection] to .PCB
					*[Connection Type] *[Power Nets]
					"11 11 power "[Ground Nets]
					"I2 I2 gnd "(Signal Nets) "I 000
					*2 2 DQ1 *3 3 DD2
					Load IBIS
ne dine	_				Load IBIS

3. In the Load IBIS dialog, click *Edit IBIS*.

Lo	ad IBIS								X
[D:\work\Kits\DDR3	DDR3_Design-In	-Kit_v60\DDR3kit\Po	st_route_testbench\do	dr3.ibs		Comp	onent : TSMC28HPM	Edit IBIS
Pin Mapping Bus Definition								Explicit IO Power and Ground Terminals	
[Pin	Pulldown	Pullup	GND Clamp	Power Clamp	Signal Name	Model Name	Bus Group	
	1	ground 1	power1	ground 1	power 1	DQ0	34	data	
	10	ground 1	power1	ground 1	power1	DQSN	34	Timing Ref	
	11		power1			power	Power		
	12	ground 1				gnd	Gnd		
	2	ground 1	power1	ground 1	power 1	DQ1	34	data	
	3	ground 1	power1	ground 1	power 1	DQ2	34	data	
	4	ground 1	power1	ground 1	power 1	DQ3	34	data	
	5	ground 1	power1	ground 1	power 1	DQ4	34	data	
	6	ground 1	power1	ground 1	power 1	DQ5	34	data	
	7	ground 1	power1	ground 1	power 1	DQ6	34	data	
	8	ground 1	power1	ground 1	power 1	DQ7	34	data	
	9	ground1	power1	ground 1	power1	DQSP	34	Timing Ref	
[Filter								OK Cancel

The AMM IBIS Editor launches.



The IBIS Editor User Interface

The IBIS Editor is divided into three panes:

- The Workflow pane
- The IBIS file pane
- The Output pane

When an IBIS file is loaded, the text editing frame on the right displays the structure and the content of the IBIS file. The left side of the IBIS file pane is a section tree and each tree node is a keyword in the IBIS File. The right side of this pane is the text area.

In the text area, you can edit the content of the IBIS file. The syntax of the text typed in the text area is automatically checked. As you click a keyword in section tree, the cursor jumps to the location of the corresponding line in the text area.

IBIS Editor Workflow Functions

The IBIS Editor workflow provides functions, which help you manage IBIS models. You can view an IBIS file and IBIS curves, add and view die or package circuits.

Viewing or Editing IBIS Files

This option displays the contents of the IBIS file in the IBIS file pane, where you can view and edit the IBIS models.

Viewing IBIS Curves

This option displays the curve and waveform view of the IBIS models. The information displayed in spread across three panes:.

- To the left is the curve organization tree, where the first level is the model name, the second level is the curve type (I-V curves, Waveforms), and the third level is the curve.
- The upper right part displays the I-V curve.
- The lower right part displays the Waveform curve. You can resize the area to display the curve or the waveform. You can also double-click to have a waveform or curve cover the entire display area on the right.

 Combined I-V curves are generated automatically, and are displayed in the I-V curve view.



Adding Die and/or PKG Circuits

- Adding Die PKG Circuits
- Adding PKG Circuit
- Adding Die and Package Circuits

Adding Die PKG Circuits

To add a die circuit,

1. Select Add Die and/or PKG Circuits in the IBIS Editor workflow.

Select Mode		and manda		Dia nada			
Add Die Circuit	Origin	al IBIS File	Port 1	Pin node			
C Add FKG Circuic	ĬŎ	buffer					
O Add Die & PKG Cir	rcuits m		S On-die circ	cuit model			
rcuit File:	camps)Sample, DIMM cl	4- C		TRIS Model Eiler	Dulsamps) generic?	Pibe	
Cold Files	amps(pample_primm.c)			TRI2 Model Hile;	D:(samps(genericz	LIDS	
CP SUBCKT: Sam	ple_DIMM	-		IBIS Component:	Generic	-	
CP SUBCKT: Sam	ple_DIMM	 ▼ ▼ 		IBIS Component:	Generic	•	
CP SUBCKT: Sam onnection Port: J1 ayout PinName / letName	ple_DIMM IBIS PinName / SignalName	▼ ▼ Model Name	Pulldown	IBIS Component:	Generic	Power Clamp	,
CP SUBCKT: Sam onnection Port: J1 ayout PinName / letName umped(B9) / VCC	IBIS PinName / SignalName	Model Name	Pulldown	IBIS Component:	Generic GND Clamp NC	Power Clamp	_
CP SUBCKT: Sam sonnection Port: J1 ayout PinName / letName umped(B9) / VCC umped(B9) / VCC	IBIS PinName / SignalName p1 / VCC p1 / VCC	Model Name POWER POWER	Pulldown NC NC	IBIS Component: Pullup pwr1 pwr1	Generic GND Clamp NC NC	Power Clamp NC NC	
CP SUBCKT: Sam innection Port: J1 ayout PinName / letName umped(B9) / VCC umped(B9) / VCC umped(B2) / GROUND	IBIS PinName / SignalName p1 / VCC p1 / VCC g1 / GROUND	Model Name POWER POWER GND	Pulldown NC NC gnd1	IBIS Component: Pullup pwr1 pwr1 NC	Generic GND Clamp NC NC NC	Power Clamp NC NC NC	
CP SUBCKT: Sam innection Port: J1 ayout PinName / letName umped(B9) / VCC umped(B9) / VCC umped(B2) / GROUND umped(B2) / GROUND	IBIS PinName / SignalName p1 / VCC p1 / VCC g1 / GROUND g1 / GROUND	Model Name POWER POWER GND GND	Pulldown NC gnd1 gnd1	IBIS Component: Pullup pwr1 pwr1 NC NC	Generic GND Clamp NC NC NC NC NC	Power Clamp NC NC NC NC	
CP SUBCKT: Sam innection Port: J1 ayout PinName / letName umped(B9) / VCC umped(B9) / VCC umped(B2) / GROUND umped(B2) / GROUND 7 / DQ50#	IBIS PinName / SignalName p1 / VCC p1 / VCC g1 / GROUND g1 / GROUND s1 / DQ50#	Model Name POWER GND GND 120ohm_ODT_2133	Pulldown NC gnd1 gnd1 gnd1	IBIS Component: Pullup pwr1 pwr1 NC NC pwr1	Generic GND Clamp NC NC NC NC NC SNC Qnd1	Power Clamp NC NC NC NC NC pwr1	
CP SUBCKT: Sam annection Port: J1 ayout PinName / letName umped(B9) / VCC umped(B9) / VCC umped(B2) / GROUND umped(B2) / GROUND 7 / DQ50# 3 / DQ00	IBIS PinName / SignalName p1 / VCC p1 / VCC g1 / GROUND g1 / GROUND s1 / DQ50#	Model Name POWER POWER GND GND 120ohm_ODT_2133	Pulldown NC gnd1 gnd1 gnd1	IBIS Component: Pullup pwr1 pwr1 NC NC pwr1	Generic GND Clamp NC NC NC NC NC gnd1	Power Clamp NC NC NC NC NC pwr1	
CP SUBCKT: Sam ponnection Port: J1 ayout PinName / letName umped(B9) / VCC umped(B9) / VCC umped(B2) / GROUND umped(B2) / GROUND 7 / DQ50# 3 / DQ00 7 / DQ50	IBIS PinName / SignalName p1 / VCC p1 / VCC g1 / GROUND g1 / GROUND s1 / DQ50#	Model Name POWER POWER GND GND 120ohm_ODT_2133	Pulldown NC gnd1 gnd1 gnd1	IBIS Component: Pullup pwr1 pwr1 NC NC pwr1	Generic GND Clamp NC NC NC NC NC gnd1	Power Clamp NC NC NC NC pwr1	
CP SUBCKT: Sam ponnection Port: J1 ayout PinName / letName umped(B9) / VCC umped(B9) / GROUND umped(B2) / GROUND if / DQ50# 3 / DQ00 7 / DQ50 2 / DQ02	IBIS PinName / SignalName p1 / VCC p1 / VCC g1 / GROUND g1 / GROUND s1 / DQ50#	Model Name POWER GND GND 120ohm_ODT_2133	Pulldown NC gnd1 gnd1 gnd1	IBIS Component: Pullup pwr1 pwr1 NC NC pwr1	Generic GND Clamp NC NC NC NC gnd1	Power Clamp NC NC NC NC pwr1	
CP SUBCKT: Sam connection Port: J1 ayout PinName / letName umped(B9) / VCC umped(B9) / VCC umped(B2) / GROUND mped(B2) / GROUND 7 / DQ50# 3 / DQ00 7 / DQ50 2 / DQ02 7 / DQ01	IBIS PinName / SignalName p1 / VCC p1 / VCC g1 / GROUND g1 / GROUND s1 / DQ50#	Model Name POWER GND GND 120ohm_ODT_2133	Pulldown NC gnd1 gnd1 gnd1	IBIS Component: Pullup pwr1 pwr1 NC NC pwr1	Generic GND Clamp NC NC NC NC gnd1	Power Clamp NC NC NC NC pwr1	
CP SUBCKT: Sam onnection Port: J1 ayout PinName / letName umped(B9) / VCC umped(B9) / VCC umped(B2) / GROUND umped(B2) / GROUND i7 / DQ50# 3 / DQ00 7 / DQ50 2 / DQ02 7 / DQ01 8 / DQ03	IBIS PinName / SignalName p1 / VCC p1 / VCC g1 / GROUND g1 / GROUND s1 / DQ50#	Model Name POWER GND GND 120ohm_ODT_2133	Pulldown NC gnd1 gnd1 gnd1	IBIS Component: Pullup pwr1 pwr1 NC NC pwr1	Generic GND Clamp NC NC NC SNC gnd1	Power Clamp NC NC NC NC pwr1	
CP SUBCKT: Sam onnection Port: J1 ayout PinName / letName umped(B9) / VCC umped(B9) / VCC umped(B2) / GROUND umped(B2) / GROUND v7 / DQ50# 3 / DQ00 7 / DQ50 2 / DQ02 7 / DQ01 8 / DQ03 2 / DQ06	IBIS PinName / SignalName p1 / VCC p1 / VCC g1 / GROUND g1 / GROUND s1 / DQ50#	Model Name POWER GND GND 120ohm_ODT_2133	Pulldown NC gnd1 gnd1 gnd1	IBIS Component: Pullup pwr1 pwr1 NC NC pwr1	Generic GND Clamp NC NC NC gnd1	Power Clamp NC NC NC NC pwr1	
CP SUBCKT: Sam pannection Port: J1 ayout PinName / letName umped(B9) / VCC umped(B2) / GROUND umped(B2) / GROUND i7 / DQS0# 3 / DQ00 i2 / DQ02 i2 / DQ02 i2 / DQ01 i8 / DQ03 i2 / DQ06 i3 / DQ04	IBIS PinName / SignalName p1 / VCC p1 / VCC g1 / GROUND g1 / GROUND s1 / DQ50#	Model Name POWER GND GND 120ohm_ODT_2133	Pulldown NC gnd1 gnd1 gnd1	IBIS Component:	Generic GND Clamp NC NC NC gnd1	Power Clamp NC NC NC NC pwr1	
CP SUBCKT: Sam printection Port: 31 ayout PinName / letName umped(B9) / VCC umped(B2) / GROUND mped(B2) / GROUND 7 / DQS0# 3 / DQ00 7 / DQS0 2 / DQ02 7 / DQ01 8 / DQ03 2 / DQ04 	IBIS PinName / SignalName p1 / VCC p1 / VCC g1 / GROUND g1 / GROUND s1 / DQ50#	Model Name POWER GND GND 120ohm_ODT_2133	Pulldown NC gnd1 gnd1 gnd1	IBIS Component: Pullup pwr1 pwr1 NC NC pwr1	Generic GND Clamp NC NC NC gnd1	Power Clamp NC NC NC NC pwr1	

You need to load an XPI PDN circuit file and assign signal models for signal pins.

Field	Description
Auto Pin Mapping	Completes pin mappings according to the information in the MCP header of XPI PDN circuit file.
Clear All	Clears all the model and pin mapping information.
Recover	Discards the modification and reloads the current IBIS file.

2. Specify the circuit file name.

ı

3. Click Next.

You can proceed if there is a good connection, that is there is at least one power, one ground pin, and one signal pin.

4. Click the Edit icon in the Model Name cell for a pin/net.

A list of available model appears.

5. Select a model and click OK.

Select Mode						
Add Die Circu Add PKG Circu	uit	Pad Original I	BIS File		about 2 about 2	
Add Die & PK	(G Circuits	IO bi moc	uffer Iels	On-die circuit mod		
		Pin Name	Signal Name	Model Name	^	
				DM_ODT48_2400		
				DM_ODT60_2133		
				DM_ODT60_2400		
cuit File:	D:\samp			DM_ODT80_2133	bs	
	Comela 1			DM_ODT80_2400		
P DODCK1.				DQ5_34_2133	=	
nnection Port:	J1			DQS_34_2400		
wout PipName /	IBI			DQ5_40_2133		Power Clamp
etName	Sig			DQ5_40_2400		romor cidinp
mend/pol/ucc	- 1			DQ5_48_2133		NC
Imped(B9) / VCC	p1			DQ5_48_2400		NC
imped(09) / VCC imped(82) / CBO				DQ5_IN_ODT120_2		NC
imped(B2) / GRO imped(B2) / GRO	UND q1			DQS_IN_ODT120_2		NC
7 / DOS0#	UND gi			DQ5_IN_ODT240_2		INC.
3 / DO00			ine col	DOS IN OD12411-2		
7 / DOS0			ancer			
2 / DO02						
7 / DQ01						
8 / DQ03						
2 / DQ06						
3 / DO04						
			111)
					Auto Pin Mapping	ilear All Recove

The corresponding model is assigned.

6. Click Next.

7. On Assign Composite IBIS Model Pins dialog, specify a new composite IBIS file name and click *Finish*.

Composite IBIS File Name	:	new_comp_file_na	ame
Circuit PinName	IBIS Sign	PinName / alName	Model
Lumped(B2)	p1 /	VCC	POWER
1	_ 4 4		CND

A new IBIS file is generated and populated in IBIS Editor.



Adding PKG Circuit

Similarly, you can add a package circuit. You need to select *Add PKG circuit* in the Select Mode section. The rest of the procedure is the same as adding a die circuit.

Add Die Circuit Add PKG Circuit Add PKG Circuit Add Die & PKG C	Pa Original IO t mo	l IBIS File Duffer dels	PSI / Pkg circu	Pin node XIM it model		
Ircuit File: D:V ICP SUBCKT: tut Connection Port: U2/	FileSpace\Work\Task\ASI	16_63_2014_01\AM	P ildour	IBIS Model Fil IBIS Compone	e: D:\FileSpace\Work\ ent: MT46V32M8TG	Task\ASI_16_63_2014_01V
NetName	SignalName					i one camp
Lumped(Y11) / VDD1	P1/VDD1.8V_CPU	POWER	NC	pwr1	NC	NC
Lumped(A3) / GND	G1 / GND	GND	gnd 1	NC	NC	NC
	01/010					
AD 18 / DOR_MDQ <6>	S1 / DDR_MDQ<	DQ_FULL	gnd 1	pwr1	gnd1	pwr1
AD 18 / DDR_MDQ<6> AD 19 / DDR_MDQ<9>	S1 / DDR_MDQ<	DQ_FULL	gnd1	pwr1	gnd1	pwr1
AD 18 / DDR_MDQ<6> AD 19 / DDR_MDQ<9> AD 21 / DDR_MDQ<1	S1 / DDR_MDQ<	DQ_FULL	gnd 1	pwr1	gnd 1	pwr1
AD 18 / DDR_MDQ<6> AD 19 / DDR_MDQ<9> AD 21 / DDR_MDQ<1 AE 17 / DDR_MDQ<1>	S1 / DDR_MDQ<	DQ_FULL	gnd 1	pwr1	gnd 1	pwr1
AD18 / DDR_MDQ<6> AD19 / DDR_MDQ<9> AD21 / DDR_MDQ<1 AE17 / DDR_MDQ<1> AE21 / DDR_MDQ<1	S1 / DDR_MDQ<	DQ_FULL	gnd 1	pwr1	gnd 1	pwr1
AD18 / DDR_MDQ <6> AD19 / DDR_MDQ <9> AD21 / DDR_MDQ <1 AE17 / DDR_MDQ <1> AE21 / DDR_MDQ <1 AF16 / DDR_MDQ <0>	S1 / DDR_MDQ<	DQ_FULL	gnd 1	pwr1	gnd 1	pwr1
AD 18 / DDR_MDQ <6> AD 19 / DDR_MDQ <9> AD 21 / DDR_MDQ <1 AE 17 / DDR_MDQ <1> AE 21 / DDR_MDQ <1>. AE 21 / DDR_MDQ <0> AF 16 / DDR_MDQ <0> AF 17 / DDR_MDQ S0	S1 / DDR_MDQ<	DQ_FULL	gnd 1	pwr1	gnd 1	pwr1
AD18 / DDR_MDQ<6> AD19 / DDR_MDQ<9> AD21 / DDR_MDQ<1 AE17 / DDR_MDQ<1> AE21 / DDR_MDQ<1> AE21 / DDR_MDQ<0> AF16 / DDR_MDQ<0> AF17 / DDR_MDQS0 AF19 / DDR_MDQ<7>	S1 / DDR_MDQ<	DQ_FULL	gnd 1	pwr1	gnd 1	pwr1
AD18 / DDR_MDQ<6> AD19 / DDR_MDQ<9> AD21 / DDR_MDQ<1 AE17 / DDR_MDQ<1> AE21 / DDR_MDQ<1> AE21 / DDR_MDQ<0> AF16 / DDR_MDQ<0> AF17 / DDR_MDQS0 AF19 / DDR_MDQ<7> AG17 / DDR_MDQ<3>	S1 / DDR_MDQ<	DQ_FULL	gnd 1	pwr1	gnd 1	pwr1
AD18 / DDR_MDQ<6> AD19 / DDR_MDQ<9> AD21 / DDR_MDQ<1 AE17 / DDR_MDQ<1 AE17 / DDR_MDQ<1> AE21 / DDR_MDQ<0> AF16 / DDR_MDQ<0> AF17 / DDR_MDQ<0> AF19 / DDR_MDQ<7> AG17 / DDR_MDQ<3> AG18 / DDR_MDQ<4>	S1 / DDR_MDQ<	DQ_FULL	gnd 1	pwr1	gnd 1	pwr1

Adding Die and Package Circuits

You can also add die and package circuits together.

omposite IBIS Model (Generation: Connect Di	ie/PKG Circuit to IBIS	Buffer Models			×
Select Mode Add Die Circuit Add PKG Circuit Add Die & PKG C	Pr Origina IO mo	ad node	Connection Port	l Connection Port 2	PS Pkg cir	Pin node I / XIM rcuit model
Circuit File: D:\ MCP SUBCKT: TC- Connection Port: U2 Layout PinName / NetName	samps\TC4_CFG2_R1_2 4_CFG2_R1_20130429_ IBIS PinName / SignalName	0130429_x1_082713_	Pulldown	IBIS Model File: IBIS Componen	D:\samps\ssi_pba_ t: Memory GND Clamp	ex.ibs
	n1 (TOVP	POWER	NC	DWF1	NC	NC
GND1 / GND	al (GND	GND	andi	NC	NC	NC
DO0/PP DO0	s1 / PP_DO0	DDR3L DO40 ODT	3			
DO1 / PP DO1						
DO2 / PP_DO2						
DO3 / PP DO3						
DO4 / PP DO4						
DOS/PP DOS						
DOG/PP DOG						
DO7 / PP DO7						
DOSN (PP. DOS0. N						
DOSP (PP_DOSP						
•		111				•
					Auto Pin Mapping	Clear All Recover

To do this, you need to add a PKG circuit file and assign signal models for signal pins.

1. Specify a PKG circuit file.

Ensure that there are at least one power, one ground pin, and one signal pin.

2. Click Next.

3. Select the PKG model file (.ckt).



The MCP Header Editor dialog appears for connecting the PDN and PKG circuits. It
displays the unconnected signal and power and ground nets.

MCP Header Editor			×
Model File: D:\samps\TC4_C	FG2_R1_20130429_x	_short.ckt	
Sub-circuit	Туре	Conn. Port	Туре 📥
TC4_CFG2_R1_20130429_x		C119 NewEmptyCkt1 R26 DDR4_DIMM2 DDR4_DIMM1	
😑 Signal Net(s)	-> Signal Net	PinName / CktNodeName / NetN X Y	Thru Conn. Port
DDR4_DIMM1_2 DDR4_DIMM1_4 DDR4_DIMM1_9 DDR4_DIMM1_11 DDR4_DIMM1_145 DDR4_DIMM1_147 DDR4_DIMM1_147 DDR4_DIMM1_150 DDR4_DIMM1_152 DDR4_DIMM1_154 DDR4_DIMM2_2 DDR4_DIMM2_4 DDR4_DIMM2_9 DDR4_DIMM2_145 DDR4_DIMM2_147 DDR4_DIMM2_147 DDR4_DIMM2_150 DDR4_DIMM2_152 Filter:	-> Power Net -> Ground Net Select ckt node(s) and add it(them) to the selected Conn. Port.	Signal Net(s) Image: signal Net(s) 3 / DDR4_DIMM1_2 / Si 5 / DDR4_DIMM1_2 6 / DDR4_DIMM1_2 6 / DDR4_DIMM1_2 9 Power Net(s) Image: signal Net(s) 1 / C119_1 / VDD_DIMM Image: signal Net(s) 3 / C119_1 / Power Image: signal Net(s) 2 / C119_2 / GND Image: signal Net(s) 9 / NewEmptyCkt1_2 / Image: signal Net(s)	DDR4_DIMM DDR4_DIMM
		Edit XNet OK	Cancel

4. Select the circuit nodes (signal/power/ground net) and add them to the selected connectivity port and click *OK*.

5. Connect the on-die circuit model nodes with the PKG circuit model nodes either manually or using the Auto Connect feature, which you can access by clicking the *Auto Connect* button.

Composite IBIS Mode	I Generation: Connect Die and PKG Circuits		X
Pad node Original IBIS Fi IO buffer models	le XPI On-die circuit model	Pin r PSI / XIM Pkg circuit mod	del Contection Port 2
On-die Model File: Sub Circuit Name: Conn. Port: PinName / CktN	D:\samps\TC4_CFG2_R1_20130429_x1_short.c TC4_CFG2_R1_20130429_x1_BB5_Foster DDR4_DIMM1 IodeName / NetName	kt PKG Model File: Sub Circuit Name: Conn. Port: PinName / CktNod	D:\samps\Sample_DIMM_BBS.ckt Sample_DIMM J1 Indextage In
B3 / DDR B7 / DDR C2 / DDP C7 / DDP C8 / DDP E3 / DDP E3 / DDP E7 / DDP E8 / DDP	<pre>k1_DIMM1_1419P_DQ205_V (4_DIMM1_150 / PP_DQ50 (4_DIMM1_150 / PP_DQ2 (4_DIMM1_11 / PP_DQ2 (4_DIMM1_147 / PP_DQ1 (4_DIMM1_154 / PP_DQ3 (4_DIMM1_9 / PP_DQ6 (4_DIMM1_9 / PP_DQ6 (4_DIMM1_2 / PP_DQ4 (4_DIMM1_152 / PP_DQ7 (4_DIMM1_145 / PP_DQ5 B2) / DDR4_DIMM1_1 / GND</pre>	B3/31_5/ B7/31_12 C2/31_15 C7/31_2 C2/31_15 C7/31_7/ E3/31_4/ E7/31_18 C8/31_17 D2/31_16 E8/31_6/ VDD1/31	DQ00 DQ00 / DQ50 / DQ02 DQ01 DQ04 / DQ07 / DQ03 / DQ03 / DQ06 DQ05 76 / VCC ▼
7		Auto Connect Launch MCP Heade	er Editor Auto net property overwrite < Back

Finally, the Assign Composite IBIS Model Pins dialog appears. This is where you specify a new IBIS file name and component name.

6. Click Finish.

Generating IBIS Component from Layout

The workflow provides the ability to generate an IBIS model from the layout.

Workflow	×
IBIS Editor	۵
View/Edit IBIS File	
View IBIS Curves	
Add Die and/or PKG Circuits	
Generate IBIS [Component] from Layout]
 Run Golden Parser Check	
Save IBIS File	1
Customize Workflow	×

This option is enabled only when the layout component information is provided from a board (.brd) file by Allegro Sigrity SI or a .spd file by other Sigrity tools.

ayout File:):\samps\		IBIS Model File:	D:\samps\I803865-1.ib	S
ayout Comp Name: [J17 🔽		IBIS Component:	I803865-1 💌	Import IBI
Layout PinName / NetName	IBIS PinName / SignalName	Model Name	Pulldown	Pullup	GND Clamp
1/D0					
2/GND					
5 / GND					
6 / VCC					
8 / VCC					
9 / VCC					
10 / VCC					
11 / GND					
12 / GND					
13 / GND					
14 / GND					
21 / 000	111				

The layout components are loaded from the calling application, such as Allegro Sigrity SI and the IBIS components are in the current IBIS file.

Note: The pin names and the net names must be consistent between layout and IBIS file.

You can import more models from other IBIS file into current IBIS text using the *Import IBIS* function. These models are used for assigning models.

- 1. Click the Edit icon in the Model Name cell for a layout net.
- 2. Select a model from the IBIS models file for the corresponding pin/net from the layout.

Pin Name	Signal Name	Model Name	File Name
5	GND	GND	D:\samps\I803865-1.ibs
		GND	D:\samps\1803865-1.ibs =
		POWER	D:\samps\I803865-1.ibs
		Z372091_BI108	D:\samps\I803865-1.ibs
		ADDR	D:\samps\ssi_pba_ex.ib:
		CLK	D:\samps\ssi_pba_ex.ib:
		CTRL	D:\samps\ssi_pba_ex.ib:
		DDR3L_DQ40_NO	D:\samps\ssi_pba_ex.ib:
		DDR3L_DQ40_ODT	D:\samps\ssi_pba_ex.ib:
		DDR3L_DQ48_NO	D:\samps\ssi_pba_ex.ib:
		DDR3L_DQ48_ODT	D:\samps\ssi_pba_ex.ib:
		DDR3L_DQS40_NO	D:\samps\ssi_pba_ex.ib:
		DDR3L_DQS40_ODT	D:\samps\ssi_pba_ex.ib
•		DDR3L DOS48 NO	D:\samns\ssi nha ex.ib
ок с	ancel		

3. Click OK.

Generate IBIS from Lay	yout							×
Layout File:	D:\samps\ U17 🔹		IBIS IBIS	Model File: Component:	D:\samps\I803 I803865-1	3865-1.ibs	Import	IBIS
Layout PinName / NetName	IBIS PinName / SignalName (Sort By Pin)	Model Name	Pullo	lown	Pullup		GND Clamp	
1/D0	1 / D0	Z372091_BI108						
2 / GND	2 / GND	GND						
5 / GND	5 / GND	GND						
6 / VCC	6 / VCC	POWER						
8 / VCC	8 / VCC	POWER						
9 / VCC	9 / VCC	POWER						
10 / VCC	10 / VCC	POWER						
11 / GND	11 / GND	GND						
12 / GND	12 / GND	GND						
13 / GND	13 / GND	GND						
14 / GND	14 / GND	GND		_				
	111			J				
Save Connected P	ins Only					ок	Can	cel

4. Click OK to close the Generate IBIS from Layout dialog.

```
[Ibis Ver]
           3.1
                                                              .
[File Name] i80386s-1.ibs
[File Rev] 0.5
                                                              Ξ
[Date]
              January 17, 2014
[Notes] This file is automatically generated and may not fully compl
      with some of the name length and numerical size restrictions
      IBIS Specification. These length and size violations can be
      detected with the IBIS Open Forum ibischk3 utility, and the
      violations may need to be corrected before the file can be
      used outide of the Interconnectix environment.
L
[Component] I80386S-1
[Manufacturer]
              Extracted from Interconnectix IS
[Package]
    typ
           min
                 max
Т
R pkg
        0.0
               NA
                   NA
L pkg
        O.OH
               NA
                   NA
        O.OF
               NA
                   NA
C pkg
[Pin]
        signal name
                      model name
                                     R pin
                                              L pin
                                                      C pin
                      Z372091 BI108
1
        DO
        GND
2
                      GND
٠
                          ш
```

The new IBIS file will contains only those components that you selected from the layout.

Running Golden Parser Check

Use golden parser to check the integrity of the IBIS models file.

AMM IBIS Editor [IBIS ver] Workflow × 🖹 [File name] [IBIS ver] 5.0 **IBIS Editor** File Rev] [File name] ssi_pba_ex.ibs View/Edit IBIS File [File Rev] 1.0 Date] October 24, 2012 View IBIS Curves [Date] [] [Source] [Notes] [Source] Generic memory device Add Die and/or PKG Circuits [Disclaimer] [Notes] Created memory controller from a memory device [Copyright] [Disclaimer] Just an example file Generate IBIS [Component] from L IComponent] Memory [Copyright] Copyright 2012 Cadence Design Systems, Inc. All right 🗄 🏦 [Component] Controll Run Golden Parser Check 🖹 [Model Selector] DQ ****** 🖹 [Model Selector] DM Save IBIS File [] [Model Selector] DQS [Component] Memory **Customize Workflow** × [Model Selector] ADDR [Manufacturer] Cadence Design Systems, Inc. [Model Selector] CTRL [Package] The Imodel Selector CLK | variable typ min max 🗄 🛃 [Model] DDR3L_DQ40_I R_pkg 1.0146 0.97286 1.0957 L_pkg C_pkg 🗄 🔂 [Model] DDR3L_DQ40_ 7.151e-9 6.591e-9 7.955e-9 3.058e-12 2.634e-12 3.335e-12 🗄 🔂 [Model] DDR3L_DQ48_I 🗄 🛃 [Model] DDR3L_DQ48_ [Pin] с signal name model name R pin L_pin 🗄 🛃 [Model] DDR3L_DQS40 A1 VDDQ POWER ----ш Editor × Checking C:\Users\soniap\AppData\Local\Temp\SPDGEN6068\ssi_pba_ex.ibs for IBIS 5.1 Compatibility... WARNING (line 637) - Model DDR3L_DQ40_NO_ODT: C_comp_pullup min value is not the smallest value listed WARNING [line_637] - Model DDR3L_DQ40_NO_ODT: C_comp_pullup max value is not the largest value listed NOTE (line`661) - Púlldown Minimum data is non-monotonic NOTE (line 664) - Pulldown Typical data is non-monotonic NOTE (line 667) - Pulldown Maximum data is non-monotonic NOTE (line 749) - Pullup Typical data is non-monotonic NOTE (line 750) - Pullup Minimum data is non-monotonic NOTE (line 753) - Pullup Maximum data is non-monotonic NOTE (line 893) - GND Clamp Maximum data is non-monotonic NOTE (line 895) - GND Clamp Typical data is non-monotonic 111

The result of model parsing are displayed in the Editor pane.

All the warnings and errors encountered in the IBIS file are listed along with the line numbers on which they were found. You can double-click an error/warning message to jump to the corresponding line in the IBIS file and edit the file.

Saving the IBIS File

Use this command to save the IBIS file.

SPICE Model Management

SPICE Editor is a supported module of Analysis Model Manager. SPICE Editor facilitates management of SPICE model files and helps you ensure the integrity of the model data. It provides you an easy-to-use editing environment to create and validate models quickly.

Launching SPICE Editor

You can launch IBIS Editor from the AMM user interface. To launch SPICE Editor:

- 1. Open the library containing SPICE models in AMM.
- 2. Select a model name from the list.
- **3.** Click the *Edit* button in the Setup dialog of SPICE model, the SPICE Editor will pop up and load the selected SPICE file automatically.



SPICE Editor		×
Sub-circuit	-Local Parameter	_
Name	Name ∇ Value	
cdn_ddr3_package		
Create Delete	Create Delete	
Definition	External Nodes	5
.MODEL Spara S + BNPFILE = "cdn_ddr3_package.bnp" S + DIE_A5 DIE_A4 + DIE_D11 DIE_A4 + DIE_D12 DIE_A4	DIE_A5_DIE_A4_DIE_D11_DIE_D12 DIE_B11_DIE_B12_DIE_D16_DIE_D17 DIE_B16_DIE_B17_DIE_C11_DIE_C12 BGA_K2_BGA_A1_BGA_W21_BGA_W20 BGA_AB19_BGA_AA19_BGA_V21_BGA_AA21 BGA_W19_BGA_V19_BGA_AA20_BGA_AB20	
+ DIE_B11 DIE_A4 + DIE_B12 DIE_A4	Header/Footer	
+ DIE_D16 DIE_A4 + DIE_D17 DIE_A4	+ DIE_A5	1
+ DIE_B16 DIE_A4 + DIE_B17 DIE_A4	+ DIE_A4 + DIE_D11	
+ DIE_C11 DIE_A4 + DIE_C12 DIE_A4	+ DIE_D12 + DIE_B11	
+ BGA_K2_BGA_A1 + BGA_W21_BGA_A1	+ DIE_B12 + DIE_D16	
+ BGA_W20 BGA_A1 + BGA_AB19 BGA_A1	+ DIE_017 + DIE_B16	
+ BGA_AA19 BGA_A1 + BGA_V21 BGA_A1	+ DIE_B17 + DIE_C11	
+ BGA_AA21 BGA_A1 + BGA_W19 BGA_A1	+ DIE_C12 + BGA_K2	
+ BGA_V19 BGA_A1 + BGA_AA20 BGA_A1	+ BGA_A1 + BGA_W21	
+ BGA_AB20 BGA_A1 + MNAME = Spara	+ BGA_W20 + BGA_AB19	
*	+ BGA_AA19 + BGA_V21	
Error Check Import MCP Header	Read Only	
MCP Header Editor Whole Text View	Save Cancel	

The SPICE Editor launches with the spice circuit file.

Working with SPICE Editor

In SPICE Editor, you can perform the following functions:

- Create a New Sub-circuit
- Edit Model Definition
- Create or Delete a Local Parameter
- Edit MCP Header Information
- <u>View Whole Text of the Model File</u>

Create a New Sub-circuit

You can create a new sub-circuit in SPICE Editor.

1. Click Create.

A new blank line appears

2. Specify a name and press Enter.

Sub-circuit
Name
DDR2_s2k_sample_test1_T2_110210_132203
Create Delete

You can also delete the selected sub-circuits. Observe that the External Nodes, Definition, Local Parameter, and Header/Footer information is refreshed based on the selected sub-circuit. By default, the first sub-circuit is selected.

Edit Model Definition

You can edit the model definition in the *Definition* edit area. You can import MCP header information from a sub-circuit of any other circuit file.

1. Click Import MCP Header.

Load MCP Head	ler ×
Circuit File:	D:\work\%its\PCIE\PCIe3.0_production_kit_v_2.1.1\PCIe3.0_production_kit_v_2.1.1\PCIe3.0_
Sub-circuit:	postroutenew 🗸
Matched Sub	-circuit Node: 0; Unmatched Sub-circuit Node: 6
	OK Cancel

2. In the Load MCP Header dialog, select the circuit file and then the sub-circuit name and click *OK*.

When a sub-circuit is selected, the number of sub-circuit nodes matched or unmatched with those in current sub-circuit is displayed. Also, the original MCP header information in the definition is replaced by the imported MCP header.

Create or Delete a Local Parameter

You can also create or delete a local parameter.

Name	∇	Value
new_loc		1.0
Edit MCP Header Information

MCP header information can be edited in the MCP Header Editor.

1. Click *MCP Header Editor* to open the MCP Header Editor.

ub-circuit		Туре		Conn. Port			Туре
)IMM_conn_R			ř]			
kt Node							
1		-> Signal Net	Pir	Name / CktNodeName / NetN	x	Y	Thru Conn. Port
3			-				
4			-				
5		-> Power Net	Ŀ				
6	=		Ŀ				
7		Cround Nat					
8		-> Ground Net					
9			Ŀ				
10		Select ckt node(s)	E				
11		and add it(them) to	E				
12		Port.	E				
13							
14							
15							
241							
242							
243							
244							

- 2. Add a connectivity port or select an existing connectivity port.
- **3.** Select a circuit node from the list and add it to the selected connectivity port as a signal, power, or ground net.

4. Repeat step 3 for adding more signal/power/ground nets.

MCP Header Editor				×
Sub-circuit	Туре	Conn. Port		Туре
DIMM_conn_R		cn1 cn2		
Ckt Node $ riangle$	A			
241	S Signal Mat	PinName / CktNodeName / NetN	X	Y Thru Conn. Port
242	-> bighar Nec	Signal Net(s)		
243		1/3/Signal1		
244	-> Power Net	Power Net(s)		
245	L	2 / 250 / Power		
247		: 🖂 Ground Net(s)		
248	-> Ground Net	3 / 246 / Ground		
249				
251	Colorbald and (a)			
252	and add it(them) to			
200	 -> Signal Net -> Power Net -> Ground Net Select ckt node(s) and add it(them) to the selected Conn. Port. 			
255	Port.			
Signal Net(s)	-> Power Net -> Ground Net Select ckt node(s) and add it(them) to the selected Conn. Port. =			
3				
Power Net(s)				
250				
Ground Net(s)	Ų			
Filter:				
		Edit XNet	ОК	Cancel

You can also delete a selected pin/net from the list or move it from one group to another.

PinN	ame / CktNo	odeName / NetN	x	Y	Thru Conn. Port
	Signal Nel	t(s)			
	1 / Power	Delete Selected F	Pins		
-	2/	Set As Power Ne	t Group		
•	Grouni 3 /	Set As Ground N Set As Signal Net	et Group t Group		
		Auto Lump Pins Lump Selected P Detach Lumped	Auto Lump Pins By Net .ump Selected Pins Detach Lumped Pins		

- 5. Click OK to close the MCP Header Editor dialog.
- 6. Click Save in SPICE Editor to save the changes you have made.

View Whole Text of the Model File

SPICE Editor provides a quick view of the complete text of the sub-circuit file.

→ Click the Whole Text View button to open Whole Text View.

1 T				
iole Lext View				
.SUBCKT DDR2_s2	k_sample	e_test1_T2_11021	0_132203	
+ vrm_18_1 vrn	n_18_2	U20_AC8 U20_A	3 U20_AF16 U20_AE17 U20_AH17 U20_AG17 U20_AG18 U20_AH18	
+ U20_AD18 U2	20_AF19	U20_AH19_U20_	_AD19 U20_AG20 U20_AH20 U20_AH21 U20_AE21 U20_AH22 U2 <u>0_AD21</u>	
+ U20_AG10 U2	20_AH9	U20_AH8 U20_A	D11 U20_AH7 U20_AG7 U20_AF8 U20_AD10 U20_AE9 U20_AH6	
+ U20_AH5 U20)_AG6 U	J20_AH4_U20_AE	6 U20_AD8 U20_AF5 U20_AF17 U20_AG21 U20 <u>_AG9 U20_AF7</u>	
+ U17_A1 U17_	A3 U17	_F9 U17_G8 U1	7_H3_U17_H9_U17_F1_U17_H1_U17_G2_U17_H7	
+ U17_D9 U17_	C8 U17	_B9_U17_D7_U1	7_D1 U17_B1 U17_C2 U17_D3 U17_F7 U17_B7	
+ U23_A1 U23_	A3 U23	_H1_U23_H3_U2	I3_G2_U23_F1_U23_H7_U23_H9_U23_G8_U23_F9	
+ U23_B1 U23_	D3 U23	_D1_U23_C2_U2	<u>3_D7_U23_D9_U23_B9_U23_C8_U23_F7_U23_B7</u>	
+ new_loc = 1.0				
*[MCP Begin]				
*[MCP Ver] 1.2				
*[MCP Source] Ca	dence De	esign Systems, Inc.	MCP Editor	
*				
*[REM]*********				
*[Connection] U21	DOWNST	REAM 55		
*[Connection Type	3			
*[Ground Nets]	CN	0.0740077		
*A1 U2_A1	GND	0.0/192//	0.121112	
*U2_A4_U2_A1	GND	0.0795477	0.121112	
"UZ_A5_UZ_A1	GND	0.0820877	0.121112	
"UZ_A8_UZ_A1	GND	0.0897077	0.121112	
*U2_A9_U2_A1	GND	0.0922477	0.121112	
"UZ_AILUZ_AI	GND	0.0973277	0.121112	
"UZ_AI4 UZ_AI	GND	0.1049480.121		
TUZ_DI UZ_AI	GND	0.0719277	0.116572	
*DE UD A1	GND	0.0770077	0.110572	
*DD UZ_AI *DC UD_A1	GND	0.0020077	0.116572	
*D0 U2_A1	GND	0.0047977	0.116572	
*D10 U2_A1	GND	0.0947077	0,110372	
*C1 U2_A1	CND	0.1049400.110	0.115023	
*C1 U2_A1	CND	0.0713277	0.110032	
*U2_05_U2_A1	GND	0.0744077	0.116032	
912_C3_U2_A1	CND	0.0020077	0.110022	
*12 C0 U2_A1	GND	0.0037077	0.116032	
*12 C10 U2_A1	GND	0.0947877	0.116032	
*12 C11 U2 A1	GND	0.0973277	0.116032	
*12 C12 U2_A1	GND	0.0998677	0.116032	
*112 D3 112 Δ1	GND	0.0770077	0.113492	
*112 D14 L12 A1	GND	0 104948 0 113	3492	
年1 112 41	GND	0.0719277	0 110952	
*F14 U2_A1	GND	0.104948.0_108	3412	
*G1 U2_A1	GND	0.0719277	0.105872	
01 02_AI	CIND.	0.0000677	0.105972	
*G12 II2 ∆1	GND	1111998577		

Capacitor Model Management

Refer to the *Working with Capacitor Libraries* chapter of *OptimizePI User Guide* (OptimizePI_UG.pdf). You can access this user guide from *Help – Documents* menu of the Allegro Sigrity tool.