XtractIM User’s Guide

Product Version 16.6
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Table of Contents

Chapter 1

Introduction

Welcome to the XtractIM User’s Guide. This manual is designed to give you a brief introduction to the XtractIM application by providing real life examples and demonstrations so you can understand some of the basic concepts of the XtractIM application.

System Requirements

Please refer to ***Installation Guide*** to check the system requirements.

How to Use This Guide

This guide provides descriptions, demonstration examples and step-by-step instructions on how to get the desired results with the XtractIM tool.

Additional Documentation

In addition to this document, refer to the following documentation for additional information.

- ***.spd File Format Reference Guide*** explains the format of the Sigrity .spd file. Files must either be created as a .spf file or translated from another format into .spd file format.
- ***Translators User’s Guide*** explains how to translate layout data contained in various file formats into the Sigrity .spd file format.

Conventions Used in This Guide

Convention	Use
Bold	GUI text, special names, terms (window names, buttons, menus, etc.)
`Arial`	Examples
>	Menu hiearchy

How to Contact Technical Support

We are committed to helping you in using XtractIM. If you have any questions, contact the *Cadence Online Support*.

Chapter

2

Learning the Basics

This chapter describes the basics of the XtractIM application.

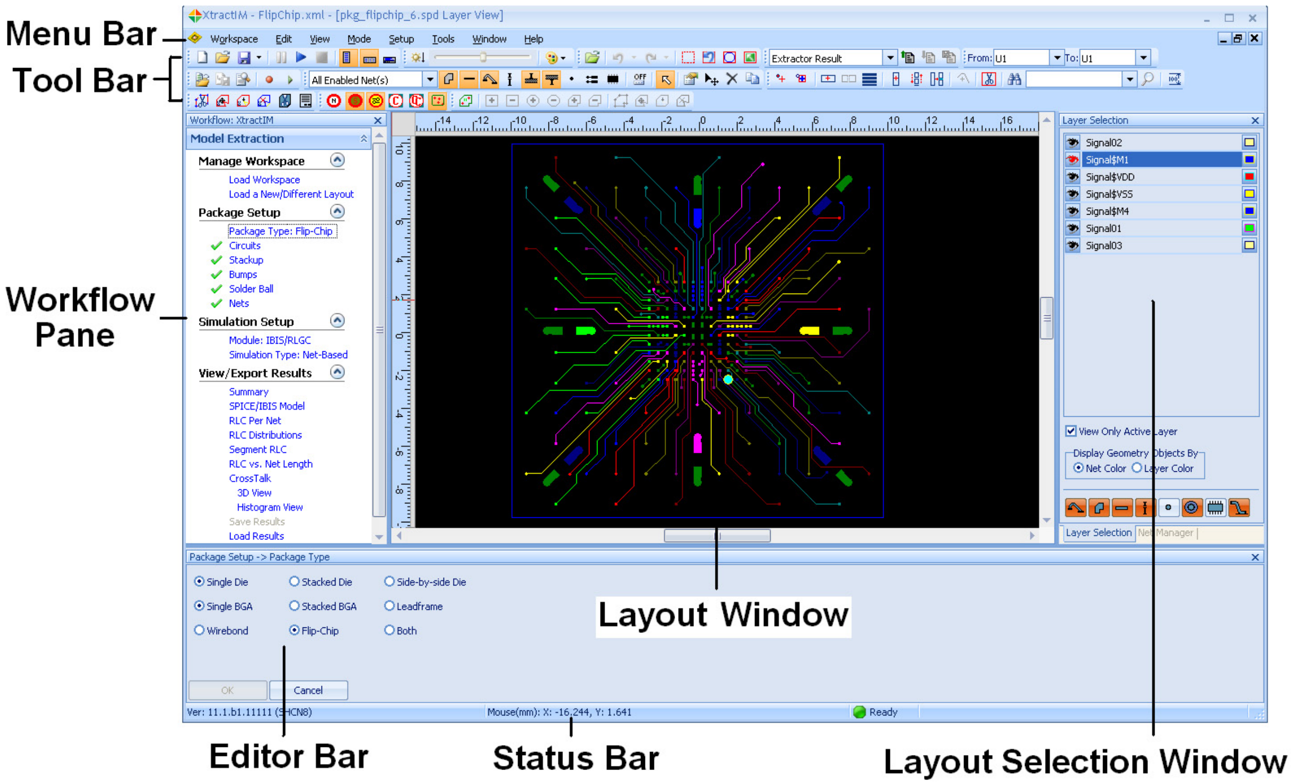
Using XtractIM

1. Load a layout file (also called a package file).
2. Create a Workspace.
3. Save the workspace for future use. You'll use this workspace to prepare for the simulation.
4. Run the simulation.
5. View the results.
6. Repeat theses steps, as needed, to change your settings.
7. Run the simulation as many times as you need.

The Workflow Pane

The workspace is made up of the **Workflow** pane and the **Layout Area**. All the workflow tasks are listed in the Workflow pane. Tasks of the same type are sorted and listed together. When a task is clicked, details associated with that task appear in an **Editor** pane.

- Check results
- Modify a design
- Report results.
- Run a simulation
- Set up a simulation



- **Editor pane** — A spreadsheet. Users can easily input information into the pane for simulation setup or check the simulation results in the pane.
- **Layout Selection Window** — Controls the active layer, displayed layers and the object display on or off.
- **Layout Window** — Edit your layout file.
- **Status Bar** — Shows the version information, the current *X-Y* coordinates of the cursor and the simulation progress.
- **Tool Bar** — Quick access icons for common XtractIM commands.

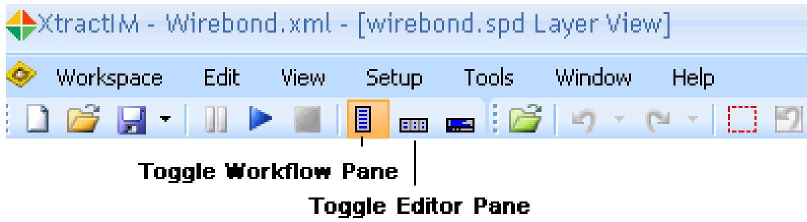
Using the Workflow Pane

The Workflow pane includes Manage Workspace, Package Setup, Simulation Setup, and View and Export Results.

- **Layout Area** — Displays the configuration of the layout file.
- **Workflow Tasks** — For different packages vary slightly.

Show and Hide Icons

When you click on the **Show** and **Hide** icons in toolbar, the selected item is displayed or hidden.



Net-Based Extraction on Single-BGA Package

Workflow Task	Description
Manage Workspace	Load workspace and/or layout file.
Load Workspace	Load in an existing workspace.
Load a New/Different Layout	Create a new layout file or remove the current layout file and load in a desired layout file.
Package Setup	Set up all basic parameters for simulation.
Package Type	Wirebond or Flip-chip, Single-BGA or Stacked-BGA.
Circuit	Select/deselect Die circuit or Board circuit.
Stackup	Setup the Stackup parameter of a package.
Bumps	Seup Bumps parameters for a Flip-chip package.
Solder Ball	Set Solder Ball parameters.
Nets	Select the desired nets for RLC extraction.
Simulation Setup	
Module	IBIS/RLGC or Optimized Broadband.
Simulation Type	Choose from Net-based and Pin-based.
View / Export Results	
Summary	View the RLC matrix, the minimum and maximum R, L, C values.
SPICE/IBIS Model	View the SPICE model, IBIS .pkg model and IBIS .ibs Pin model.
RLC Per Net	2D display of R, L and C value for each net.
RLC Distributions	3D display of R, L and C full matrix values.
Segment RLC	View segment RLC on each metal layer.
RLC vs.Net Length	2D Display of R, L, and C, vs. net length for signal nets.

Workflow Task	Description
Crosstalk	View the near-ended and far-ended crosstalk among signal nets.
Save Results	Save the result on hard disk. A text file and a binary file with the extension .xim will be saved.
Load Results	Load in the saved results on display.

Net-Based Extraction on Stacked-BGA Package

Workflow Task	Description
Manage Workspace	Load workspace and/or layout file.
Load Workspace	Load in an existing workspace.
Load a New/Different Layout	Create a new layout file or remove the current layout file and load in a desired layout file.
Package Setup	Set up all basic parameters for simulation.
Package Type	Wirebond or Flip-chip, Single-BGA or Stacked-BGA.
Circuit	Select/deselect Die circuit or Board circuit.
Stackup	Setup the Stackup parameter of a package.
Bumps	Seup Bumps parameters for a Flip-chip package.
Solder Ball	Set Solder Ball parameters.
Nets	Select the desired nets for RLC extraction.
Simulation Setup	
Module	IBIS/RLGC or Optimized Broadband.
Simulation Type	Choose from Net-based and Pin-based.
View / Export Results	
Summary	View the minimum and maximum R, L, C values.
SPICE Model	View the SPICE model, RLC for each path (Die-toBGA1, Die-to-BGA2, BGA1-to-BGA2).
Branch RL	View each branch R and L of the generalized T-topology circuit.
Save Results	Save the result on hard disk. A text file and a binary file with the extension .xim will be saved.
Load Results	Load in the saved results on display.

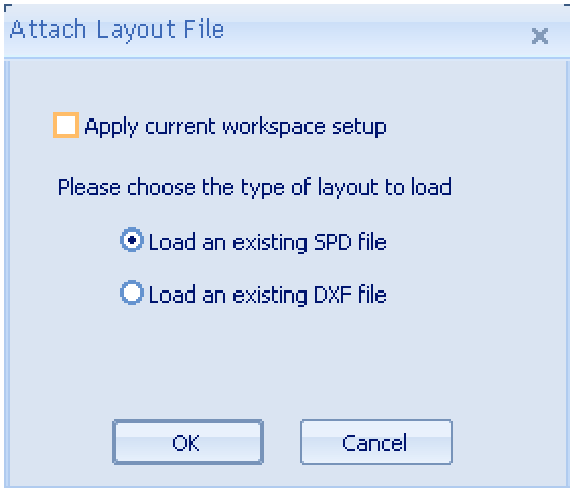
Pin-Based Extraction

Workflow Task	Description
Manage Workspace	Load workspace and/or layout file.
Load Workspace	Load in an existing workspace.
Load a New/Different Layout	Create a new layout file or remove the current layout file and load in a desired layout file.
Package Setup	Set up all basic parameters for simulation.
Package Type	Wirebond or Flip-chip, Single-BGA or Stacked-BGA.
Circuit	Select/deselect Die circuit or Board circuit.
Stackup	Setup the Stackup parameter of a package.
Bumps	Seup Bumps parameters for a Flip-chip package.
Solder Ball	Set Solder Ball parameters.
Nets	Select the desired nets for RLC extraction.
Simulation Setup	
Module	IBIS/RLGC or Optimized Broadband.
Simulation Type	Pin-based.
View / Export Results	
Summary	View the minimum and maximum R, L, C values.
SPICE Model	View the SPICE model.

Working on a Layout File

Working on layout files includes working with package layers, objects, nets, vias, traces, shapes, nodes, wirebonds, stackups, etc.

1. Open the **Attach Layout File** window.



2. To apply the current workspace setup, click

   Apply current workspace setup

3. To load a desired SPD layout file, click

   Load an existing SPD file

4. To load a desired DXF layout file, click

   Load an existing DXF layout

.spd File Format

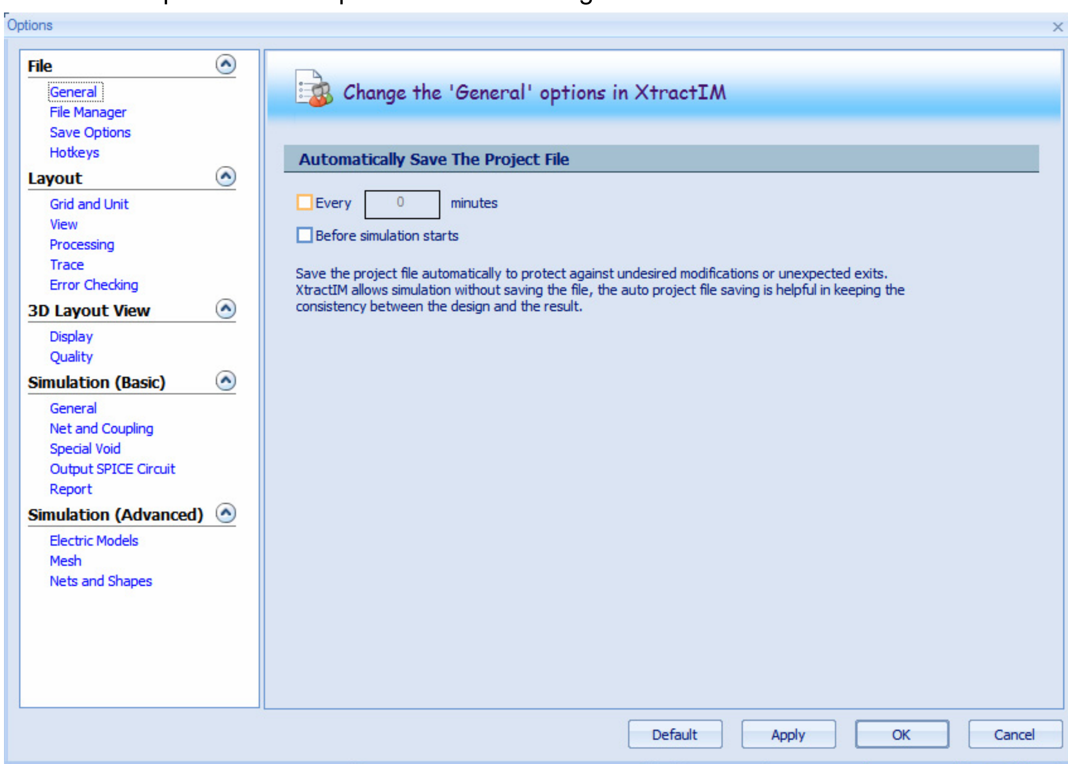
The layout file is in Sigrity .spd file format. As part of the Sigrity family of products, XtractIM includes file format translators which translate the following file formats in .spd files for simulation.

- Cadence .brd, .mcm, and .sip files
- Cadvance .dbr files
- Mentor BoardStation ASCII design outputs files
- Mentor Expedition .hkp files
- Mentor PADS .asc files
- P-CAD .pcb files
- Zuken CADStar & Visula .rif files
- Zuken CR5000 .pcf, .ftf, and .mrf files

File Manager

You may specify the directories where output files of different types are placed.

Tools > Options > Edit Options... > File Manager



File Folders

- **Black items** — Editable. The default value of the temporary folder is the operating system's temporary folder. Other default values include the directory where the current case is located.
- **Gray items** — Not editable. Indicate current working paths.

File Name Pattern

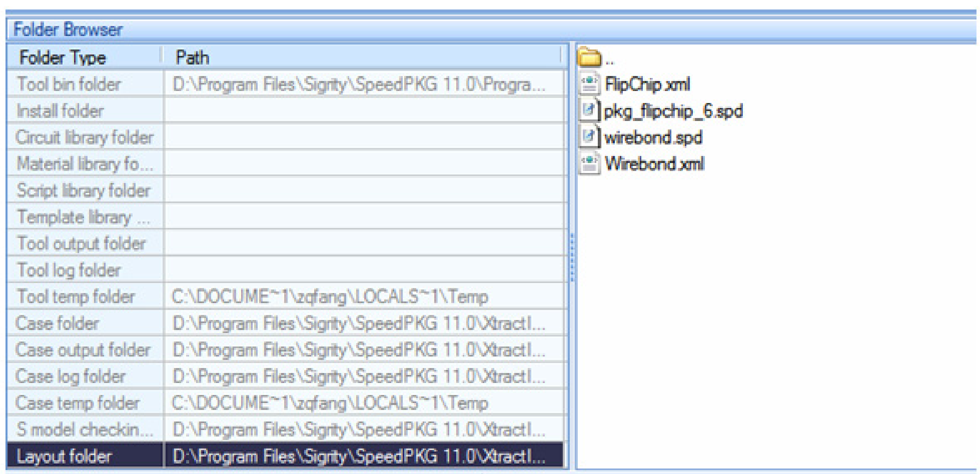
The names of the output files are customized.

[W]	Workspace Name
[L]	Layout Design Name
[Y]	Year
[M]	Month
[D]	Day
[h]	Hour
[m]	Minute
[s]	Second

Folder Browser

The Folder Browser goes through files in special folders. Select:

View > Pane > Folder Browser



Click on a folder in the left side of the window. The folder contents are displayed in the right side of the window.

Double-click on a file in the right list to open the file. A pop-up window displays file information the cursor hovers over the filename.

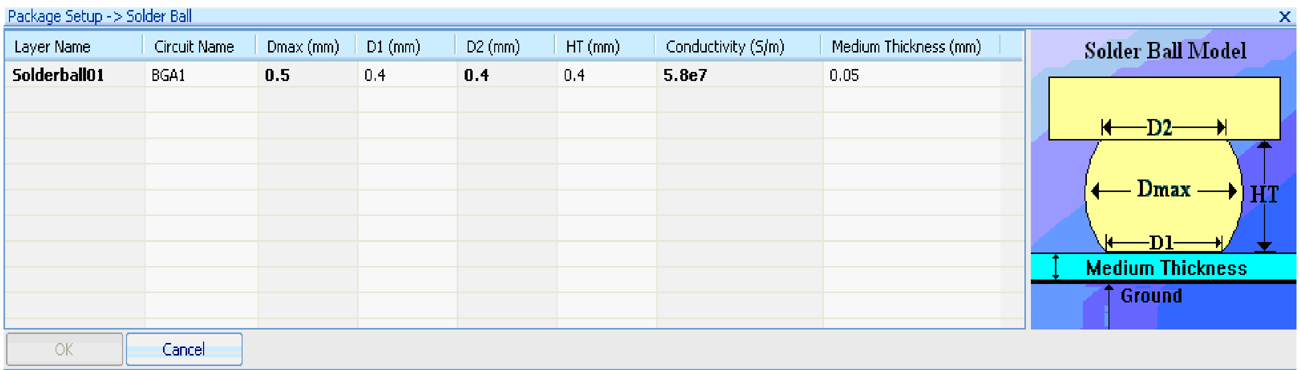
NOTE!	Currently, Sigrity analysis tools do not offer any folder type containing multiple items.

Prepare for Simulation

To prepare for the simulation you need to set all the parameters in the Package setup.

- Symbol next to an item is a reminder that this item has not been set.
- Symbol next to an item means it has been set.

1. Click on an item under **Package Setup** in the Workflow pane. Our example shows Solder Ball selected and displayed.
2. An Editor pane opens across the bottom of the workspace. You can easily input all information for the Solder Ball model.



Save Workspace Files

After having gone through each step in the Package setup, you can save the workspace in ***.ximx format**. This *.ximx file includes the **.spd file name** and all the settings in the Package setup.

NOTE	Since version 12.0, XtractIM workspace file is named with the extension "*.ximx". An .ximx file includes the .spd file name but, does **not** include the actual layout of the .spd file.

Save a Workspace

1. To save a newly created workspace, select

   Workspace > Save

2. Enter a name for the new workspace.
3. To save the existing workspace under a different name, select

   Workspace > Save as

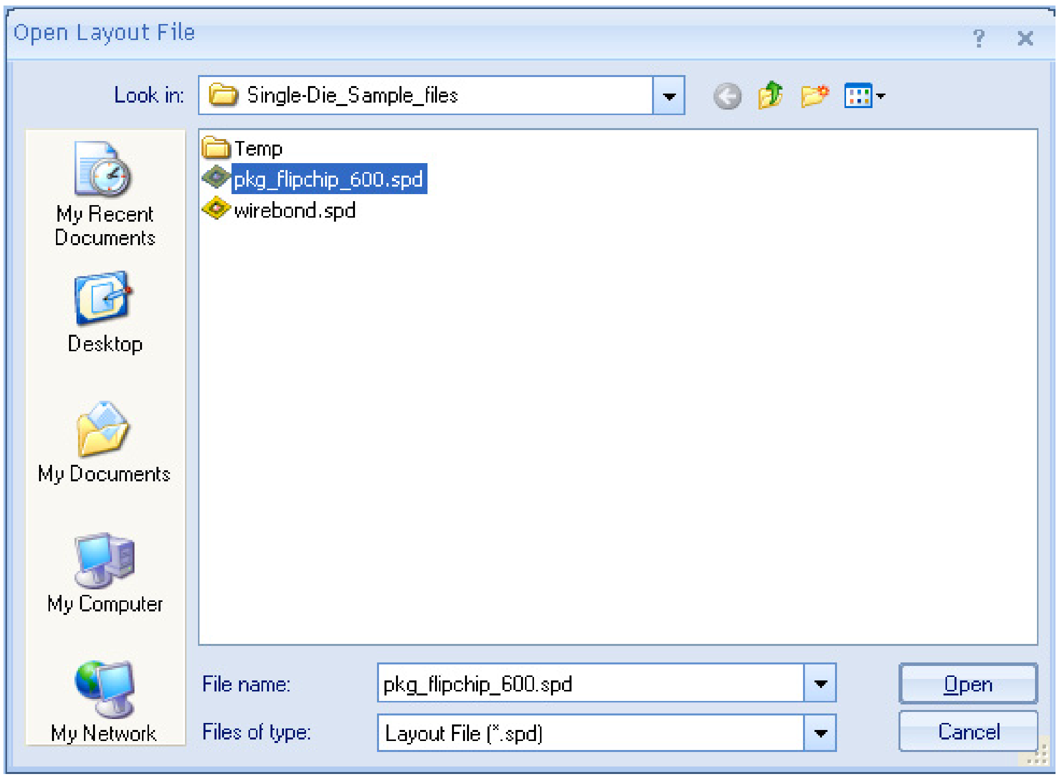
4. Enter the new name.

Load Workspace

1. To load an existing workspace and its associated layout file, select

   Load Workspace

2. If the associated layout file does not exist in the same directory as the workspace file, the following window opens.



3. Choose the desired layout file from the list shown in this new window. For example: pkg_flipchip_600.spd.

RUN THE SIMULATION AND VIEW RESULTS

1. Click on the **Start** icon  in the Toolbar to run the simulation.

   XtractIM only extracts RLCG for the net which has at least one pin at the Die side and at least one pin at the board side.

2. At the beginning of the simulation, if some nets have Die-Board mis-match, a pop-up window asks you to select the next action.

   - **Continue** — Continue the simulation.
   - **More Information** — Lists all mis-matched nets.

- **Stop** — Cancel the simulation.

NOTE	If 30 seconds pass and you have not made a choice, by default, the simulation continues.

3. Choose **More Information** to investigate mis-matched nets. The information lets you see whether it is a special design or a defective design. You can then decide whether or not to proceed with the simulation.
4. To view the results in each selection., select

   View > Export Results

Chapter 3

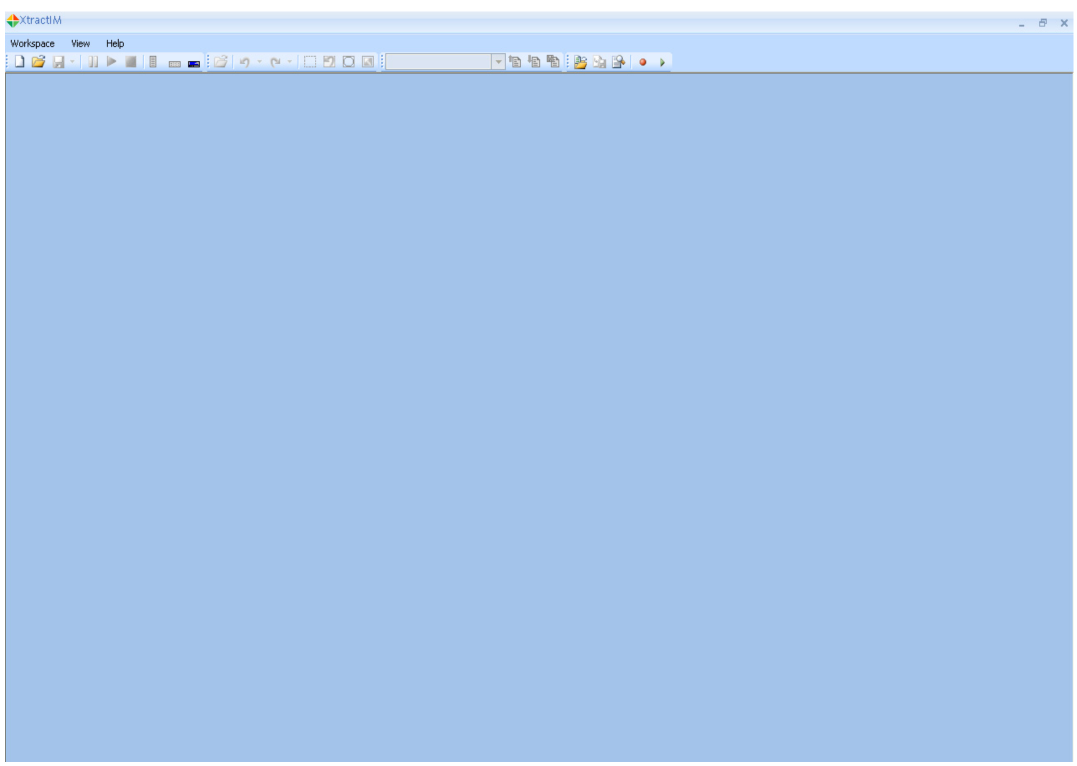
Learning the Workspace

This section describes how to use the Workspace.

XTRACTIM WORKSPACE

When you launch XtractIM for the first time, the **Main Window** opens. From this window, you can create a new workspace. Select

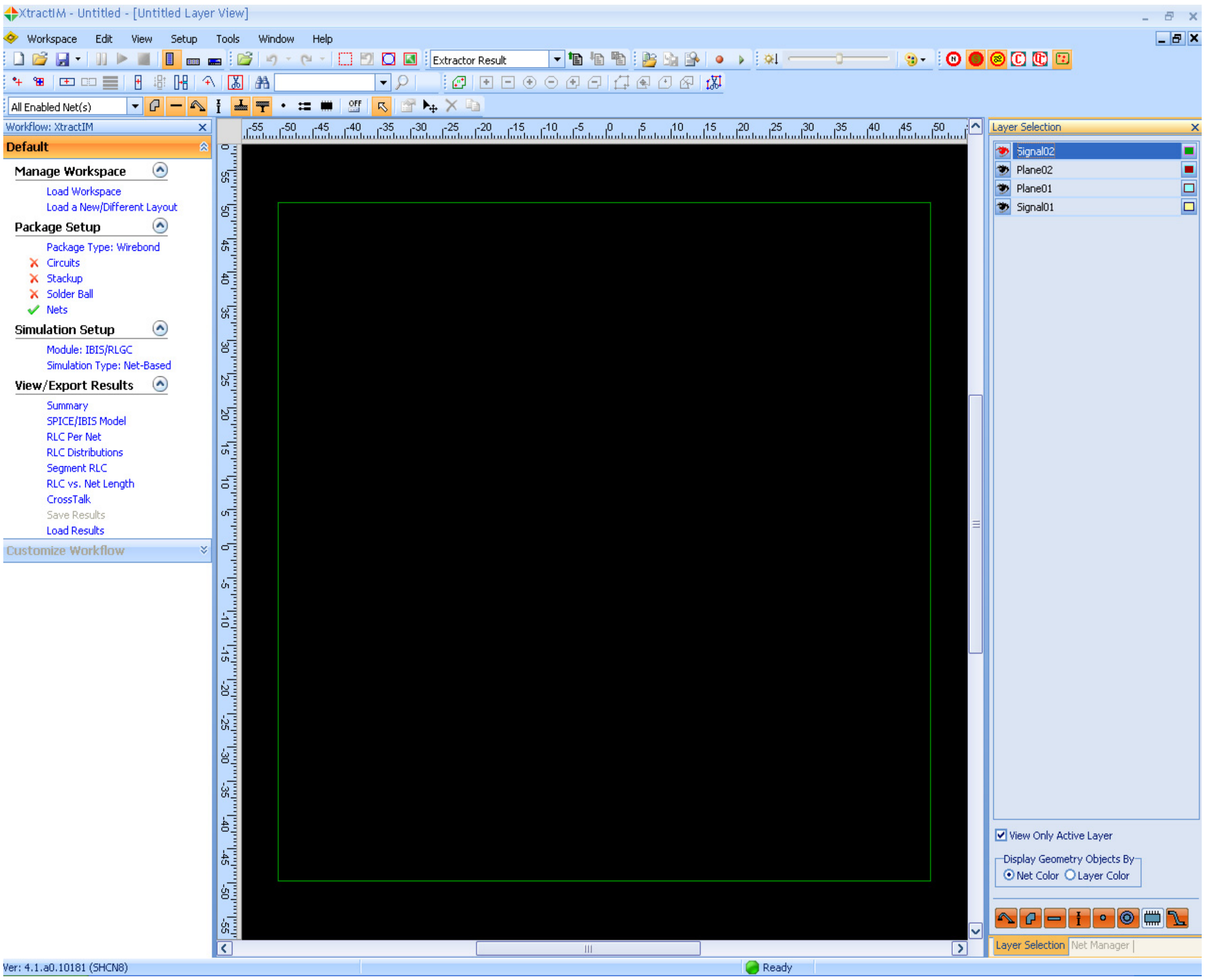
Workspace > New



New Workspace

The new workspace is made up of three major areas:

- **Workflow pane** — Left side of the screen.
- **Layout Area** — Large blank area on the right side of the screen
- **Layer Selection and Net Manager Pane** — Right side of the screen.

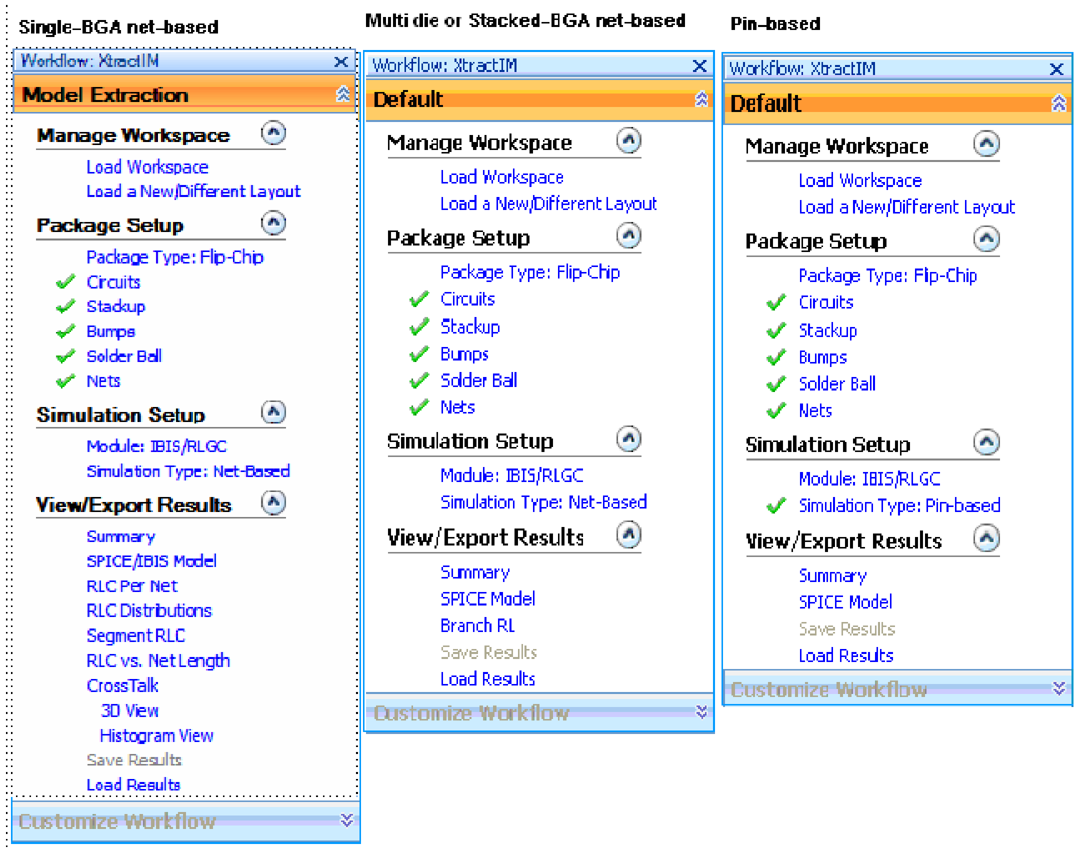


Workflow Pane

All Workflow tasks are listed in the Workflow pane. From left to right, the samples show the workflow for Single-BGA net-based, Stacked-BGA net-based, and pin-based extraction, respectively.

Click on the tasks to expand or collapse them. When a task is expanded, details associated with that task appear in an Editor pane, across the bottom of the screen.

When you move the mouse onto a task, a tool-tip appears and provides associated information.



Editor Pane

When you click on a task, the corresponding detail information of the task is displayed in the **Editor** pane (the horizontal section along the bottom of the screen).

1. Input information into the pane.
2. Highlight an item listed in the Editor pane.
3. View the item in the Layer View window.

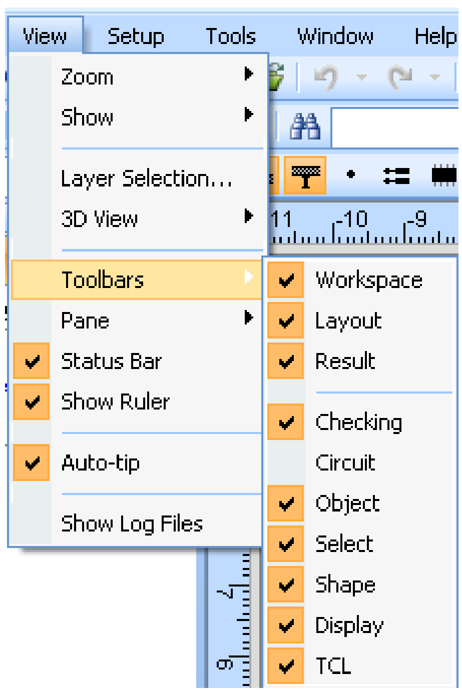
The Menu Toolbars

1. To see the all the toolbars available to you, select:

   View > Toolbars

2. Use the Status Bar to view:
   - Current X, Y coordinates of the cursor
   - Simulation progress
   - Version information

3. Use the commands on the pull-down menus.
   - Check results
   - Modify a design
   - Report results
   - Run the simulation
   - Setup installation

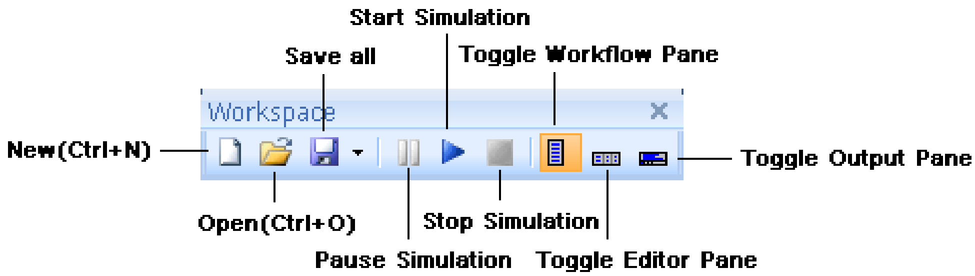


Note	Once a tool is selected, it remains in use until you select another tool. Right-click to deselect the tool and return to non-drawing mode.

Workspace Toolbar

The Workspace Toolbar provides quick access to common XtractIM commands.

Use this easy access to perform some of the more basic functions of XtractIM.



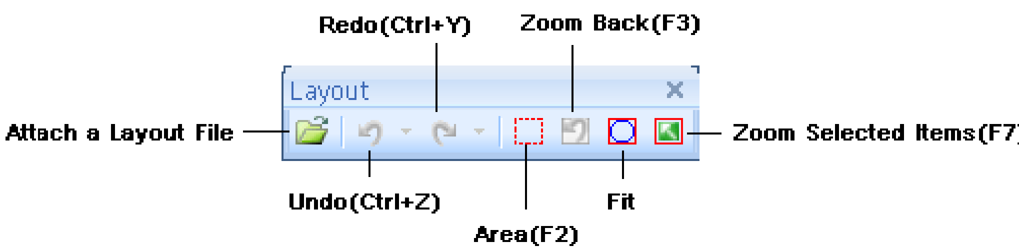
Layout Toolbar

The Layout Toolbar also allows you to perform some of the more basic functions of XtractIM.

Undo and Redo Buttons

You can undo or redo any action that you have performed for package editing.

The Undo and Redo buttons allow you to choose from the last few actions you have performed.



Zoom Functions

Use the zoom functions to view various parts of the package.

1. Select **Area** to display a magnified view of a rectangular area selected by mouse dragging.
2. **Zoom in** to a selected area.
3. **Zoom-out** to display the window contents in reduced size.
4. Select **Fit** to display the entire curve graph or package in the window.

TIP	You can use two hot keys for the zoom-in and zoom-out function: F2 for area zoom in; F3 for zoom-out.

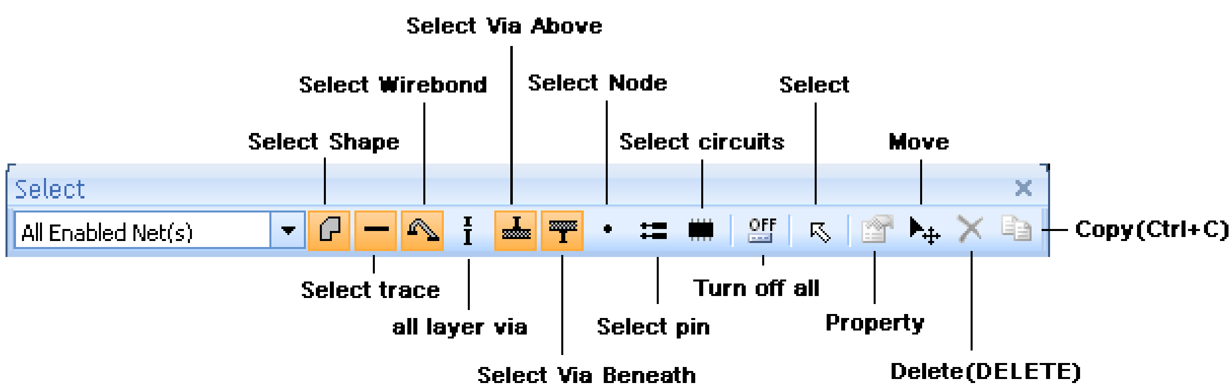
The Select Toolbar

At times, the object you want to select for a procedure is so close to another object on a layer that it is difficult to select the object you want. A special toolbar exists to help you select specific objects.

Select an Object

1. Click on the button for the type of objects you want to select.
2. Select an operation button.

- **Delete** — Move the cursor to the objects of interest. Left-click. Hold and drag to select an object or objects. Click the **Delete** key to remove objects.
- **Move** — Move the cursor to the objects of interest. Left-click. Selected objects move.
- **Property** — Move the cursor to the object of interest. Left-click to select an object. Click on the **Property** button to see the **Property Report** for the object.
- **Select** — Move the cursor to the objects of interest. Left-click. Hold and drag to select objects.
- **Unselect** — Hold down the CTRL key. Click on the selected object.

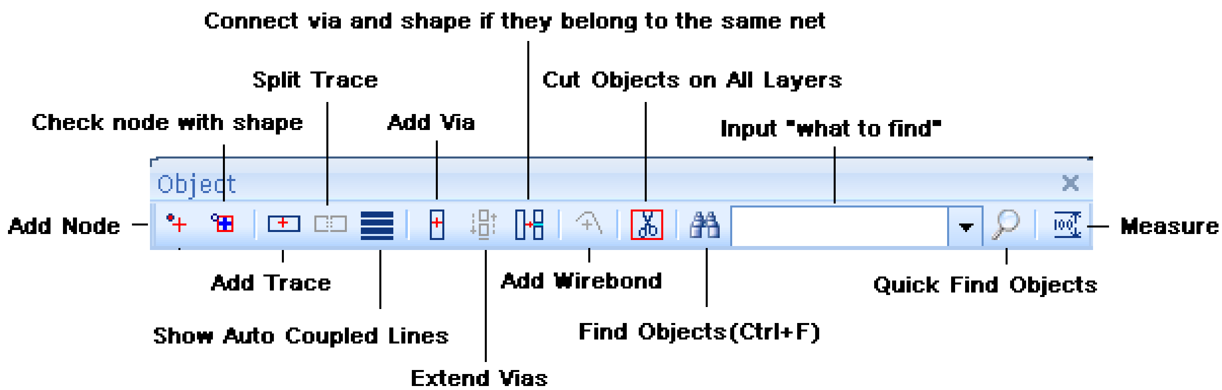


The Object Toolbar

Use the Object Toolbar to add or cut package objects (vias, shape vertices and Traces).

View the different areas of this toolbar.

These buttons provide quick access to the tasks you will frequently perform.



- **Cut Objects** — Cut out objects on all layers in an area that you specify. This function cuts all objects including: nodes, vias, Traces, shapes, and pads.
- **Node Tools** — Add a node to the package.
- **Trace Operations** — Add or split a Trace and setup a current observation.
- **Via Operations** — Add, copy, or extend vias.

Cut Area Rules

When cutting an area, the following rules apply:

- Objects are cut, regardless if the object's net is enabled or disabled.
- If a node is used in a circuit link, the node is unlinked prior to being cut.

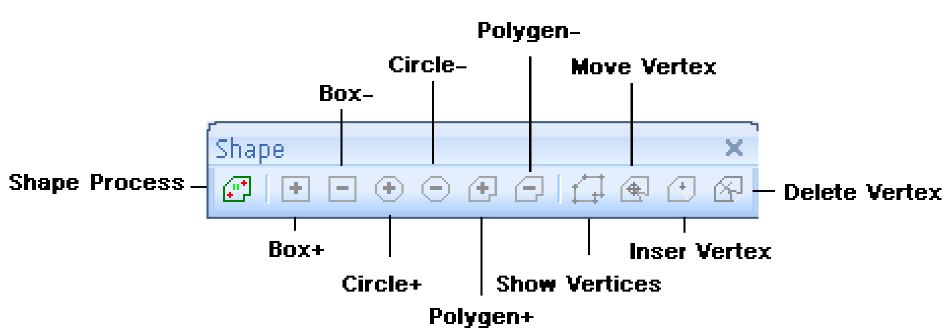
Shape Toolbar

Use the Shape Toolbar to draw and work with shapes.

Three kinds of shape tools are provided with both add and cut features:

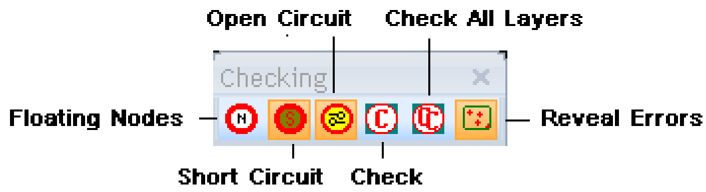
- Box
- Circle
- Polygon

The shape tools can be applied to plane layers or patches on signal layers.



Error Checking Toolbar

Use the Error Checking Toolbar to find short circuit warnings prior to running simulations.



Chapter 4

Working with SPD Layout

For SPD layout settings, please refer to the common document **SPD Layout UG**. It introduces the common GUI capabilities and operations of Sigrity analysis tools.

Chapter 5

XtractIM Simulation of a Single BGA Package

This chapter takes you through the steps to use the XtractIM tool in the simulation of a single BGA (Board Grid Array) package.

About XtractIM

XtractIM extracts the most common electrical models of IC packages according to IBIS (I/O Buffer Information Specification) as well as SPICE netlist of electrical models.

These models can be used for system-level analysis including drivers, receivers and interconnects; as well as for assessing the electrical performance of IC packages. XtractIM functionality provides the user with capability to:

- Generate IBIS package pin RLC model.
- Generate IBIS package RLC matrix model with coupling between signal, power and ground nets.
- Generate net length, DC_R, delay of each signal net.
- Generate SPICE equivalent circuits of package RLGC models of different topologies (Pi or T), including coupling between signal, power and ground nets.
- 2D and 3D display of RLC curves and distributions, including coupling between nets.

XtractIM can handle both flip-chip packages and wirebond packages with 3D bonding wire profiles. XtractIM handles both single and stacked BGA packages.

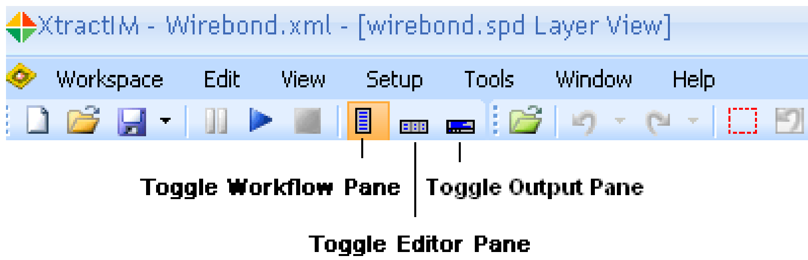
It can extract models of full packages or selected nets of a package. The interface is compatible with data files in various formats, including UPD (Unified Package Designer), MCM, .brd, .sip, NA2, DSN and SPD.

Related Topics

- ***The Workflow Pane***
- ***Using the Workflow Pane***
- ***Save a Workspace***

Toolbar Icons

- **Toggle Workflow pane** — Workflow pane appears or hides.
- **Toggle Edit pane** — Status Bar appears or hides.
- **Toggle Output Pane** — Output Pane appears or hides.



SIMULATION SETUP

A typical workflow in Interaction mode includes the following steps.

- Create a new workspace file or load an existing file (.ximx file).
- Open a layout file (.spd file).
- Select a package type: wirebond or flip-chip, single BGA or stacked BGA.
- Setup the circuits: select / deselect Die-circuit and Board circuit.
- Setup the Stackup: set parameters for the C4 Bump/Solderball medium layer.
- Set the Bump data if it is a flip-chip package.
- Set the Solder Ball data.
- Select the nets for extraction.
- Setup extraction frequency and capacitance or inductance output control.

Setup the Package Simulation

1. Launch XtractIM.

   Two icons are available: **New**  and **Open**  .

   The **New** icon creates a new workspace.

   The **Open** icon allows users to load an existing workspace file.

2. To create a new workspace click on the **New** icon;

   or select

   Workspace > New

3. To load the Package Structure, click on

   Load a New/Different Layout

Related Topic

- ***Working on a Layout File***

Select Package Type

1. Select a Package Type.

   The default package type is Single Die, Single BGA, wirebond package.

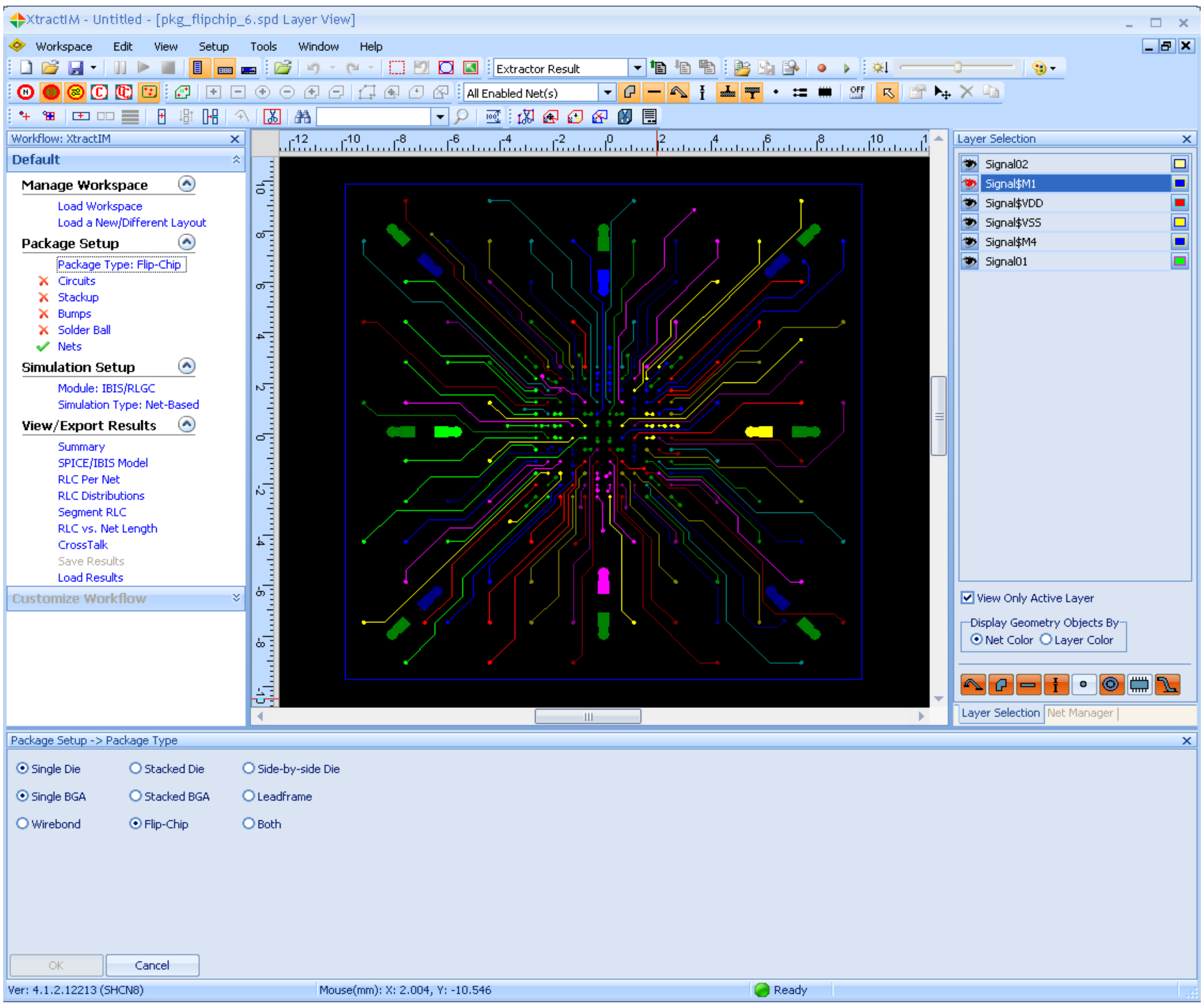
2. Click on

   Wirebond

   or

   Flip-chip

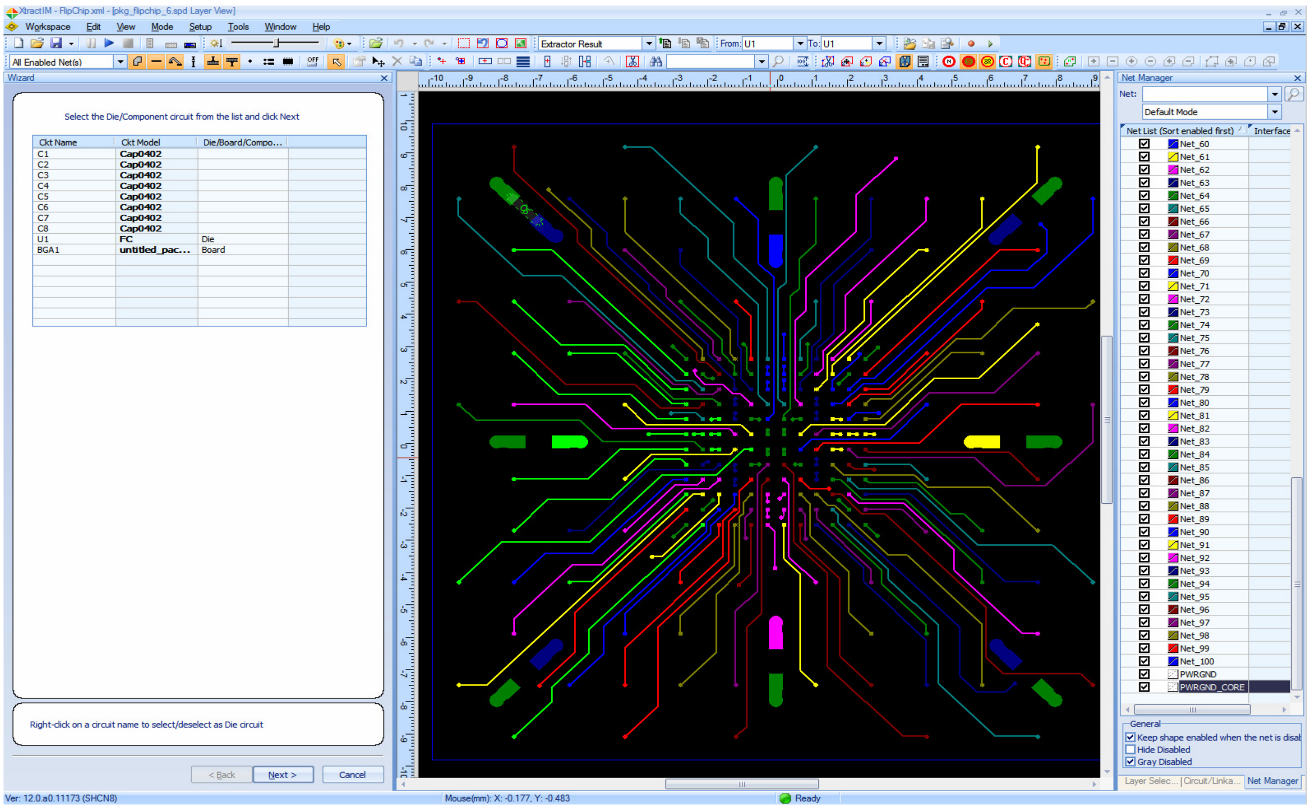
   Our example shows the Flip-chip selected.



3. Click **OK** to save your selection.
4. Click **Cancel** if you want to change your selection, start over and cancel your session.

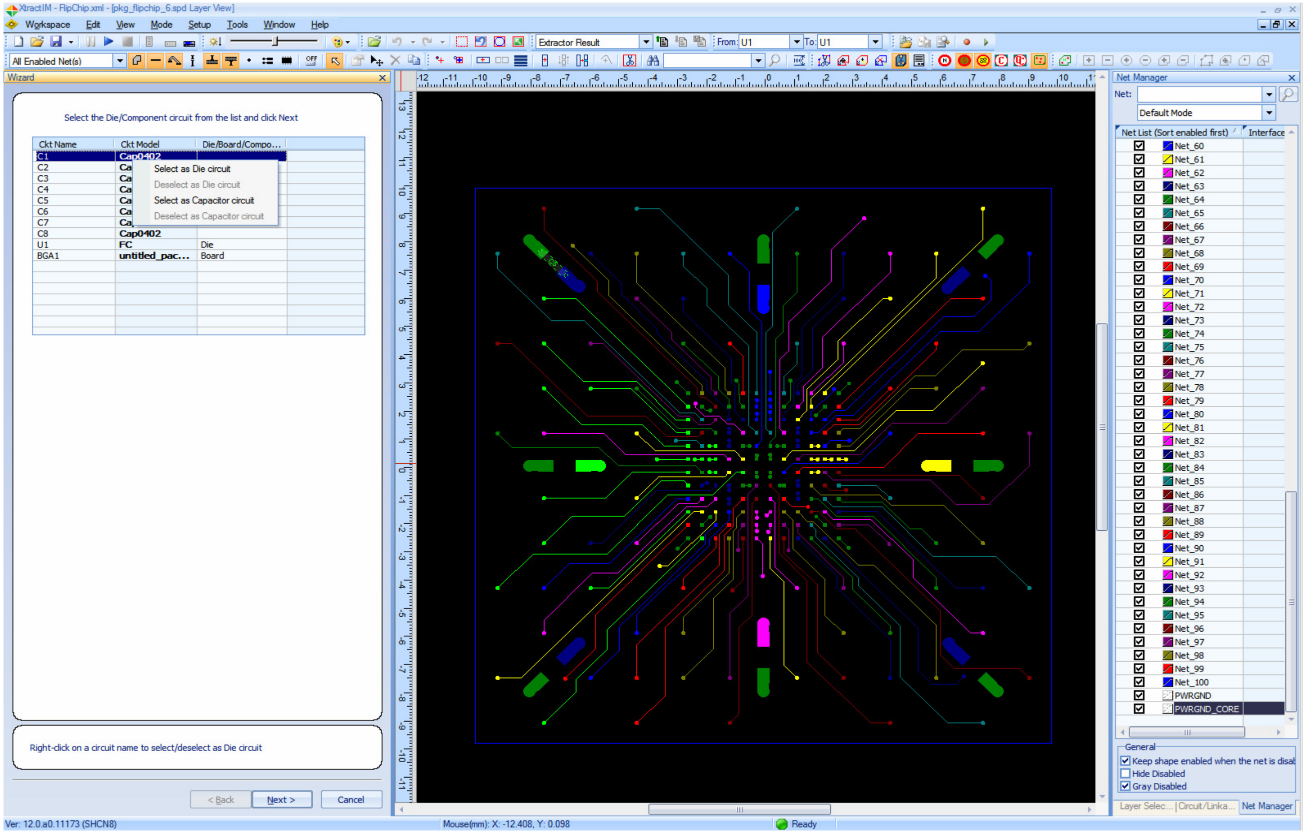
Setup Circuits

1. Click on **Circuits** in the Workflow pane to setup the Circuit data for a Flip-Chip package. A new pane opens up in the left side of the workspace.

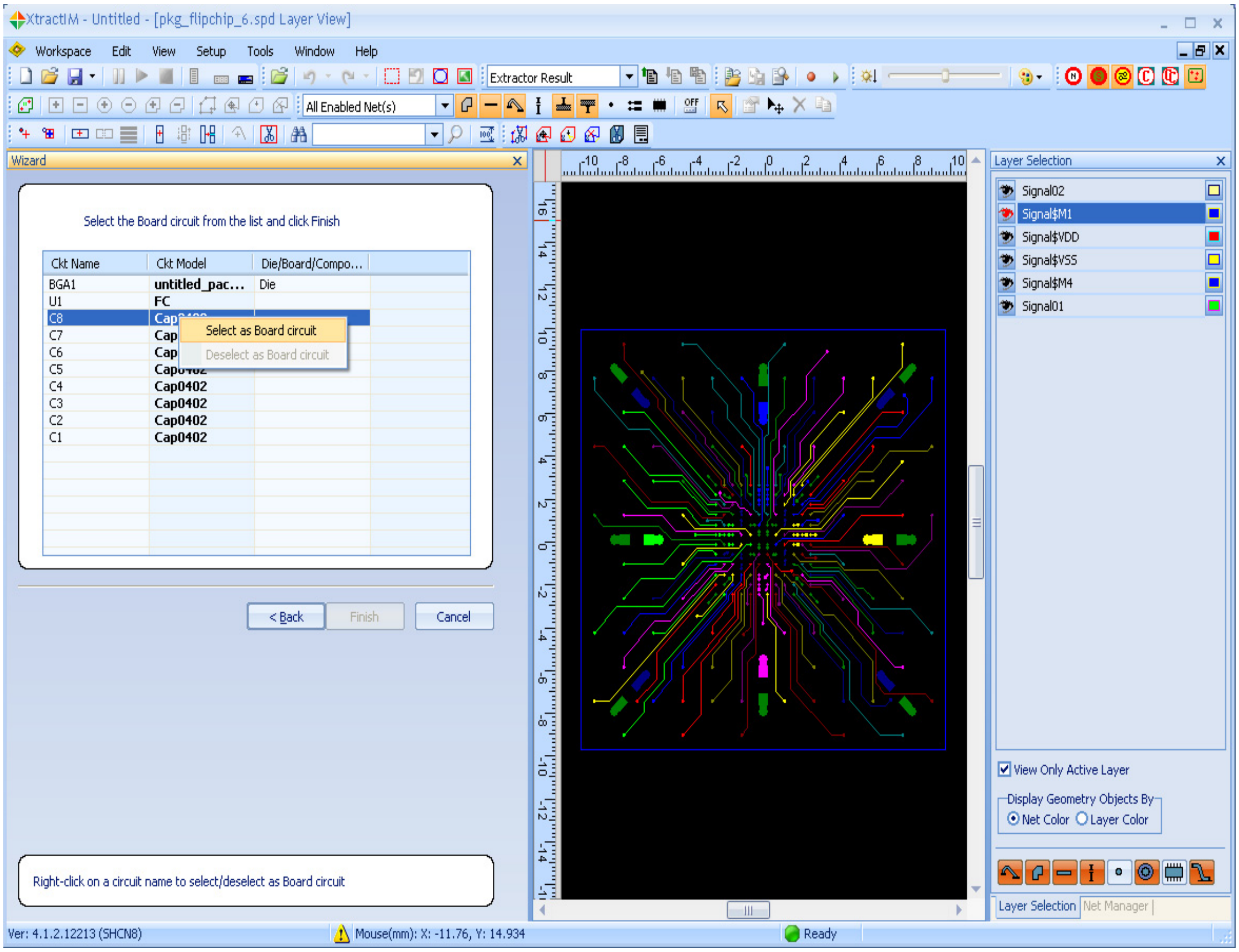


2. Right-click on the desired circuit.

3. Select it as a **Die** circuit (or a Capacitor circuit).



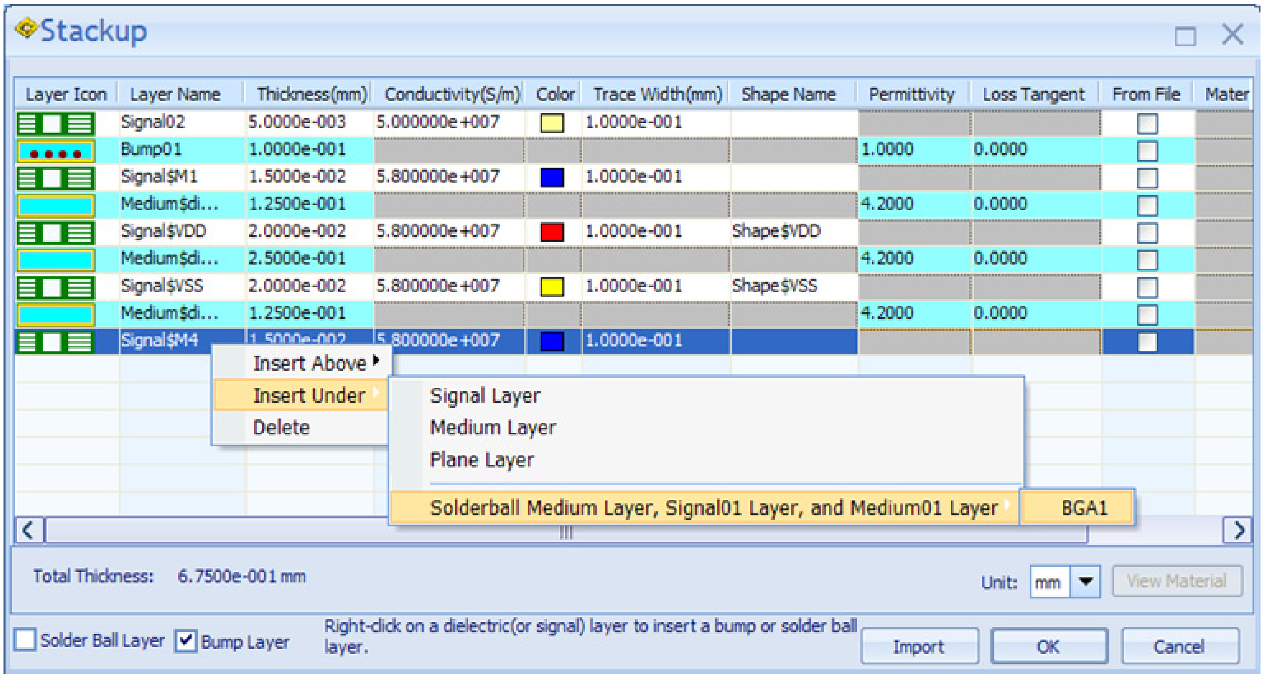
4. Click **Next**.
5. Right-click on another desired circuit.
6. Select it as a **Board** circuit.



7. Click **Finish** to finish the setup.

Setup Stackup

1. Click on **Stackup**. The Stackup window opens.
2. Right-click on the bottom signal layer. You can insert layers above or under.



You can insert:

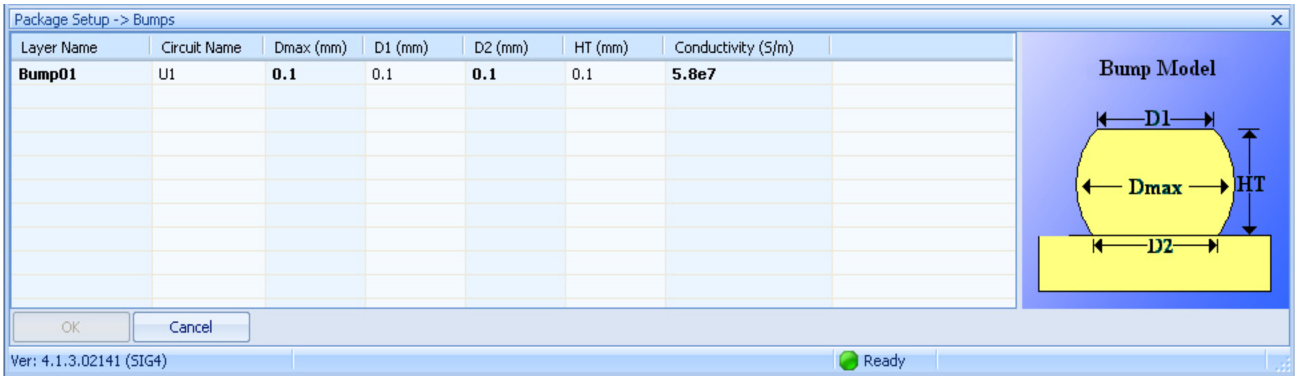
- Solder Ball Medium Layer
- Empty Signal Layer
- Medium Layer standing for a PCB Medium Layer

All layers are inserted under the bottom signal layer as shown in the example below. The added signal layer is the end of the solder ball.

Setup Bump

The example shows the setup for a Flip-chip package.

1. Click on **Bumps** in the Workflow pane. A new window opens up in the Editor pane.



2. Input the settings for the Bumps.

   Maximum Diameter: Dmax (mm)

   D1 (mm)

   D2 (mm)

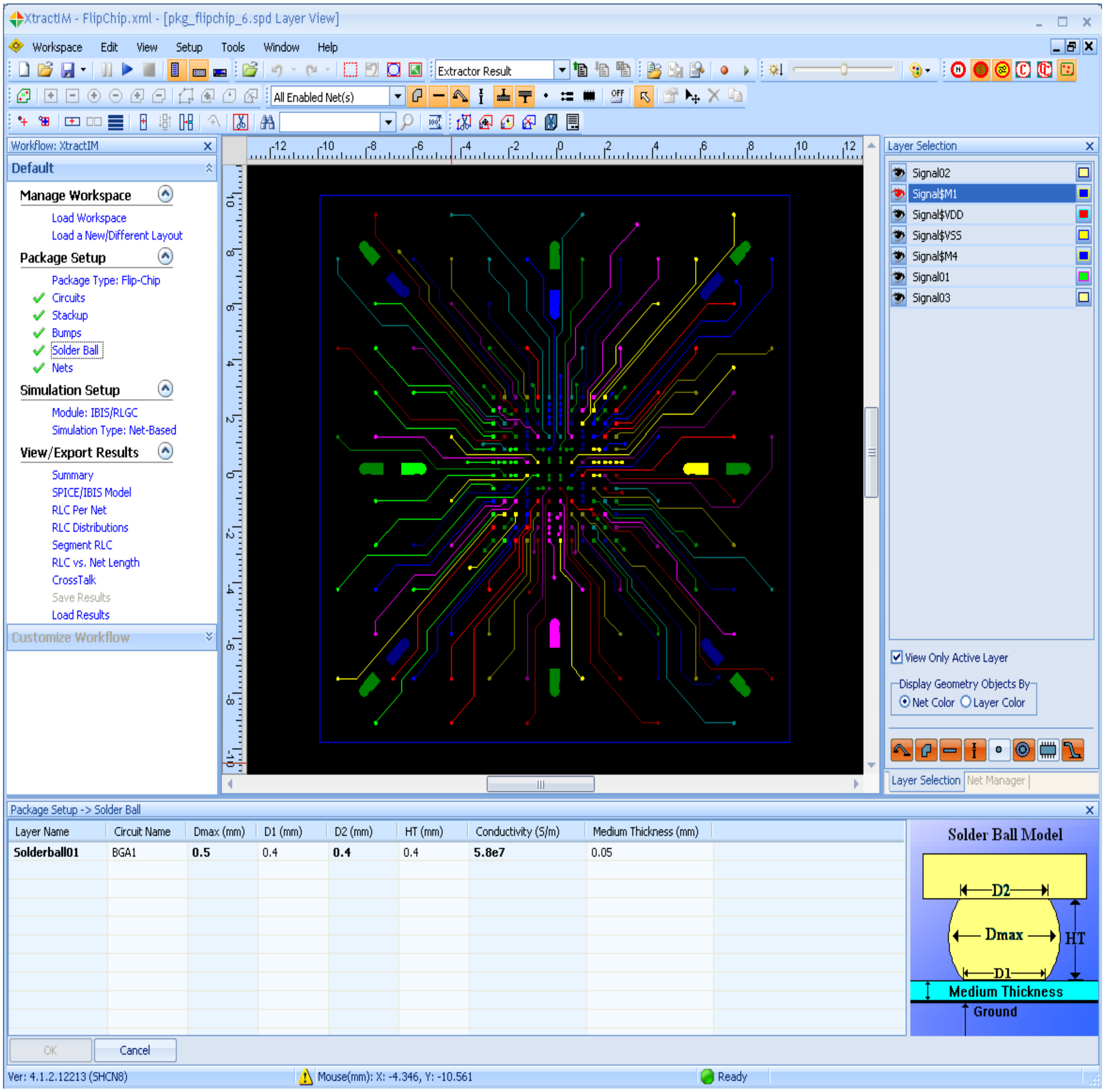
   Height: HT (mm)

   Conductivity (S/m)

3. Click **OK** to save your entries or click **Cancel** if you do not want to save your changes.

Setup Flip-chip Package

1. To setup the Solder Ball data for a Flip-Chip package, click Solder Ball in the Workflow pane under Package Setup, A new pane opens up in the bottom portion of the window.



2. Input the settings for the C4 Bumps.

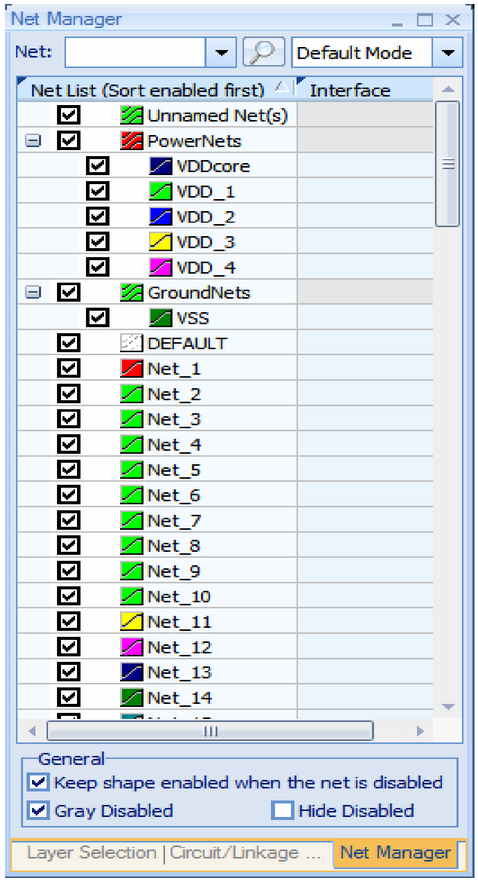
   Maximum Diameter: Dmax (mm)

   D1 (mm)
   D2 (mm)
   Height: HT (mm)
   Conductivity (S/m)

3. Click **OK** to save your entries or **Cancel** if you do not want to save your changes.

Setup Nets

1. Click on **Nets** in the Workflow window. The **Net Manager** window opens.



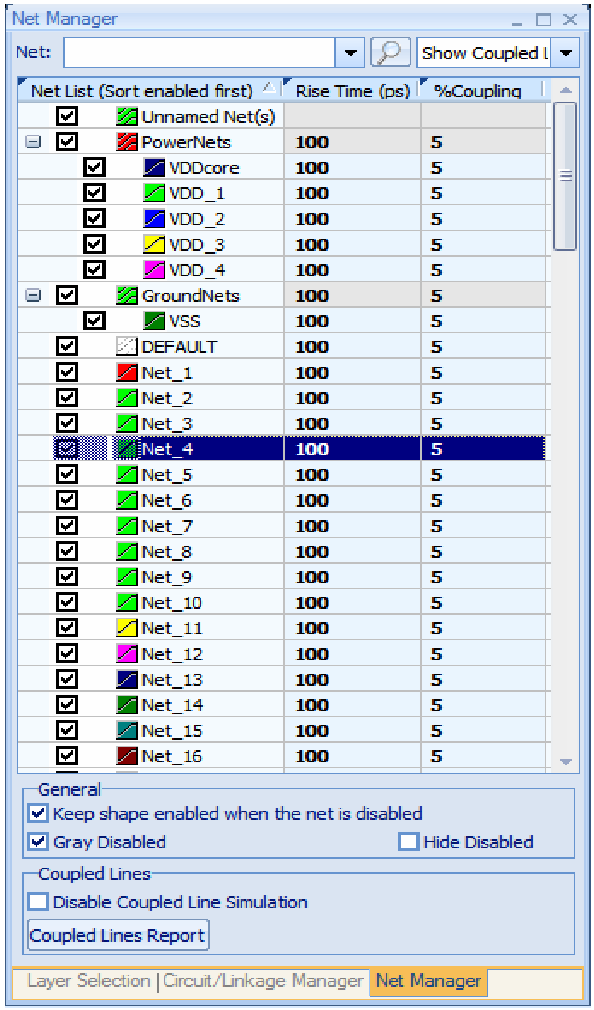
2. Choose any desired nets for RLC extraction.

   You can also move the signal net into and out of PowerNets and Ground Nets.

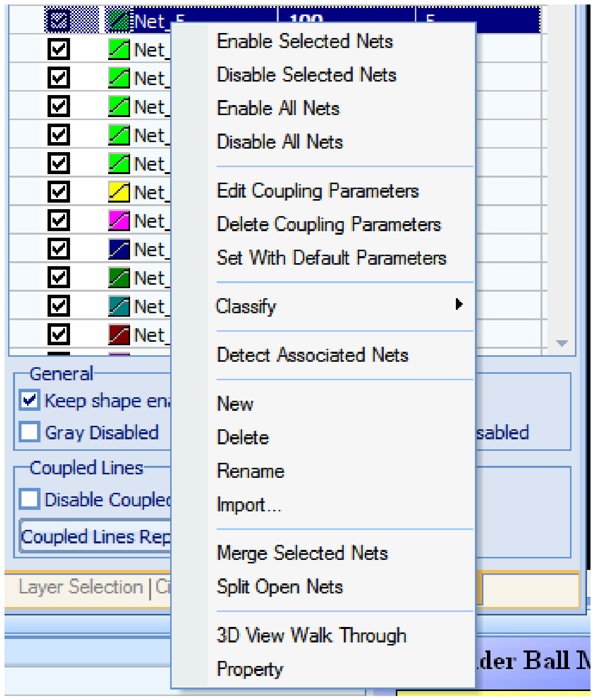
   - At least one Ground Net must be selected to act as a reference ground net.
   - Only choose the desired Ground Net as the reference ground net.

3. To set up ***Extraction Frequency and Capacitance/Inductance Output Control*** for identfying coupled Trace, click

   Auto Coupled Line



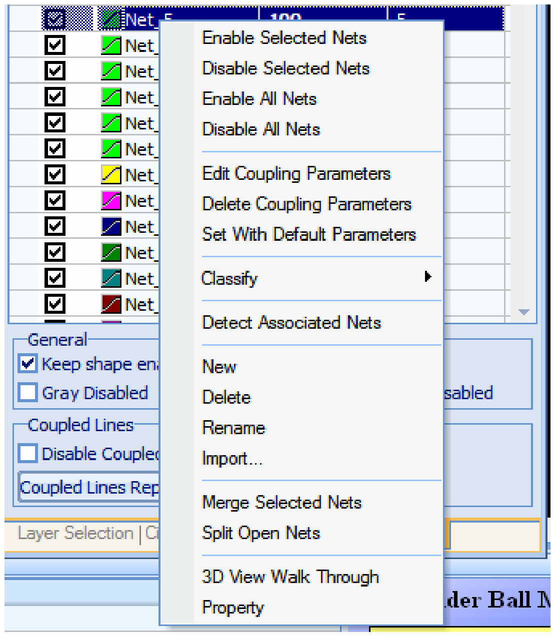
4. Select the nets you wish to edit.
5. Right-click to open the pop-menu.


Enable Selected Nets
Disable Selected Nets
Enable All Nets
Disable All Nets
Edit Coupling Parameters
Delete Coupling Parameters
Set With Default Parameters
Classify
Detect Associated Nets
New
Delete
Rename
Import...
Merge Selected Nets
Split Open Nets
3D View Walk Through
Property
General
Gray Disabled
Coupled Lines

Set With Default Parameters

1. Select the net to be edited.
2. Right-click

   A pop-up menu opens.



3. Select

   Set With Default Parameters

Rise Time and % Coupling

When Traces are identified as coupled lines, the crosstalk between these lines are calculated during the simulation.

Coupled lines are treated as multi-conductor transmission lines, whereas an isolated Trace is modeled by the single transmission line algorithm. Coupled lines can be selected after the relevant Traces have been placed.

- **Rise Time Value** — Must be greater than 0. Default value is 200 ps.
- **%Coupling Value** — Must be 0 < value < 100. Default value is 5%.

NOTE!	If the coupling parameters—%Coupling and Rise Time—are left blank, the trace-to-trace coupling is not calculated during simulation.

Based on electrical threshold parameters, Traces belonging to several nets are automatically identified and analyzed as coupled transmission line sections.

Two Traces are said to be coupled if their reverse crosstalk exceeds the %Coupling.

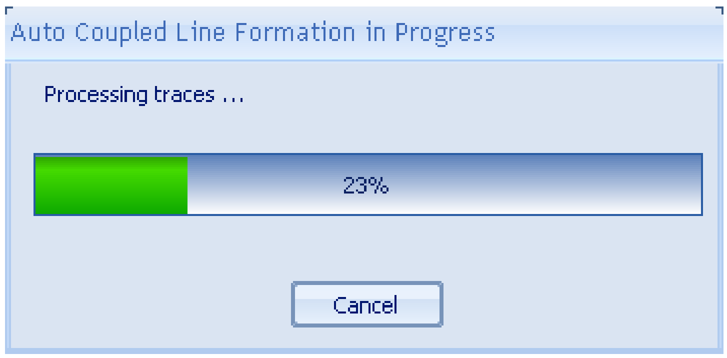
For a given Rise Time, the accumulated coupled section lengths between Trace nets should be long enough for forward crosstalk to exceed the %Coupling.

Show Coupled Lines

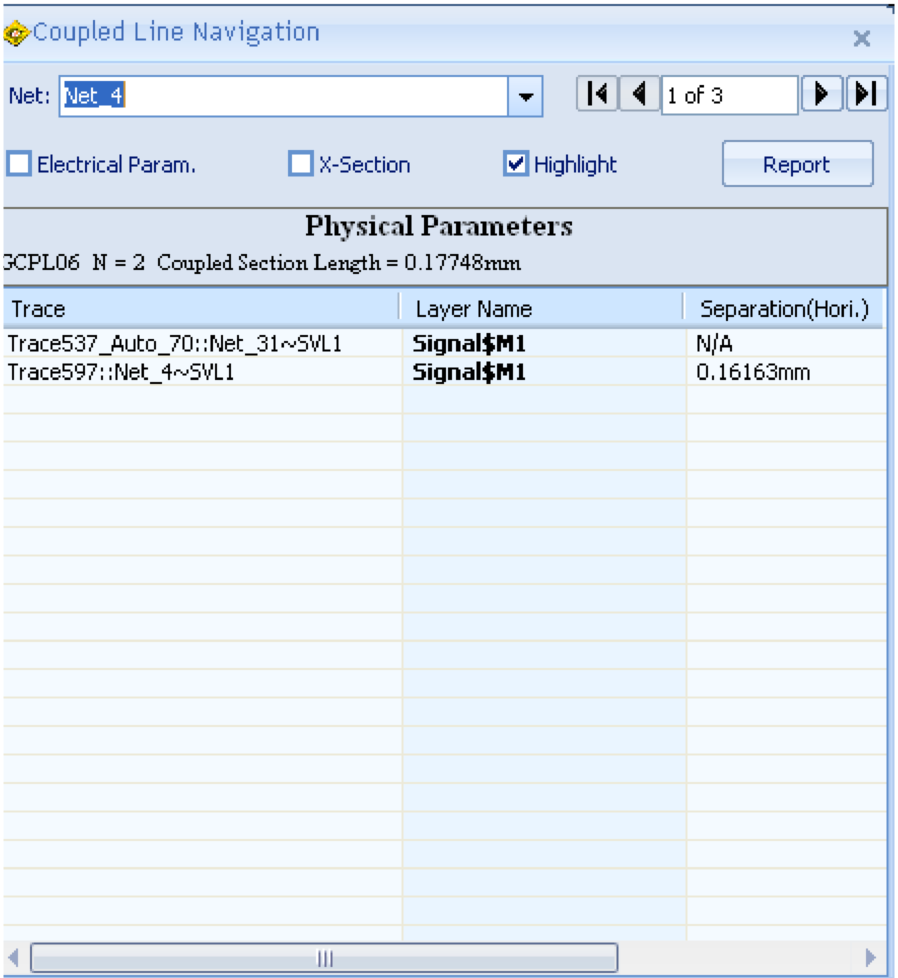
1. Select

   Net Manager > Show coupled line > Coupled lines report

   A progress window appears to show you the progress.



2. The Trace identified as coupled lines is displayed as shown in the following example.



Extraction Frequency and Capacitance/Inductance Output Control

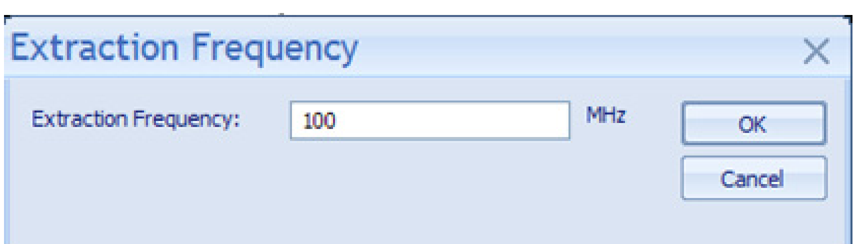
You can change the extraction frequency. The default value is 30MHz. Use the window shown in the exaple to change the default value.

Follow these steps:

1. Select

   Setup > Extraction Frequency

   The Extraction Frequency window opens.



2. Set frequency in the pop-up window.

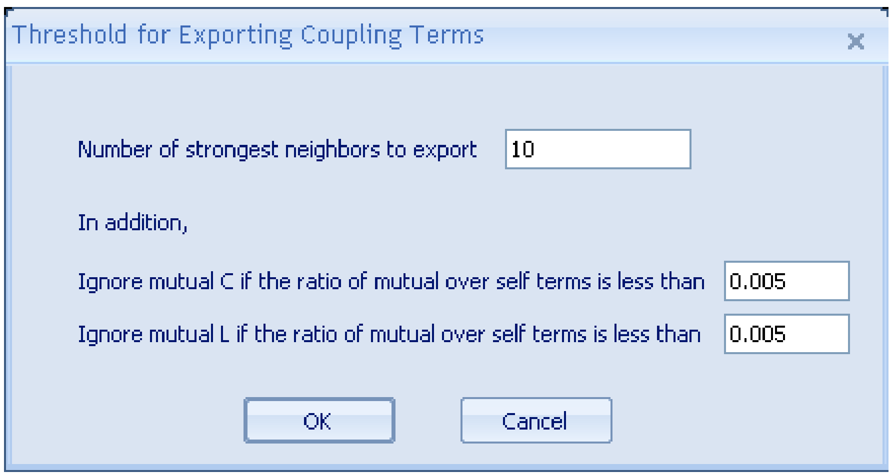
Set Threshold for Exporting Mutual Terms

XtractIM captures all the coupling during the extraction stage. It has options to reduce the size of the output circuit during the export stage.

1. Open

   Setup-> Threshold for Exporting Coupling Terms

   A pop-up window opens.



2. Enter the number of strongest coupling neighbors to be kept in the circuit model.

   The default of number of strongest coupling neighbors is 10; which means only outputting the 10 strongest neighbors (including self).

3. Ignore mutual capacitance or inductance if the ratio of mutual terms over self term is less than a percentage.

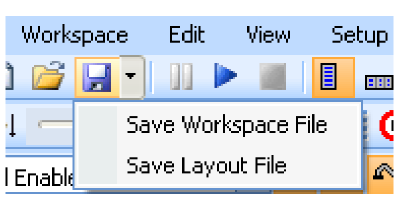
   The default percentage threshold for ignoring mutual capacitance or inductance is 0.005.

   If the mutual capacitance/inductance is less than the 0.5% of the minimum of the two self-capacitances/inductances,

   XtractIM will not output the mutual capacitance/inductance.

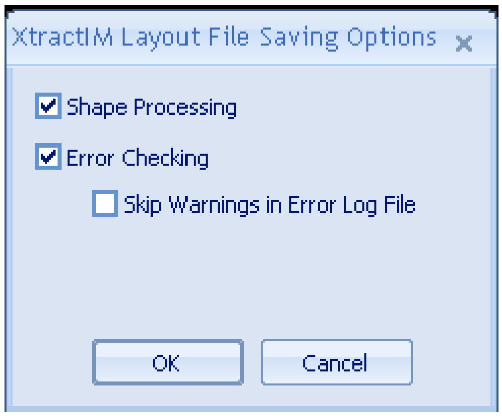
Save the Workspace and Layout File

On the Toolbar, click the next to the **Save** button , the drop-down list shows up. You can choose to save workspace file or layout file.



- Select **Save Workspace File**, the workspace file is saved.

- Select **Save Layout File**, or click the **Save** button  , the **XtractIM Layout File Saving Options** dialog opens.



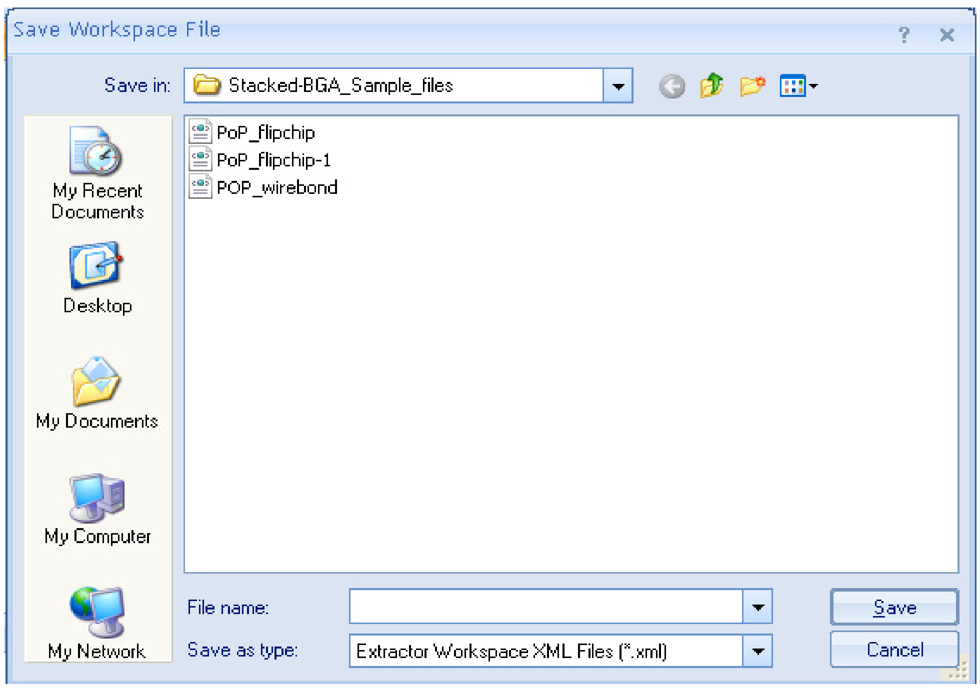
Using the Save as Option

The example below shows another way to save the workspace and layout file using the **Save as** option. Saving the workspace does not automatically save the .spd file. Similarly, saving the .spd file does not save the workspace file.

1. Select

   Workspace > Save As…

   The Save Workspace File window opens.



2. Enter a name.
3. Click Save.

Observe and Save Results

XtractIM calculates each net resistance, self loop inductance, conductance, self capacitance as well as its mutual loop inductance and mutual capacitance with other nets.

In the Inductance Matrix, the Diagonal Element is the Self Inductance of each net; the off-diagonal elements are mutual Inductance. The inductance and capacitance are matrices. For example, a simple group of four nets has the following inductance and capacitance matrix.

$$\begin{bmatrix} L_{11} & L_{12} & L_{13} & L_{14} \\ L_{21} & L_{22} & L_{23} & L_{24} \\ L_{31} & L_{32} & L_{33} & L_{34} \\ L_{41} & L_{42} & L_{43} & L_{44} \end{bmatrix} \qquad \begin{bmatrix} C_{11} & C_{12} & C_{13} & C_{14} \\ C_{21} & C_{22} & C_{23} & C_{24} \\ C_{31} & C_{32} & C_{33} & C_{34} \\ C_{41} & C_{42} & C_{43} & C_{44} \end{bmatrix}$$

Capacitance Matrix

The two concepts of capacitance matrix: Maxwell capacitance matrix and SPICE capacitance matrix.

- **Maxwell Capacitance Matrix** — Each diagonal element is the loading capacitance (i.e., capacitance to ground when other nets are grounded which represents the worst-case capacitive loading). Off-diagonal elements are mutual capacitance with negative values.
- **SPICE Capacitance Matrix** — Each diagonal element is capacitance to ground. Off-diagonal elements are mutual capacitance with positive values.

The relationship between Maxwell capacitance and SPICE capacitance matrix is shown here:

Capacitance Example

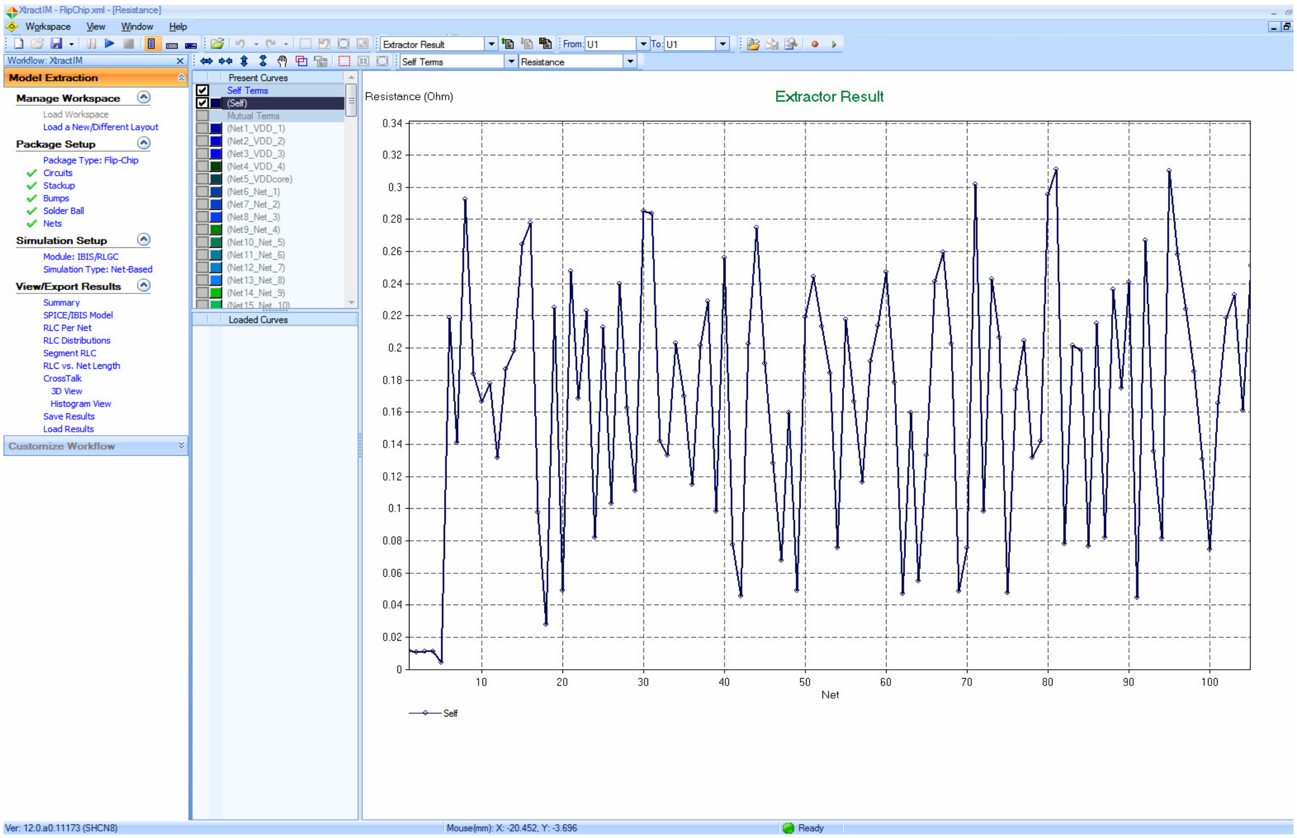
$$C_{ij}(SPICE) = -C_{ij}(Maxwell)$$
$$C_{ii}(Maxwell) = \sum_j C_{ij}(SPICE)$$
$$C_{ii}(SPICE) = \sum_j C_{ij}(Maxwell)$$

RLC Per Net View

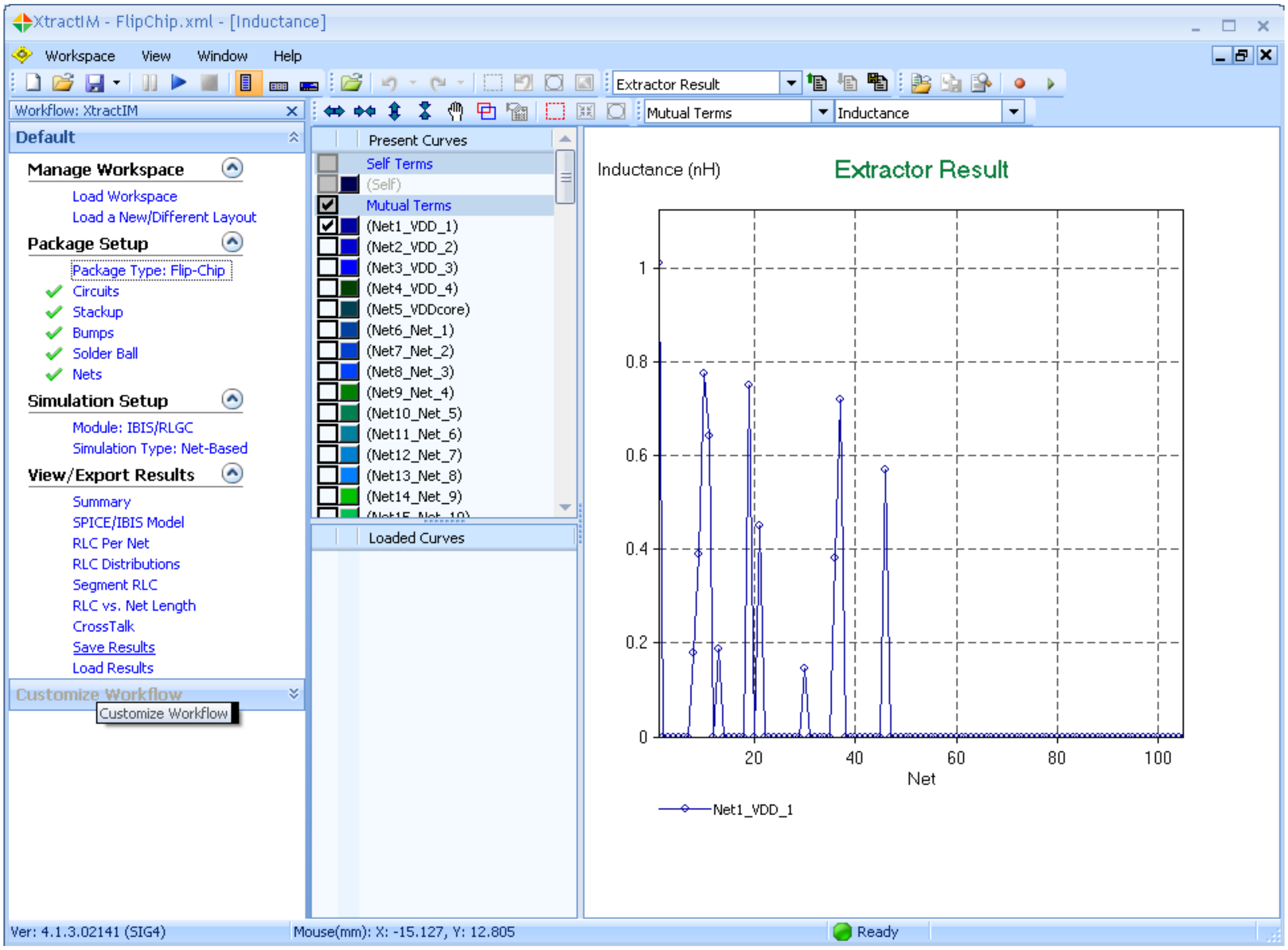
Choose to view resistance, self-inductance, self-capacitance or mutual for each net. Usually conductance is very low; so there is no view for conductance.

- **Mutual Term View** — Mutual inductance or SPICE mutual capacitance.
- **Self Term View** — Resistance, self-inductance or Maxwell diagonal capacitance.

Self Terms View



Mutual Terms View



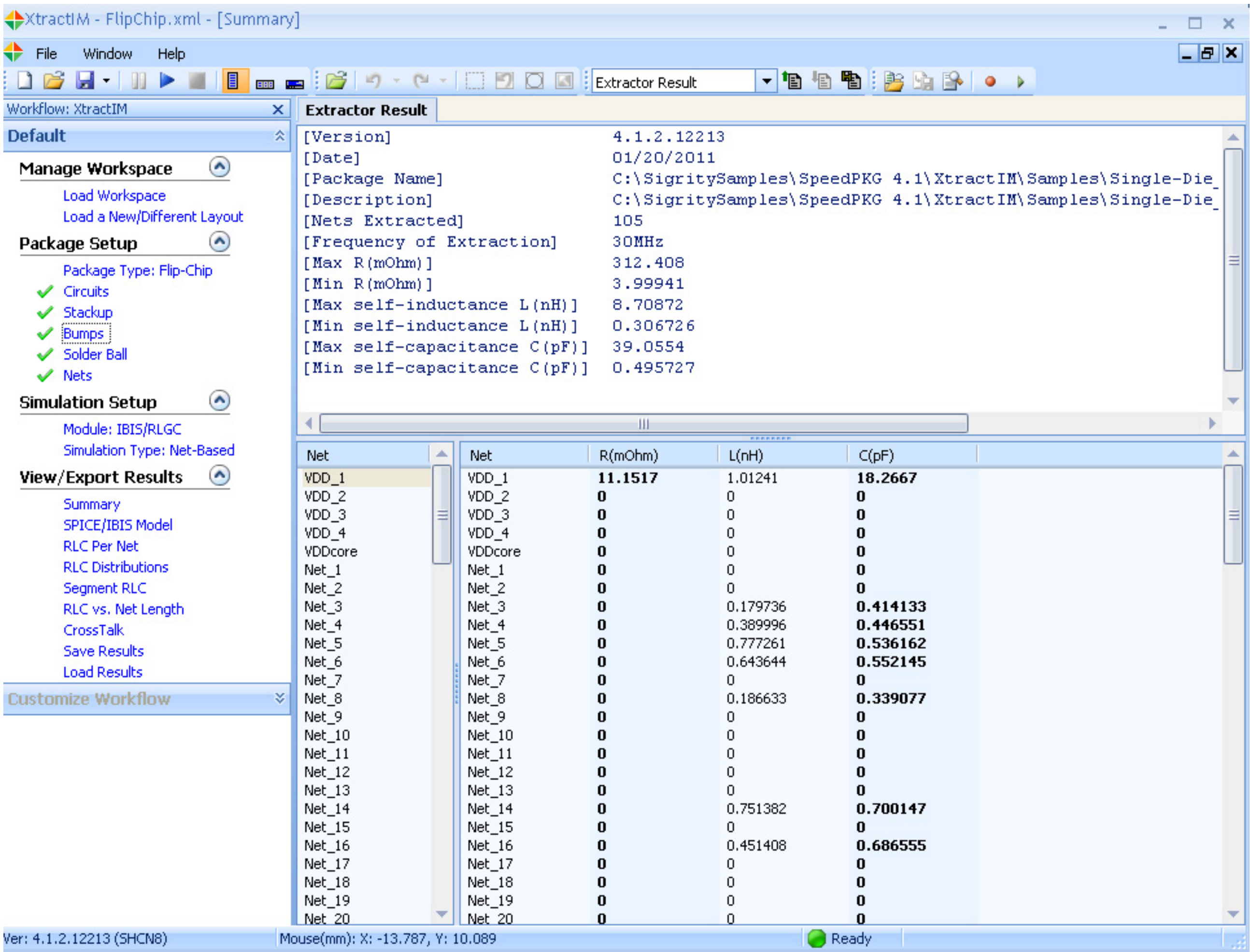
Summary of the Extracted Results

Click on **Summary** to open the summary and tabulated data for R, L and C.

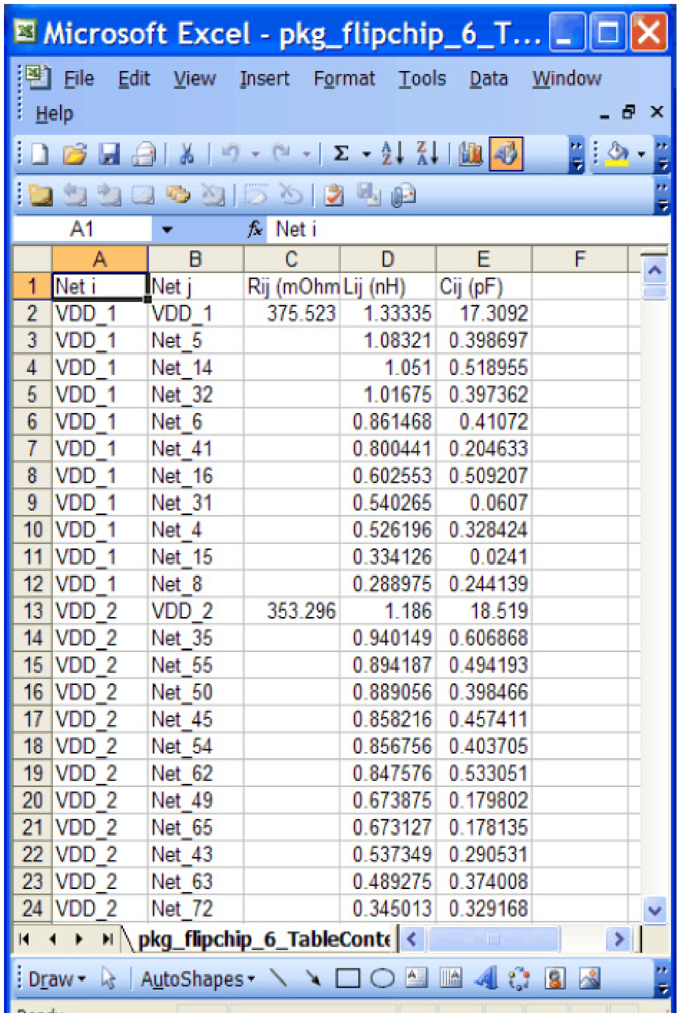
- **Bottom right window** — Displays a complete row of the R / L / C matrices when a certain net is chosen. You can also reorder the list.
- **Top right window** — Displays the overall results including package name, nets extracted, extraction frequency, maximum / minimum R, L, C and the full RLC matrix.

Click on **R / L / C** heading. The values are listed in increase or decrease order. The Table Content (RLC Full matrix) is automatically saved on hard disk in .csv format.

XtractIM Summary.



File Example



	A	B	C	D	E	F
1	Net i	Net j	Rij (mOhm	Lij (nH)	Cij (pF)	
2	VDD_1	VDD_1	375.523	1.33335	17.3092	
3	VDD_1	Net_5		1.08321	0.398697	
4	VDD_1	Net_14		1.051	0.518955	
5	VDD_1	Net_32		1.01675	0.397362	
6	VDD_1	Net_6		0.861468	0.41072	
7	VDD_1	Net_41		0.800441	0.204633	
8	VDD_1	Net_16		0.602553	0.509207	
9	VDD_1	Net_31		0.540265	0.0607	
10	VDD_1	Net_4		0.526196	0.328424	
11	VDD_1	Net_15		0.334126	0.0241	
12	VDD_1	Net_8		0.288975	0.244139	
13	VDD_2	VDD_2	353.296	1.186	18.519	
14	VDD_2	Net_35		0.940149	0.606868	
15	VDD_2	Net_55		0.894187	0.494193	
16	VDD_2	Net_50		0.889056	0.398466	
17	VDD_2	Net_45		0.858216	0.457411	
18	VDD_2	Net_54		0.856756	0.403705	
19	VDD_2	Net_62		0.847576	0.533051	
20	VDD_2	Net_49		0.673875	0.179802	
21	VDD_2	Net_65		0.673127	0.178135	
22	VDD_2	Net_43		0.537349	0.290531	
23	VDD_2	Net_63		0.489275	0.374008	
24	VDD_2	Net_72		0.345013	0.329168	

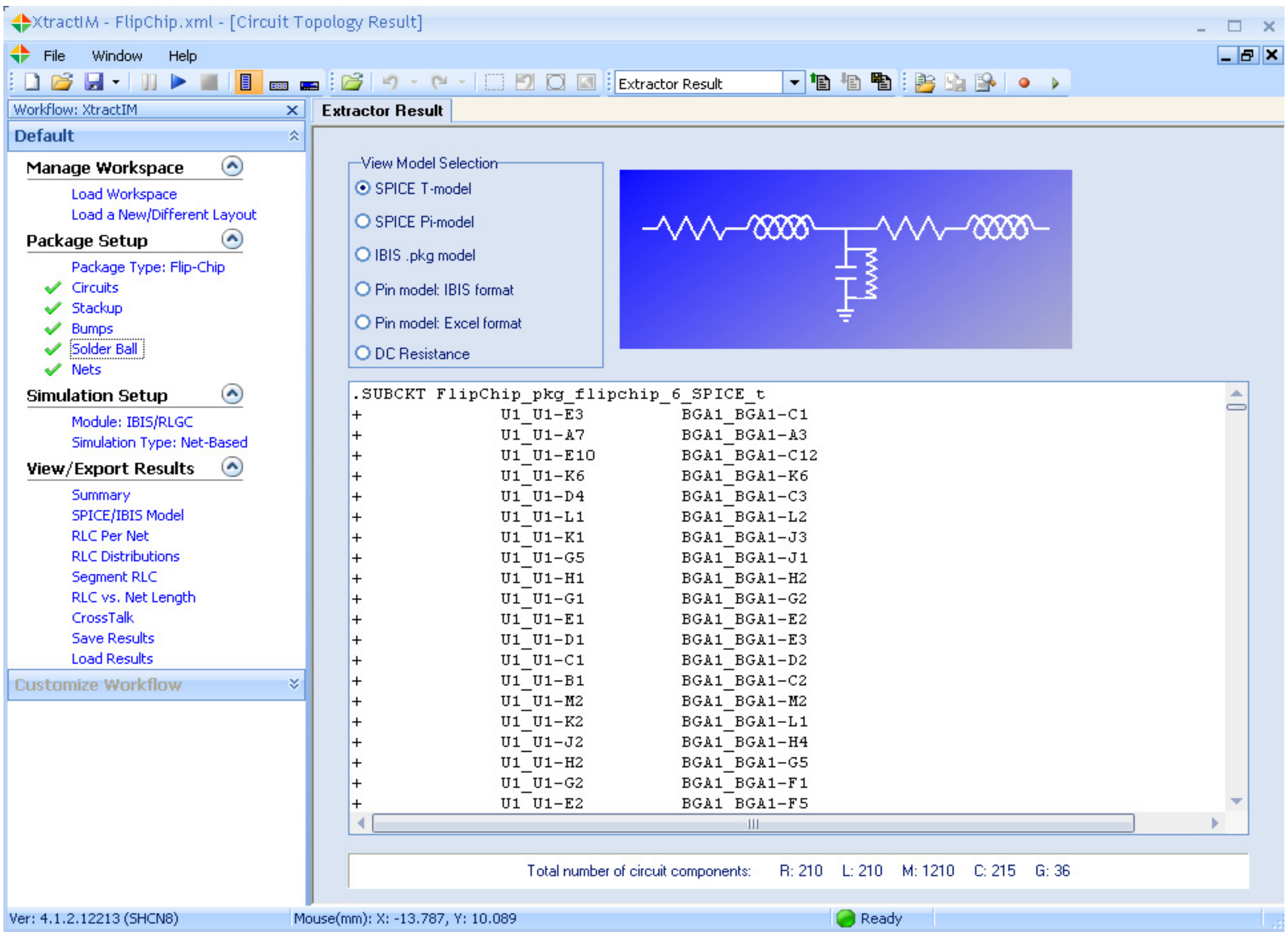
SPICE and IBIS Models

Upon completing the simulation both are in the same directory as the .spd file.

- SPICE Model is saved as a SPICE sub-circuit with the extension .ckt.
- IBIS Model is saved as an IBIS package model with the extension .pkg.

The total number of each element in the circuit is displayed along the bottom of the window.

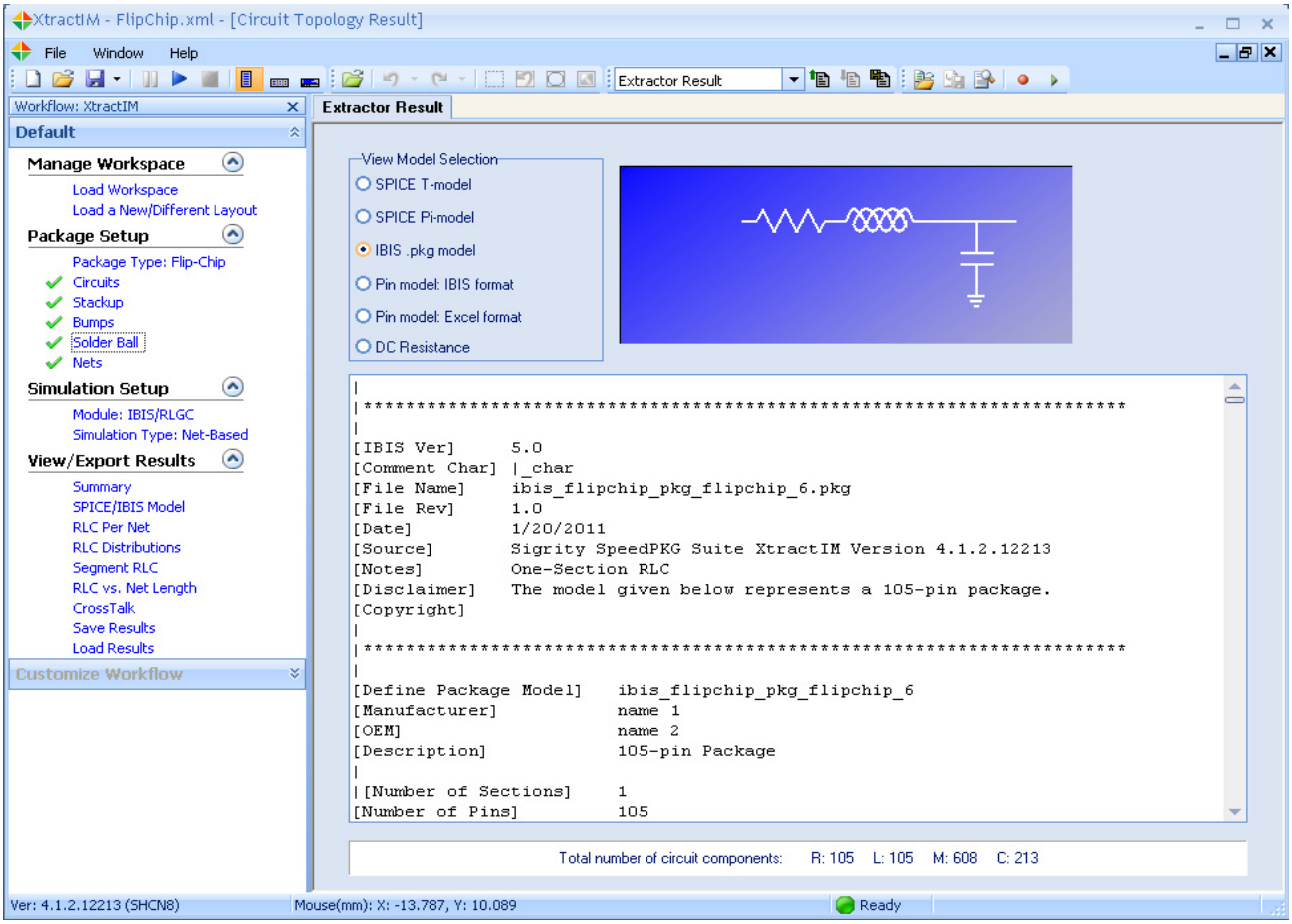
- R
- L
- M
- C
- G where M is the mutual inductance



SPICE / IBIS Model Result View

Below is the SPICE / IBIS Model result view.

- The SPICE model is a PI-circuit.
- The IBIS model is shown with coupling.



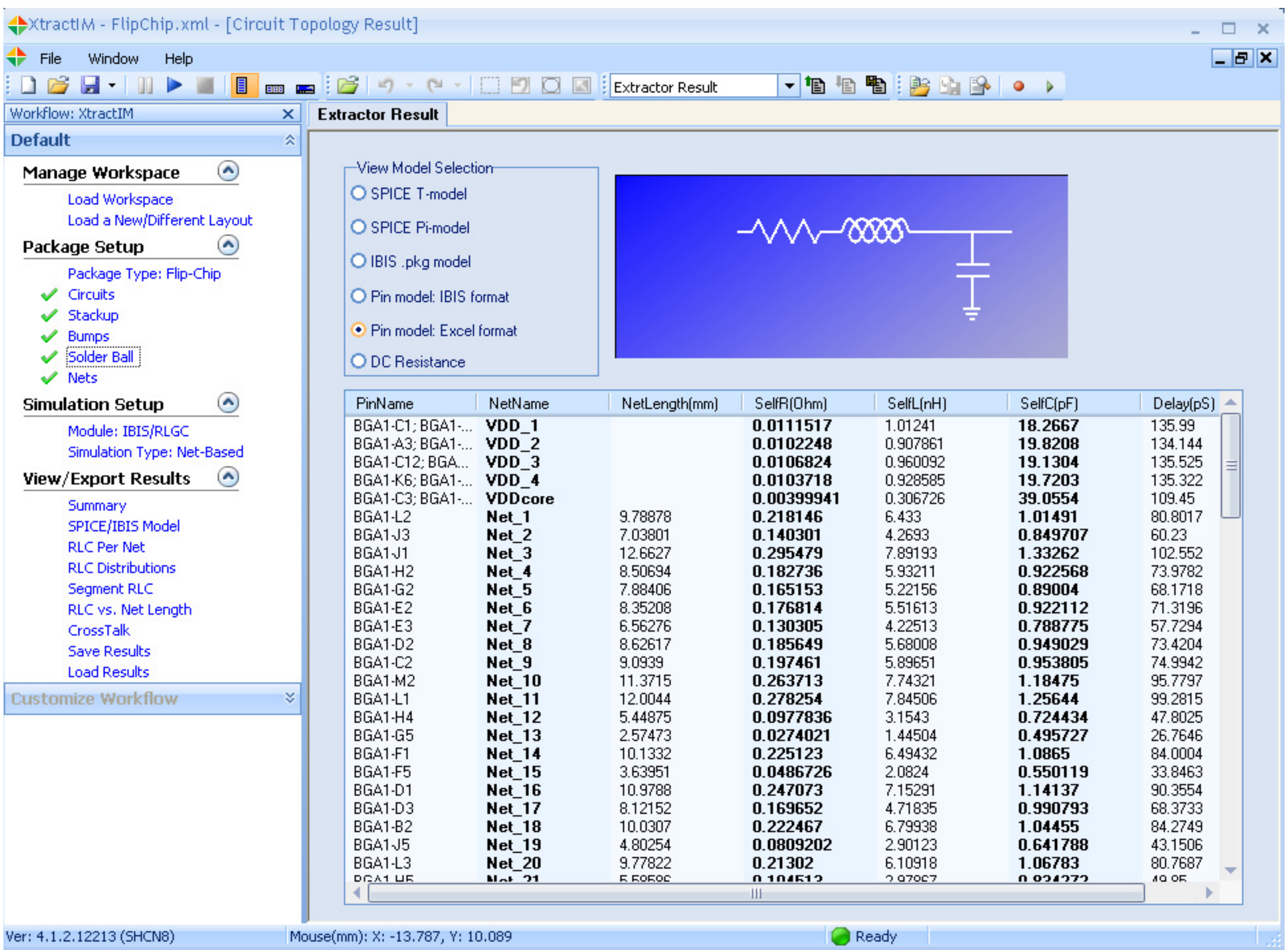
Pin Model: Excel Format

In the SPICE/IBIS Model window, click

Pin Model: Excel format

A .csv file is loaded. It includeds this information for each net. Self-C is the Maxwell Capacitance.

- DC_R
- Net length
- Net name
- Pin name
- Self-C
- Self-L
- Self-R

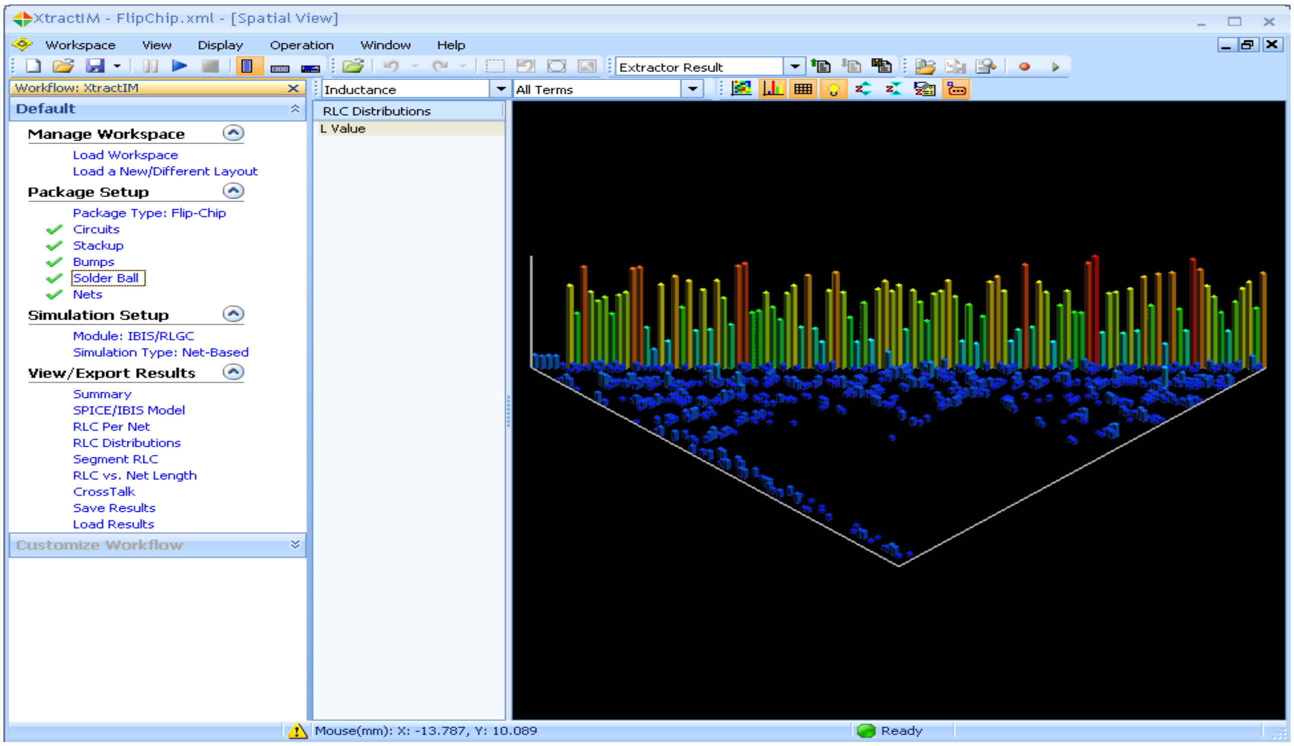


RLC Distributions

To see the full matrix value of R, L and C, click

RLC Distributions

RLC Distributions offers eight kinds of views.

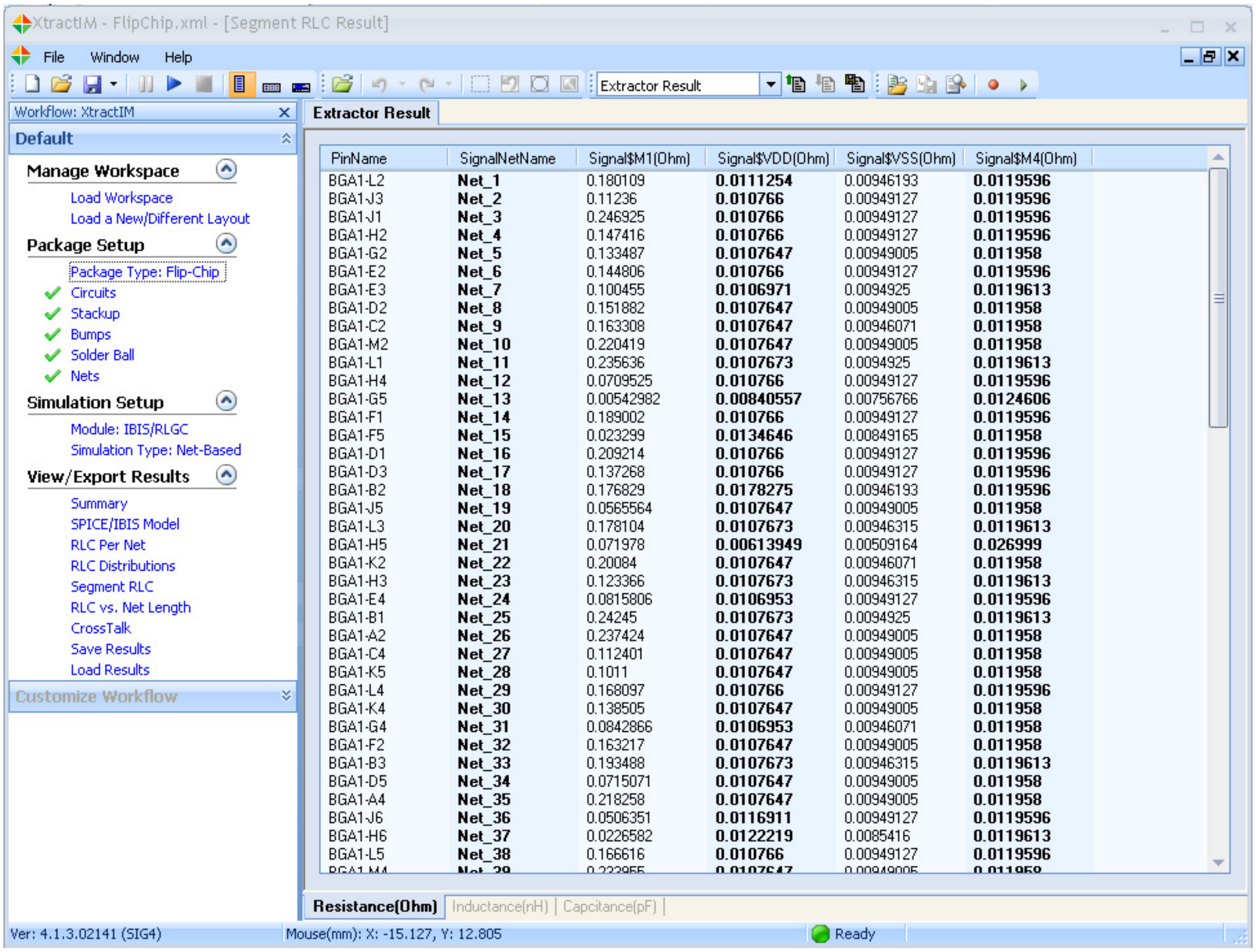


Segment RLC

For each signal net, XtractIM outputs the segment RLC of each metal layer.

Click on **Segment RLC** in the workflow pane (under View / Export Results). The Segment RLC values are shown at the bottom of the window.

There are three bars for Resistance, Inductance or Capacitance. Click on the Resistance, Inductance or Capacitance bar. The related values are displayed.

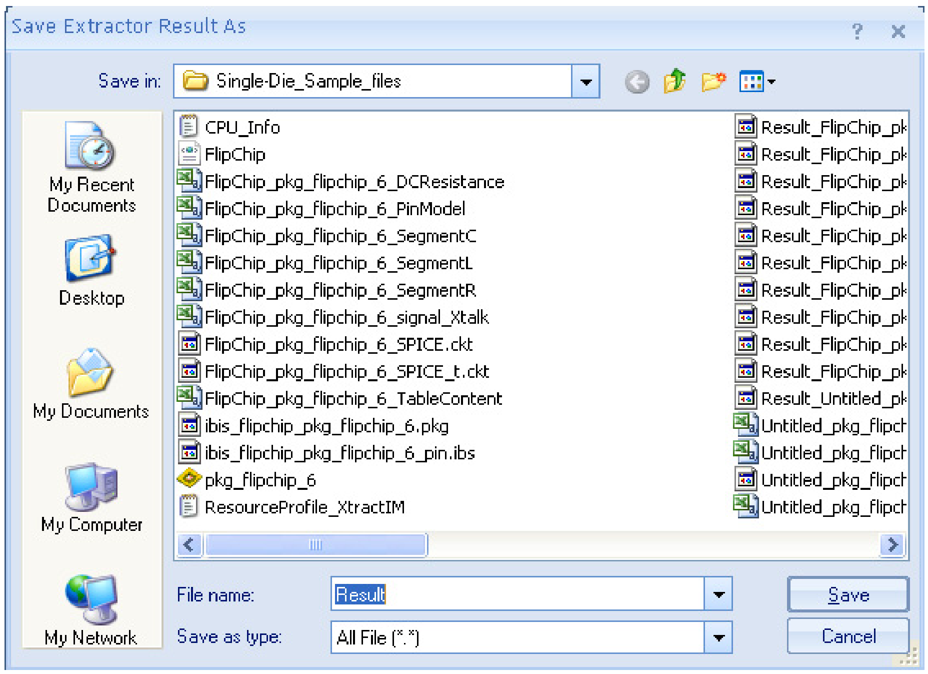


SAVE RESULTS

1. In the Workflow pane (under View / Export Results), click

   Save Results

   The Save Extractor Result window appears.



2. Enter a file name.
3. Click on **Save**. The results are saved in a binary file named as **result** and

   result_spd_file_name.xim

4. Click on **Cancel** if you do not want to save the results in the file name you entered.

Output Files

The SPICE file and two IBIS files are automatically saved by the tool. The result file is only if the user chooses to save. The **result** and **result*.xim** files save all the output data including:

- SPICE circuit
- Summary
- Two package model files.

The output files on hard disk include:

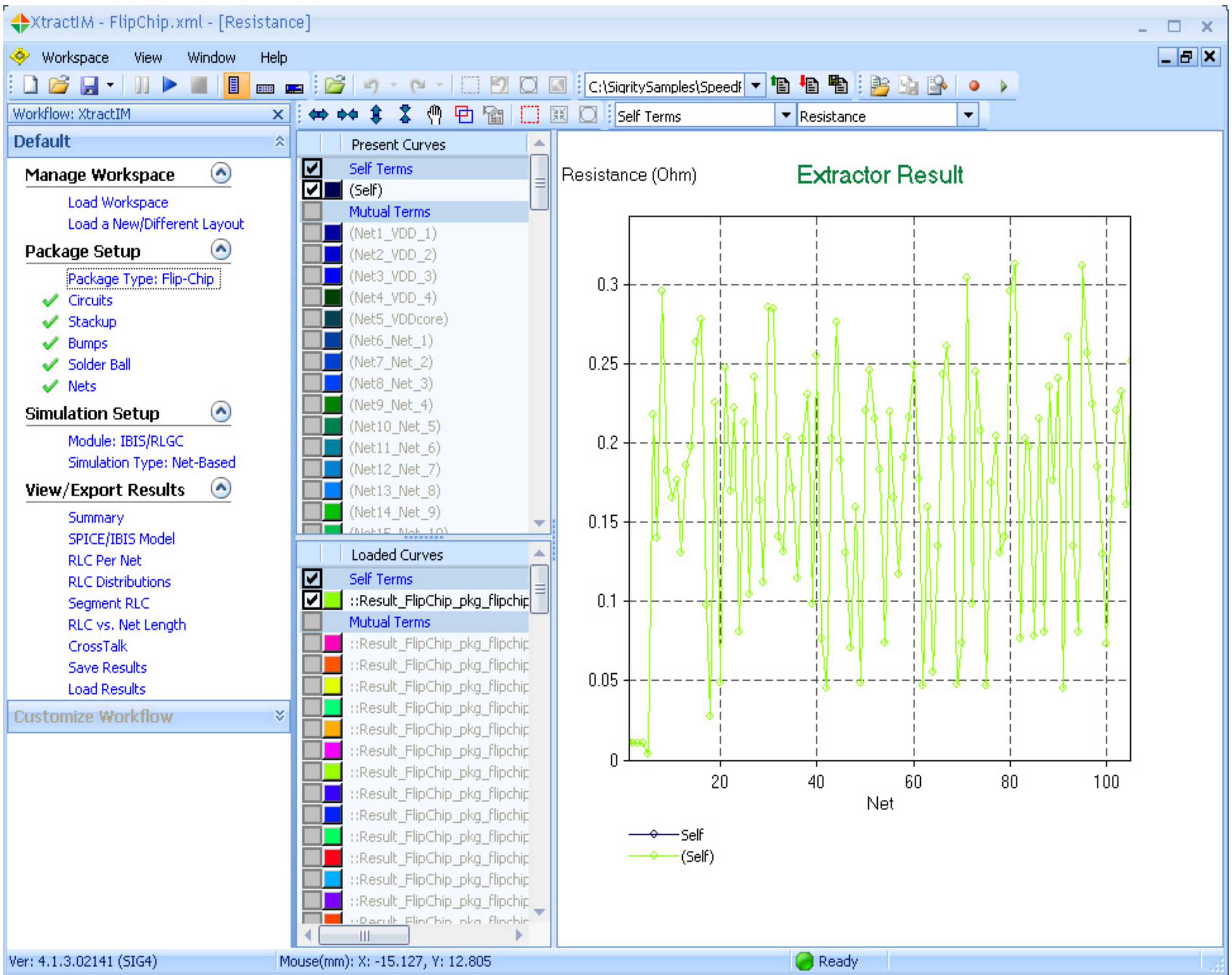
- **One IBIS Package Model File** — *.pkg file. Both L and C include coupling elements.
- **One Pin Model in Excel Format** — *.csv file. Including each signal net length, self-R, self-L, self-C, and time delay. No coupling elements are included.
- **One Pin Model in IBIS Fomat** — *.ibs file. Including self-R, self-L and self-C for each signal net. No coupling element is included.
- **One Summary Content in Excel Format** — *.csv file. Including RLC Full Matrix.
- **Three Segment RLC in Excel Format** — Segment RLC of each metal layer with *.csv files.
- **Two SPICE Circuit Files** — Pi-model named *.ckt and T-model named *_t.ckt.

Load in Saved Results

Saved results can be loaded by selecting **Load Results** in the workflow pane.

- **Loaded Curves** — Shows the loaded results.
- **Main window** — Shows the selected result.
- **Present Curves** — Present extraced results.

Choose to view present results or the loaded results. A loaded result can be unloaded by clicking on the Unload Extractor Result icon in the toolbar. The Load and Unload Result buttons are indicated.



Batch Mode Simulation

To run a simulation in Batch Mode, follow these steps.

1. Click

   Start -> Run

2. Change to the directory where the XtractIM.exe file is located.

Batch Mode Example

If you want to use the project (.spd file) defaulted in the workspace file (.ximx file), enter:

ExtraIM -b "Full_path_toMy_workspace_File*workspace filename*"

If you want to use a different project file other than the one in the .xml file, enter:

ExtraIM -b "Full_path_toMy_workspace_File*workspace filename*"

"Full_path_toMy_workspace_File*new_spd-filename"*

Saved Output Files

Upon completing the simulation, all output files are saved automatically in the same directory as the *.spd file. Saved files include:

- *.ckt
- *.csv
- *.ibs
- *.pkg

Package Setup

XtractIM can handle both flip-chip packages and wirebond packages with 3D bonding wire profiles. It can extract models of full packages or selected nets of a package.

Open the XtractIM main window. There are only two icons available: **New** and **Open**.

- **New icon** — Creates a new workspace.
- **Open icon** — Allows users to load an existing workspace file.

You'll setup the following items to prepare for a simulation.

1. Select a package type: wirebond or flip-chip.
2. Set the C4 Bump data if it is a flip-chip package.
3. Set the Solder Ball data.
4. Setup the circuits.
5. Select or deselect Die-circuit and Board circuit.
6. Setup the Stackup.
7. Set parameters for the C4 Bump and Solderball medium layer.
8. Select the nets for extraction.

There are four options to define the extraction frequency and extraction result output.

- Set Extraction Frequency.
- Set Mutual Capacitance Output Filter Factor.
- Set Mutual Inductance Output Filter Factor.
- Set Strongest Coupling Neighbors.

Chapter

6

XtractIM Simulation of a Stacked BGA Package

This chapter takes you through the steps to use the XtractIM tool in the simulation of a stacked BGA Package.

SIMULATION SETUP

A typical workflow in interaction mode includes the following steps.

- Create a new workspace file or load an existing file (.ximx file).
- Open a layout file (.spd file).
- Select a package type: wirebond or flip-chip, single BGA or stacked BGA.
- Set up the circuits: select or deselect Die-circuit and Board circuit.
- Set up the Stackup: set parameters for the C4 Bump/Solderball medium layer.
- Set the Bump data if it is a flip-chip package.
- Set the Solder Ball data.
- Select the nets for extraction.
- Setup extraction frequency and capacitance / inductance output control.

Setup the Package Simulation

1. Start in the Workspace.
2. Open the XtractIM main window.

   There are only two icons available: **New** and **Open**.

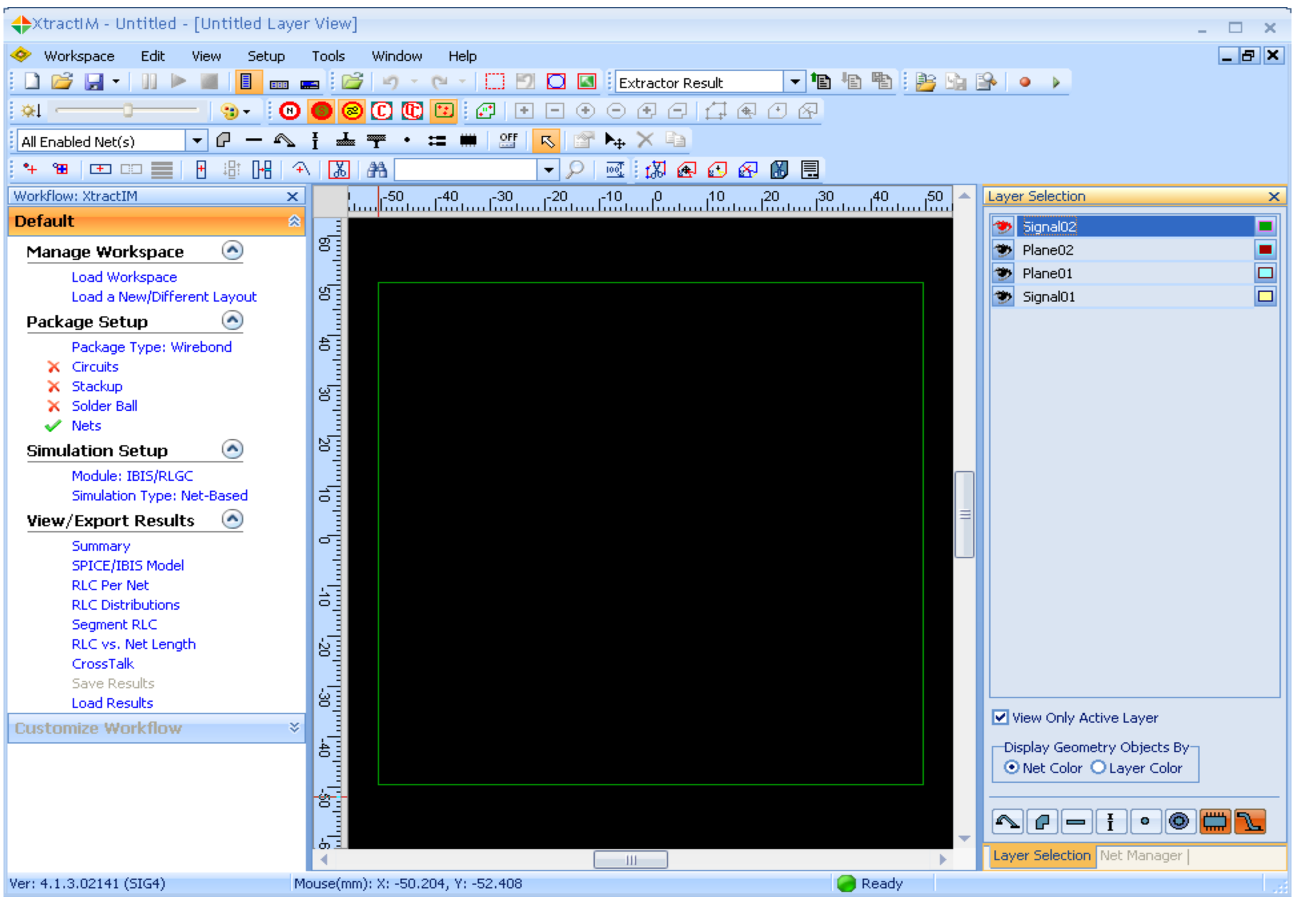
   The new icon creates a new workspace.

   The open icon allows users to load an existing workspace file.

3. Select appropriate icon (new  or open ). Click.
4. To create a new workspace, click on the **New** icon;

   or select

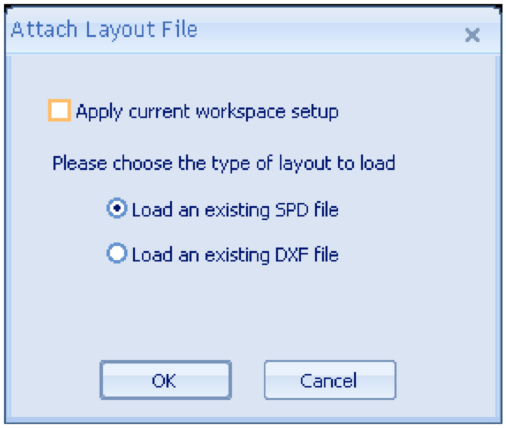
   Workspace > New



5. To load the Package Structure, click on

   Load a New / Different Layout

The Attach Layout File window opens.



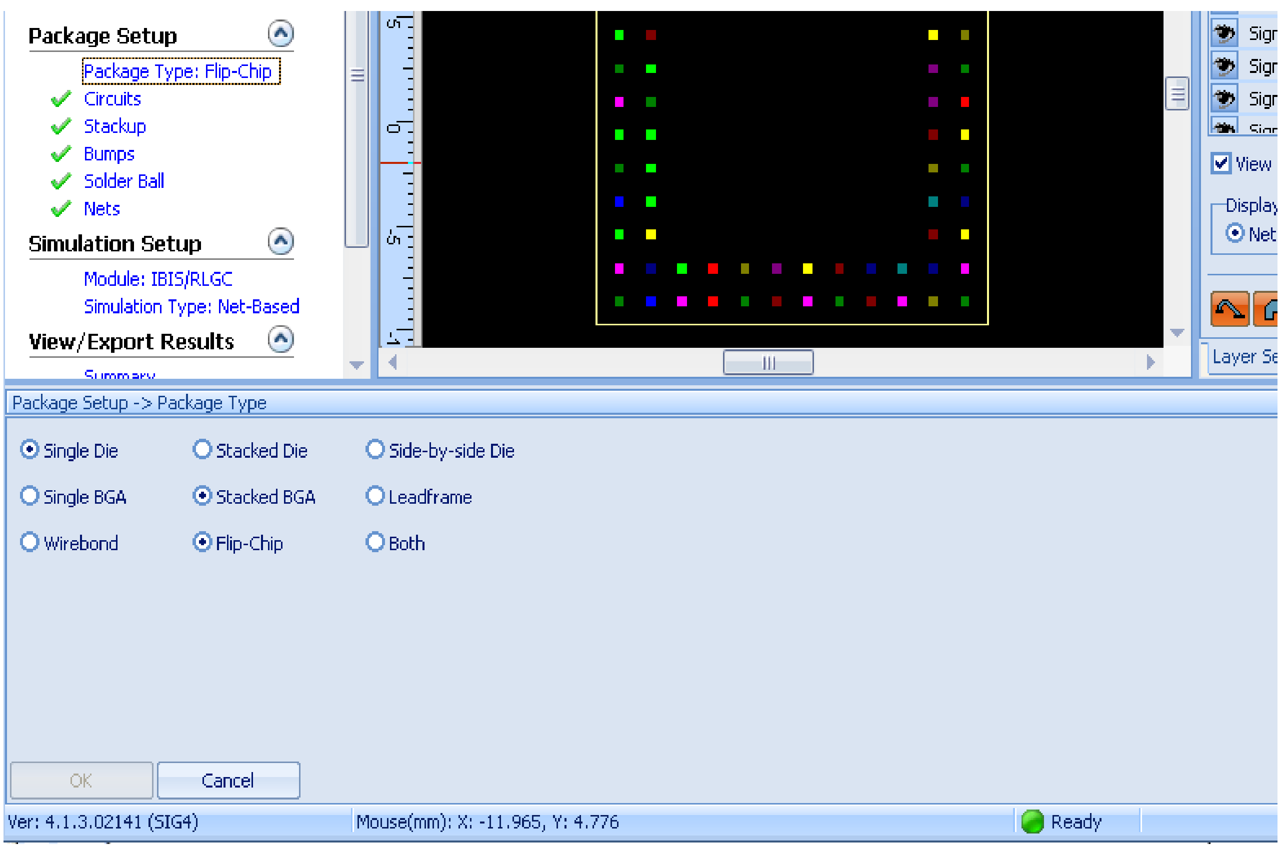
Select Package Type

1. Select a Package Type.

   The package type settings are displayed in the Editor pane.

   The example show a package type that is

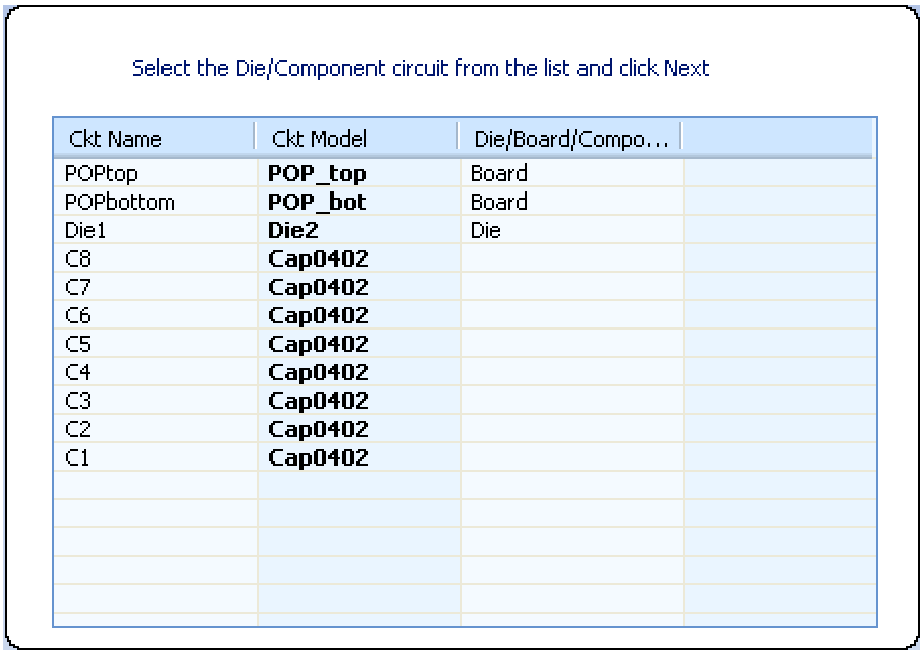
   Single Die, Stacked BGA, Flip-Chip



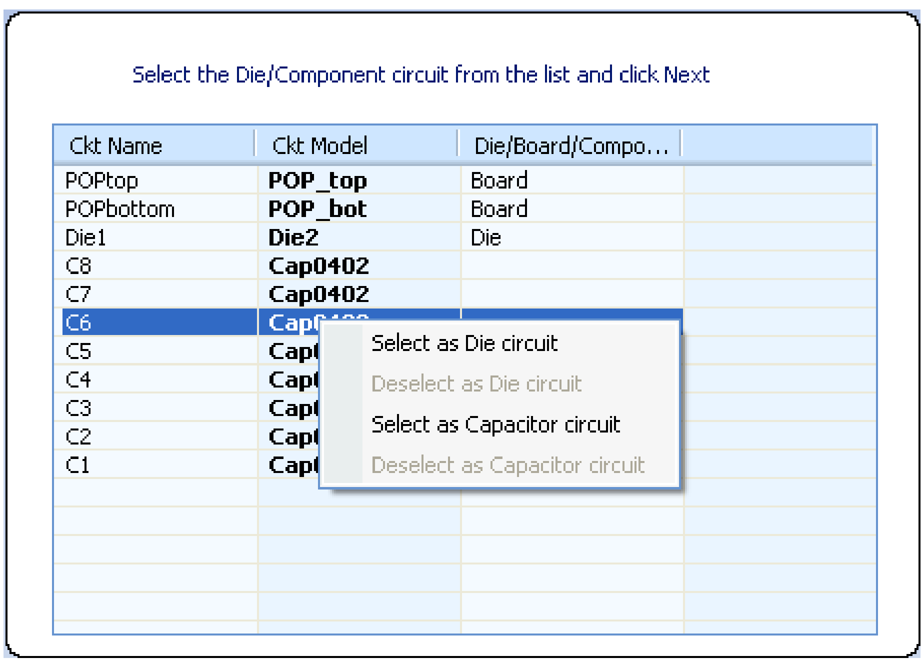
2. Click **OK** to save your selection.
3. Click **Cancel** if you want to change your selection, start over or cancel your session.

Setup Circuits

1. Click on **Circuits** in the Workflow pane to setup the Circuits data for a Flip-Chip package. A new pane opens up in the left side of the workspace.



2. Right-click on the desired circuit.

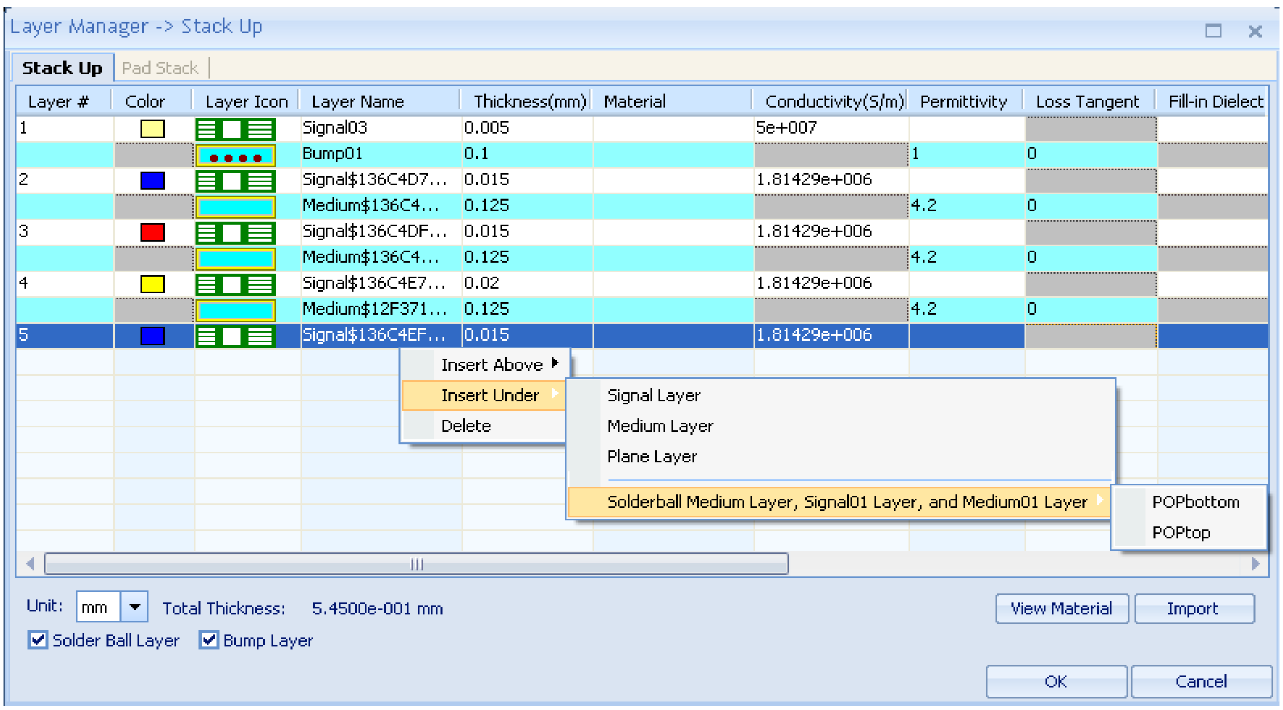


3. Select it as a **Die** circuit.
4. Click **Next**.

5. Right-click on another desired circuit.
6. Select it as a **Board** circuit.
7. Setup the second Board circuits.
8. Click **Finish** to finish the setup.

Setup Stackup

1. Click on **Stackup**. The Stackup window opens.
2. Right-click on the **Signal$Bottom** layer.



For a PCB medium layer you can insert:

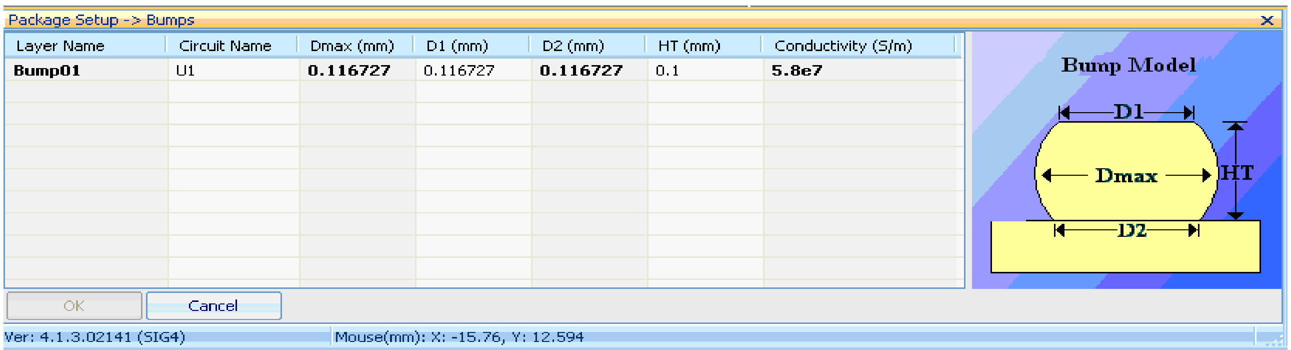
- A Solder Ball Medium Layer
- An empty signal layer
- A medium layer standing

All layers are inserted under Signal$Bottom. The added signal layer is located at the end of the solder ball.

Setup Bumps

The example shows the setup for a Flip-chip package.

1. Click on **Bumps** in the Workflow pane. A new window opens up in the Editor pane.



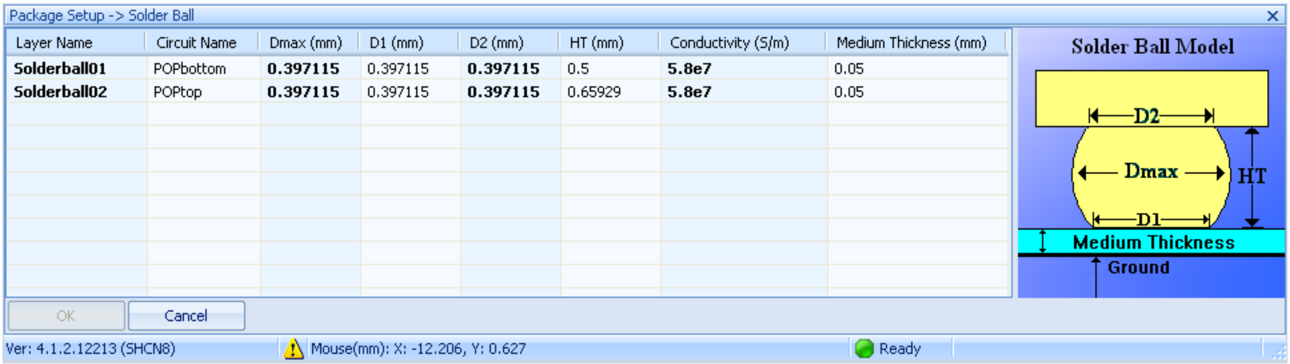
2. Input the settings for the C4 Bumps.

   Maximum Diameter: Dmax (mm)
   D1 (mm)
   D2 (mm)
   Height: HT (mm)
   Conductivity (S/m)

3. Click **OK** to save your entries or click **Cancel** if you do not want to save your changes.

Setup Solder Ball

1. Click **Solder Ball** in the Workflow pane. A new pane opens up in the Editor pane.



2. Input the settings for each Solder Ball.

   Maximum Diameter: Dmax (mm)
   D1 (mm)
   D2 (mm)
   Height: HT (mm)
   Conductivity (S/m)
   Medium Thickness

3. Click **OK** to save your entries.

   Click **Cancel** if you do not want to save your changes.

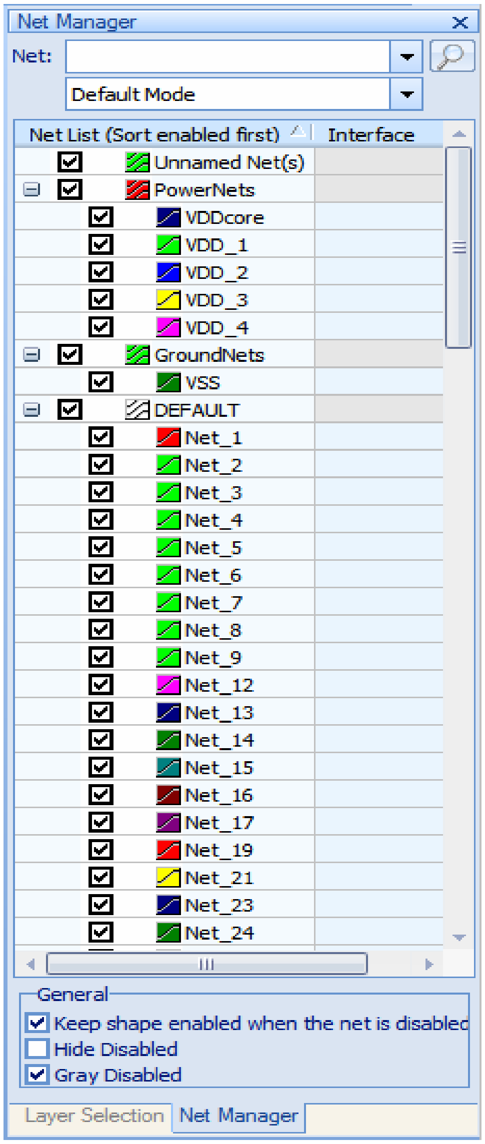
NOTE	Set up two solder balls for each stacked BGA package.

Setup Nets

1. Click on **Nets** in the workflow window. The Net Manager window opens.
2. Choose any desired nets for RLC extraction.

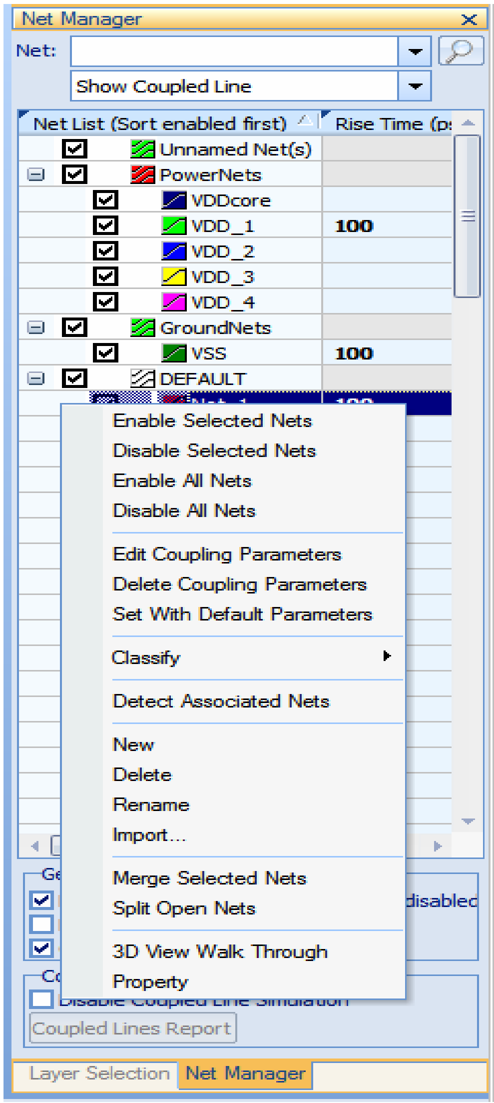
   Users can also move the signal net into and out of PowerNets and Ground Nets.

   - At least one Ground Net must be selected to act as a reference ground net.
   - Only choose the desired Ground Net as the reference ground net.

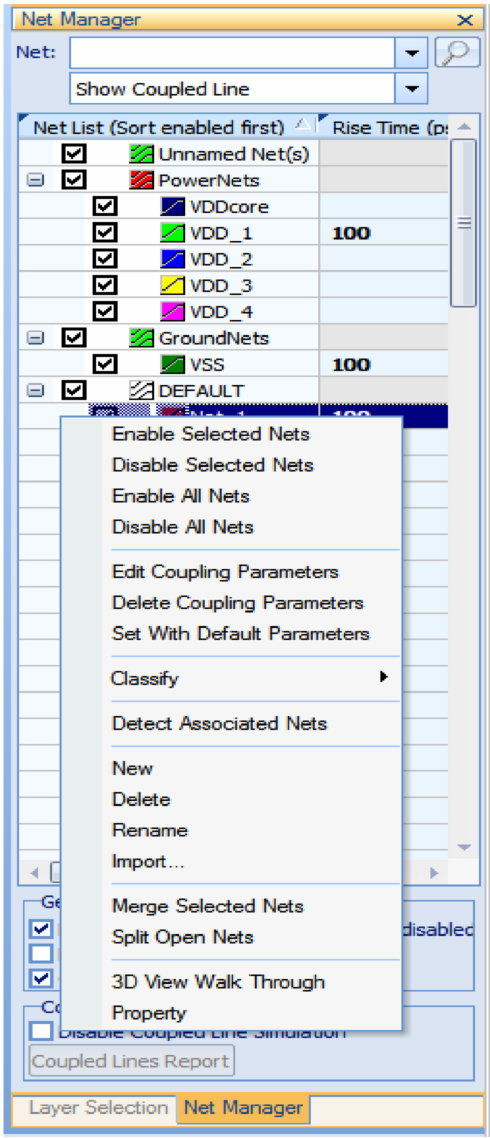


3. To set up ***Rise Time and %Coupling*** for identfying coupled Trace, click

   Auto Coupled Line



4. Select the nets you wish to edit.
5. Right-click to open the pop-menu.



6. Select

   Set With Default Parameters

7. Click

   Net Manager > Coupled Lines > Show Auto Coupled Lines

   The Trace identified as coupled lines appear.

Extraction Frequency and Capacitance / Inductance Output Control

You can change the extraction frequency. The default value is 30MHz. Use the window shown in the example to change the default value. Follow these steps:

1. Select

   Setup > Frequency of Extraction

2. Update the data in the pop-up window.

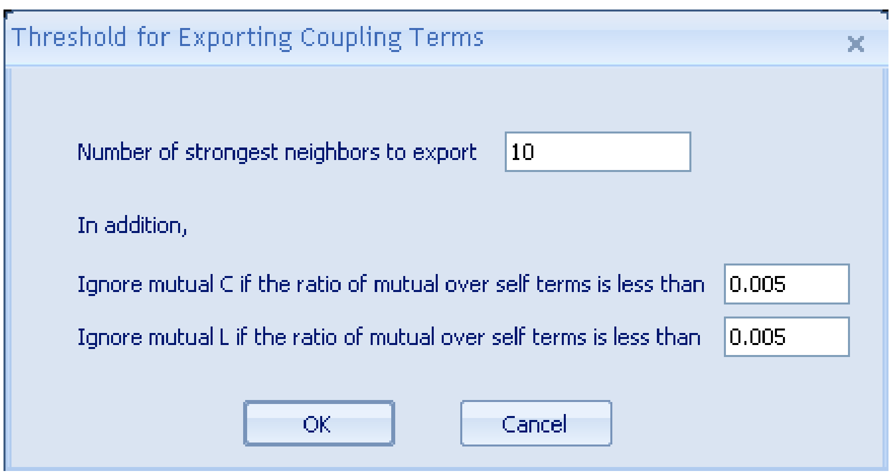
Set Output Factors

XtractIM captures all the coupling during the extraction stage. It has options to reduce the size of the output circuit during the export stage.

1. Open

   Setup > Threshold for Exporting Coupling Terms

   A pop-up window opens.



2. Choose the number of strongest coupling neighbors to be kept in the circuit model. In addition, ignore mutual capacitance or inductance if the ratio of mutual terms over self term is less than a percentage.

The default on number of strongest coupling neighbors is 10; which means

Only outputting the 10 strongest neighbors (including self)

The default percentage threshold for ignoring mutual capacitance /inductance is 0.005; which means

If the mutual capacitance or inductance is less than the 0.5% of the minimum of the two self-capacitances / inductances,

XtractIM will not output the mutual capacitanceor inductance.

Save Workspace and Layout File

You can see the save and open icons on the toolbar menu.

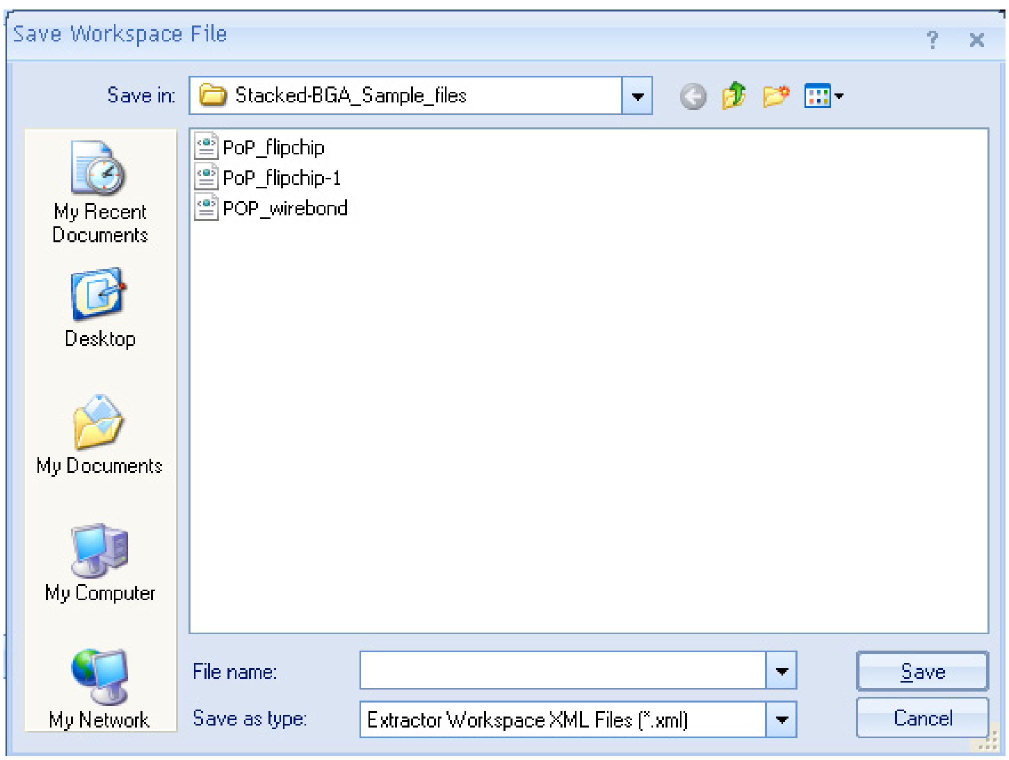
Save Workspace File

Method 1

Select

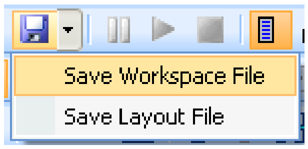
Workspace > Save As

The Save Workspace File dialog opens.



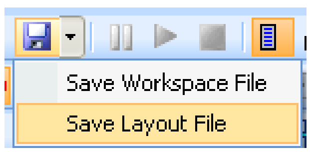
Method 2

Click on next to the Save  button, select **Save Workspace File** from the drop-down menu.



Save Layout File

Click on next to the Save  button, select **Save Layout File** from the drop-down menu.



Run the Simulation

Click on the **Play** button at the top of the window to start the extraction (simulation).

XtractIM only extracts RLCG for the net which has at least one pin at the Die-side and at least one pin at the board side. At the beginning of the simulation, if some nets have Die-Board mis-match, a pop-up window asks you to select the next action.

- **Continue** — Continue the simulation.
- **More Information** — Examine what nets are mis-matched.
- **Stop** — Cancel the simulation.

The **More Information** window lists all the mis-matched nets. You can investigate them to see whether it is a special design or a defective design. You can then decide whether or not to proceed with the simulation.

Note	Choose Continue, Stop or More Information. If 30 seconds pass and the user has not made a choice, by default, the simulation continues.

Observe and Save Simulation Results

XtractIM calculates each net's resistance, self loop inductance, conductance, and self capacitance as well as its mutual loop inductance and mutual capacitance with other nets.

The inductance and capacitance are matrices. For example, a simple group of four nets has the following inductance and capacitance matrix.

$$\begin{bmatrix} L_{11} & L_{12} & L_{13} & L_{14} \\ L_{21} & L_{22} & L_{23} & L_{24} \\ L_{31} & L_{32} & L_{33} & L_{34} \\ L_{41} & L_{42} & L_{43} & L_{44} \end{bmatrix} \qquad \begin{bmatrix} C_{11} & C_{12} & C_{13} & C_{14} \\ C_{21} & C_{22} & C_{23} & C_{24} \\ C_{31} & C_{32} & C_{33} & C_{34} \\ C_{41} & C_{42} & C_{43} & C_{44} \end{bmatrix}$$

In the Inductance Matrix, the Diagonal Element is the Self Inductance of each net, and the off-diagonal elements are mutual Inductance.

There are two concepts of capacitance matrix: Maxwell capacitance matrix and SPICE capacitance matrix.

- **Maxwell Capacitance Matrix** — Each diagonal element is the loading capacitance (for example, capacitance to ground when other nets are grounded which represents the worst-case capacitive loading). Off-diagonal elements are mutual capacitance with negative values.
- **SPICE Capacitance Matrix** — Each diagonal element is capacitance to ground. Off-diagonal elements are mutual capacitance with positive values.

The relationship between Maxwell capacitance and SPICE capacitance matrix is shown below.

$$C_{ij}(SPICE) = -C_{ij}(Maxwell)$$
$$C_{ii}(Maxwell) = \sum_j C_{ij}(SPICE)$$
$$C_{ii}(SPICE) = \sum_j C_{ij}(Maxwell)$$

In RLC Per Net view, there are two options:

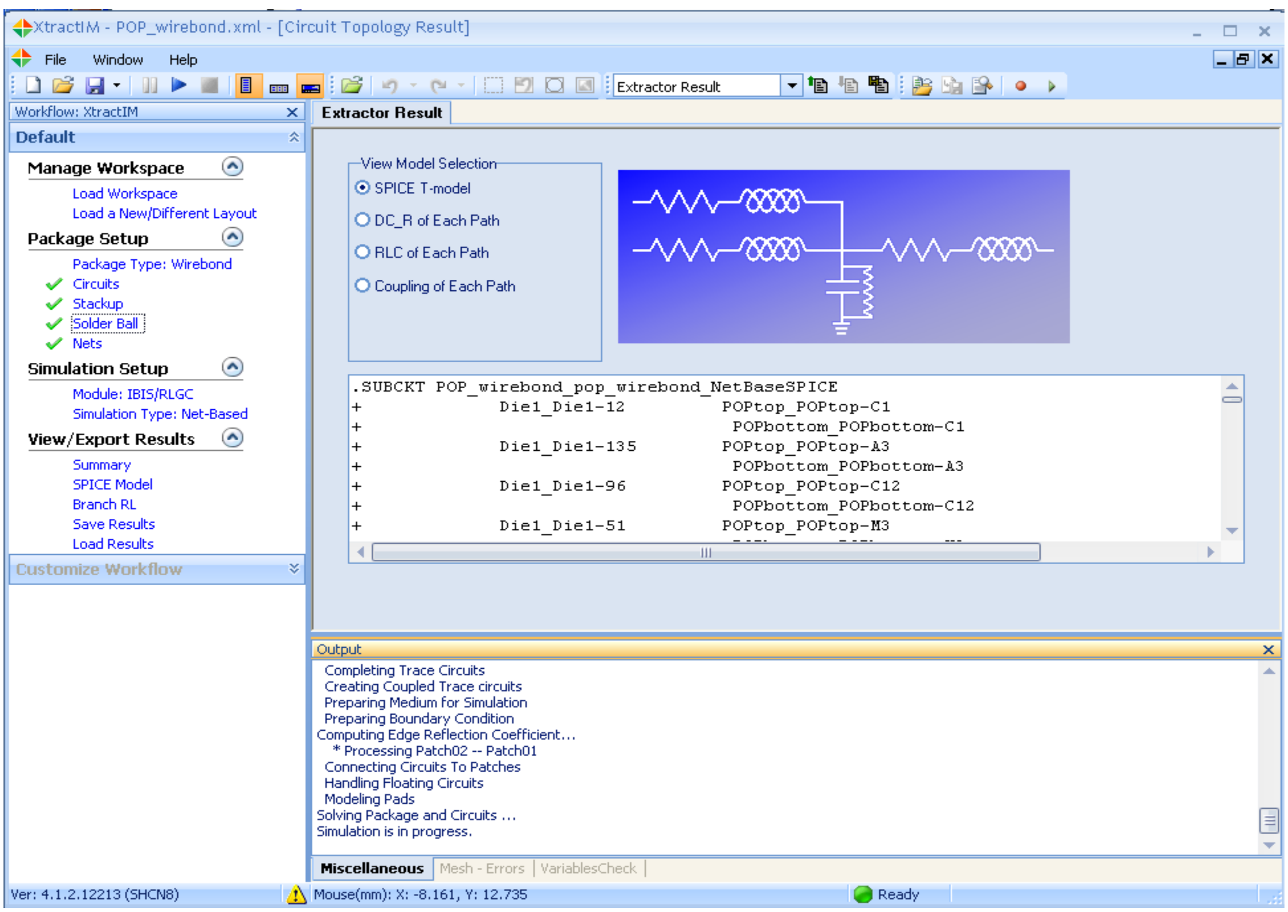
- **Mutual Term View** — Mutual inductance or SPICE mutual capacitance.
- **Self-Term View** — Resistance, self-inductance or Maxwell diagonal capacitance.

You can choose to view resistance, self-inductance, self-capacitance for each net.

You can also view mutual terms if inductance and capacitance are desired. Usually conductance is very low, so there is no view for conductance.

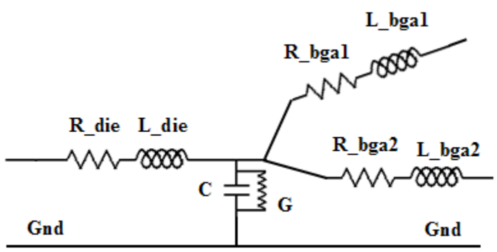
Display Results

Upon finishing the simulation, the defaulted result display is a SPICE model.



Circuit Topology

The circuit topology for stacked-BGA is shown in the following illustration. Here we see one net and three branches for Die, BGA1 and BGA2.



Display Results Example

1. Click on

   RLC of Each Path

2. Click to view the Net Length, DC R, Self R, Self L, Self C, or Delay of a Signal Net.

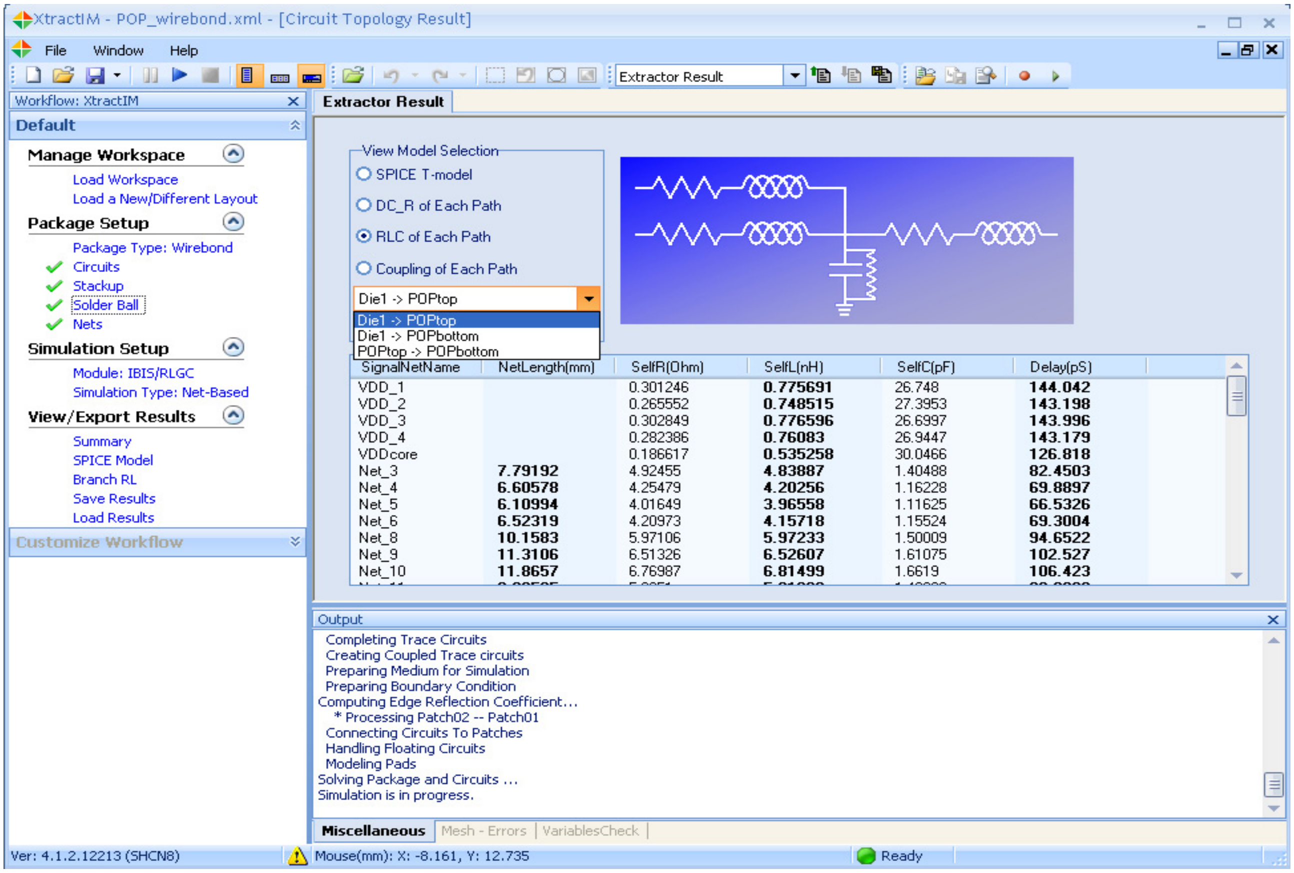
In the example, these path names are used for each of the three paths. The actual Die or BGA circuit name is given to describe each of the three paths.

Die-toBGA1 — U1 ::: POPtop

Die-toBGA2 — U1 ::: POPbottom

BGA1-toBGA2 — POPtop ::: POPbottom

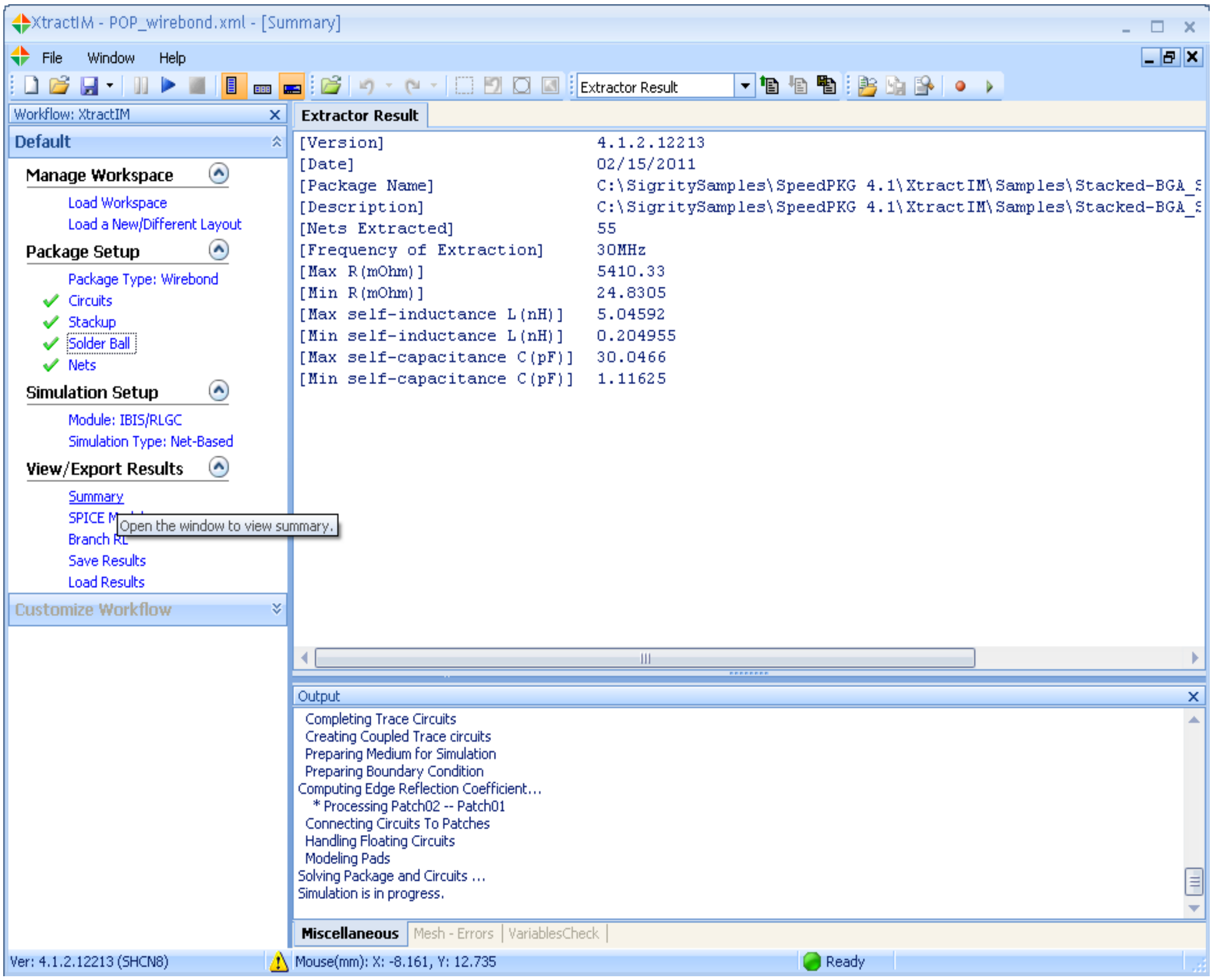
Extractor Results Display



Summary of the Extracted Results

Click on **Summary** to open the brief summary about the extracted R, L, and C. It shows the maximum (Max) and minimum (Min) values and other information.

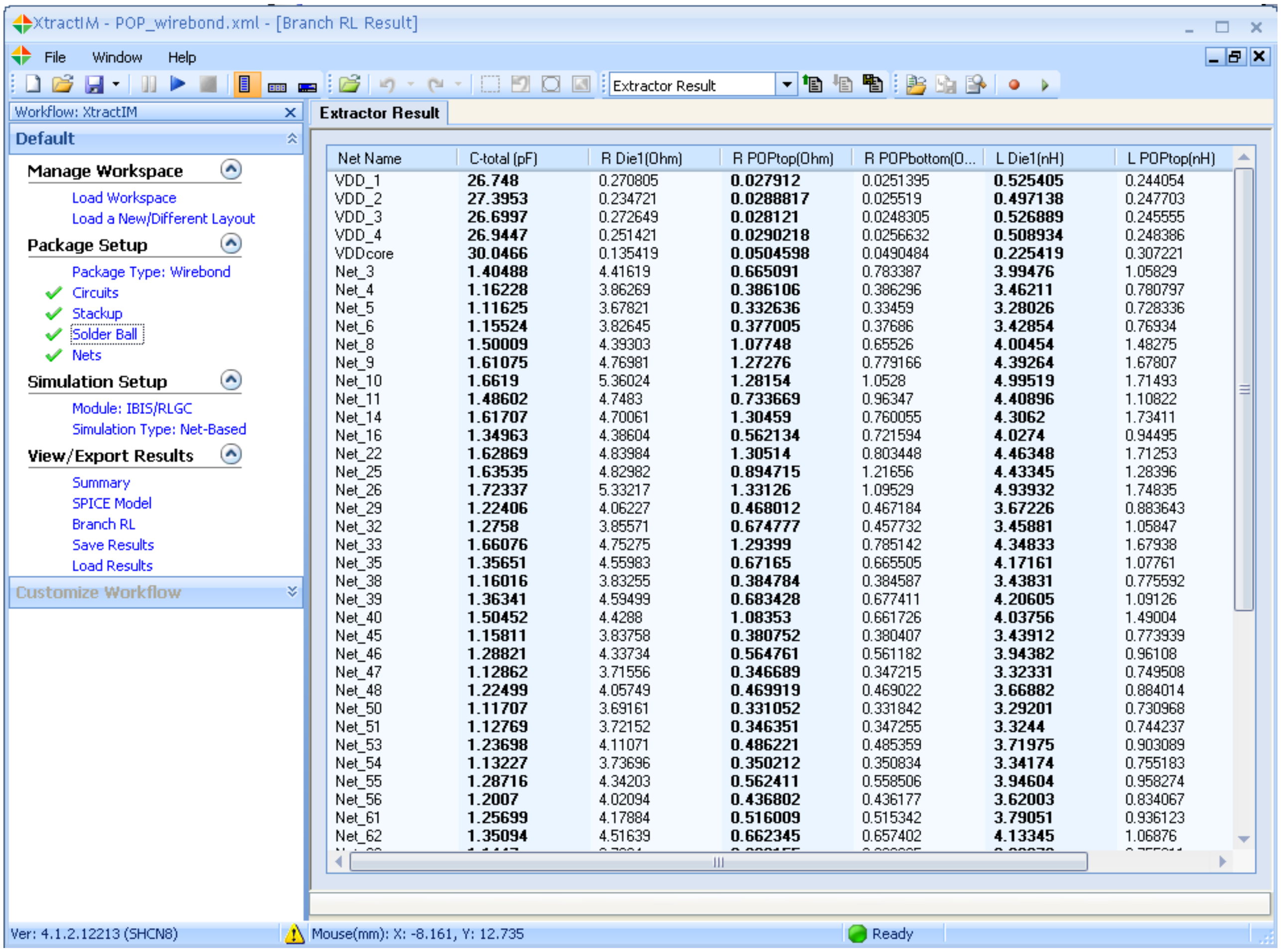
A typical Summary display is shown below.



Brand RL and Total C

Click **Branch RL** to open up a .csv file and display the branch R, L, and C of each net.

If a branch is missing from a net, the cells are left empty.

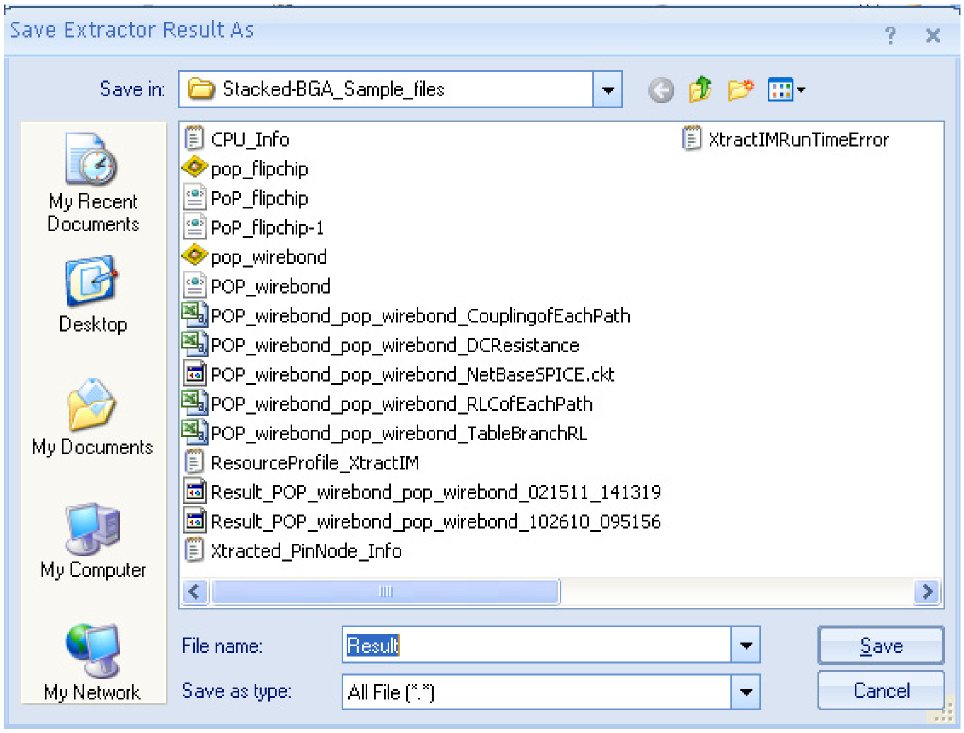


Save Results

1. In the Workflow pane under View/Export Results, select

Save Results

The Save Extractor Result window appears.



2. Enter a file name
3. Click on **Save**. The results are saved in a binary file named **Result**.
4. Click on **Cancel** if you do not want to save the results in the file name you entered.

Output Files

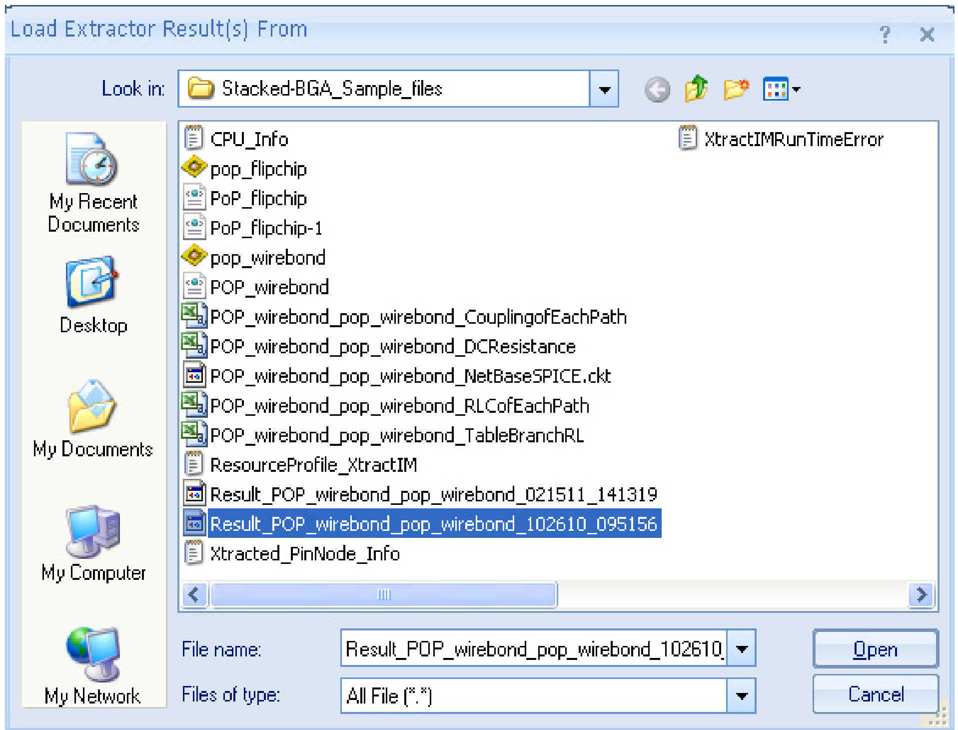
The **result** and **result*.xim** files save all the output data The output files on hard disk include:

- **One SPICE Circuit File** — Named *.ckt.
- **RLC of Each Path File** — An .xls file including each Signal Net's Name, Length, DC R, Self R, Self L, Self C and Delay.
- **Branch RL File** — An .csv file including the branch R, L, and total C of each net.

Load in Saved Results

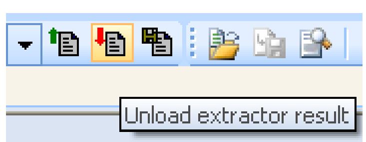
Saved results can be loaded by selecting

Load Results



Choose to view present results or the loaded results.

To unload a loaded result, click on the **Unload Extractor Result** Icon.



Batch Mode Simulation

To run a simulation in Batch Mode, follow these steps.

1. Click

   Start -> Run

2. Change to the directory where the XtractIM.exe file is located.

Example

If you want to use the project (.spd file) defaulted in the workspace file (.ximx file), enter:

ExtraIM -b "Full_path_toMy_workspace_File*workspace filename*"

If you want to use a different project file other than the one in the .xml file, enter:

ExtraIM -b "Full_path_toMy_workspace_File*workspace filename*"

"Full_path_toMy_workspace_File*new_spd-filename*"

Saved Output Files

Upon completing the simulation, all output files, including *.xls and .csv files are saved automatically in the same directory as the *.spd file.

Chapter 7

XtractIM Pin-Based Simulation of a BGA Package

This chapter takes you through the steps to use the XtractIM tool in the simulation of a BGA package with pin-based Extraction.

SIMULATION SETUP

A typical workflow in interaction mode is the same as net-base extraction.

Single-BGA Package

A qualified net is the one which has at least one pin in each of the die- and BGA- circuits. In addition, no open circuit exists for these pairs of pins.

Stacked-BGA Package

A qualified net is the one which has at least one pin in each of the die-, BGA-top, and BGA-bottom circuits. In addition, no open circuit exists for these three pins.

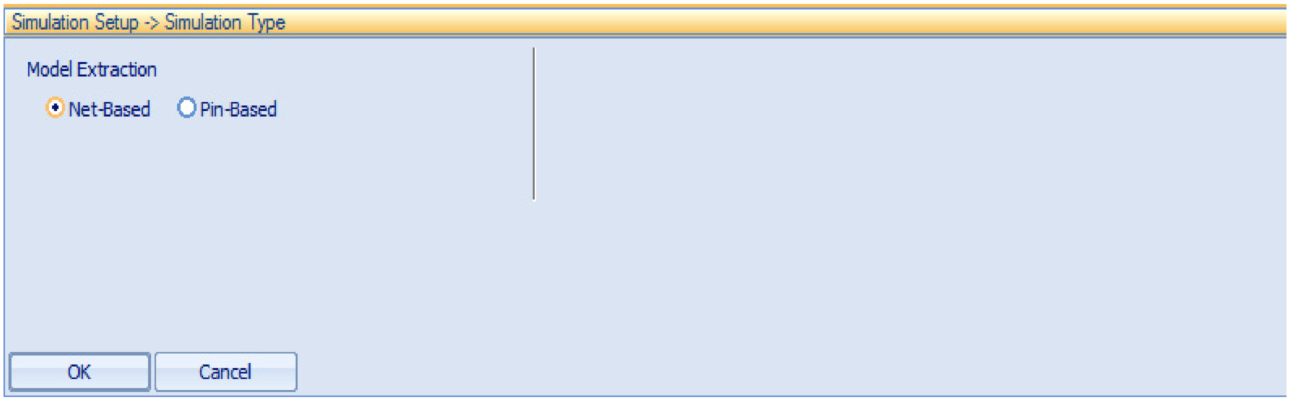
XtractIM automatically checks to see if a net is qualified to be a reference net.

Setup Simulation Type

The Simulation Setup options are located in the menu bar on the left side of the window.

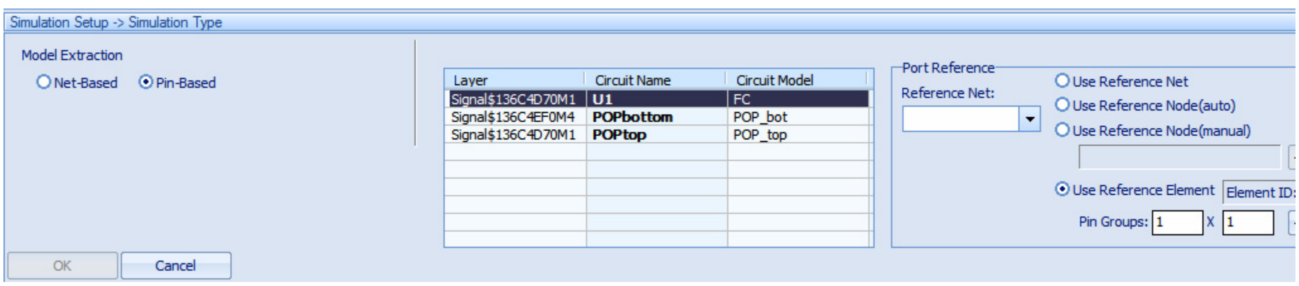
1. Click

   Simulation Type

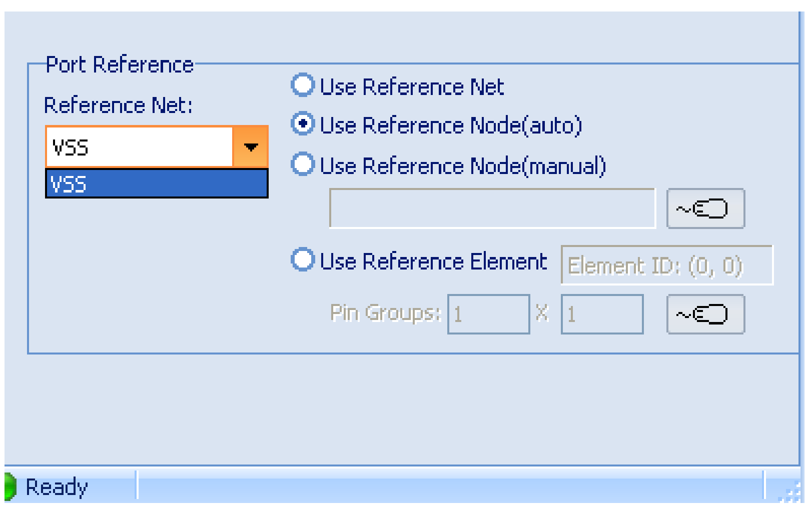


2. Select

   Pin-based



3. In the **Reference Net** field, all qualified reference nets are displayed in a list.
4. Select **Reference Net** for each layer.

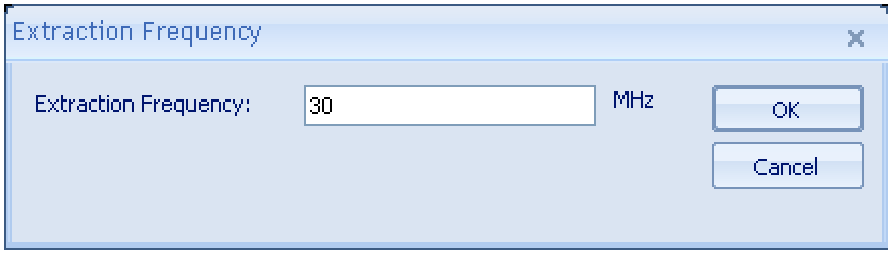


5. Select a ground net as the reference net for a pin-based simulation.

Setup Extraction Frequency

1. To change the extraction frequency, select

   Setup > Extraction Frequency



2. Update the data in the pop-up window.
3. Use the Threshold for Exporting Coupling Terms window to change the default value.

   The default value is 30MHz.

Setup Threshold for Exporting Mutual Terms

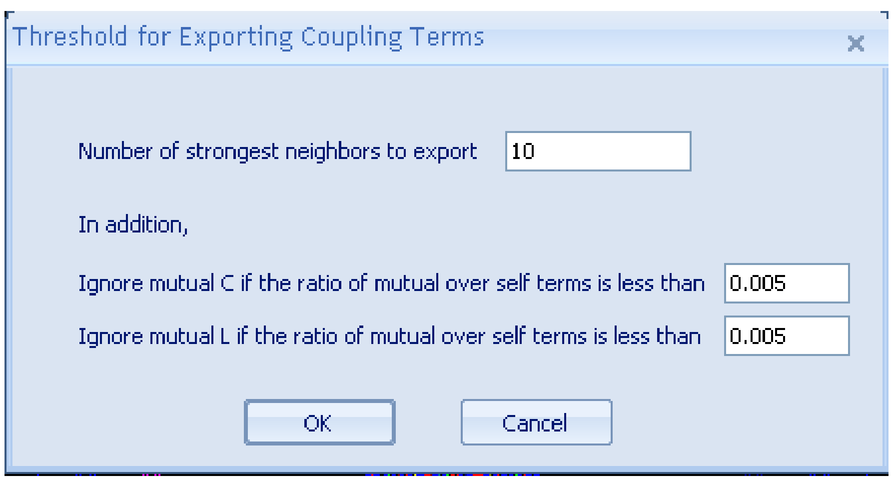
Use the XtractIM options to reduce the size of the output circuit during the export stage.

XtractIM captures all the coupling during the extraction stage.

1. Open

   Setup > Threshold for Exporting Coupling Terms

   A pop-up window opens.



2. Choose the number of strongest coupling neighbors to be kept in the circuit model.

   The default number of strongest coupling neighbors is 10 (including self).
3. Ignore mutual capacitance or inductance if the ratio of mutual terms over self term is less than a percentage.

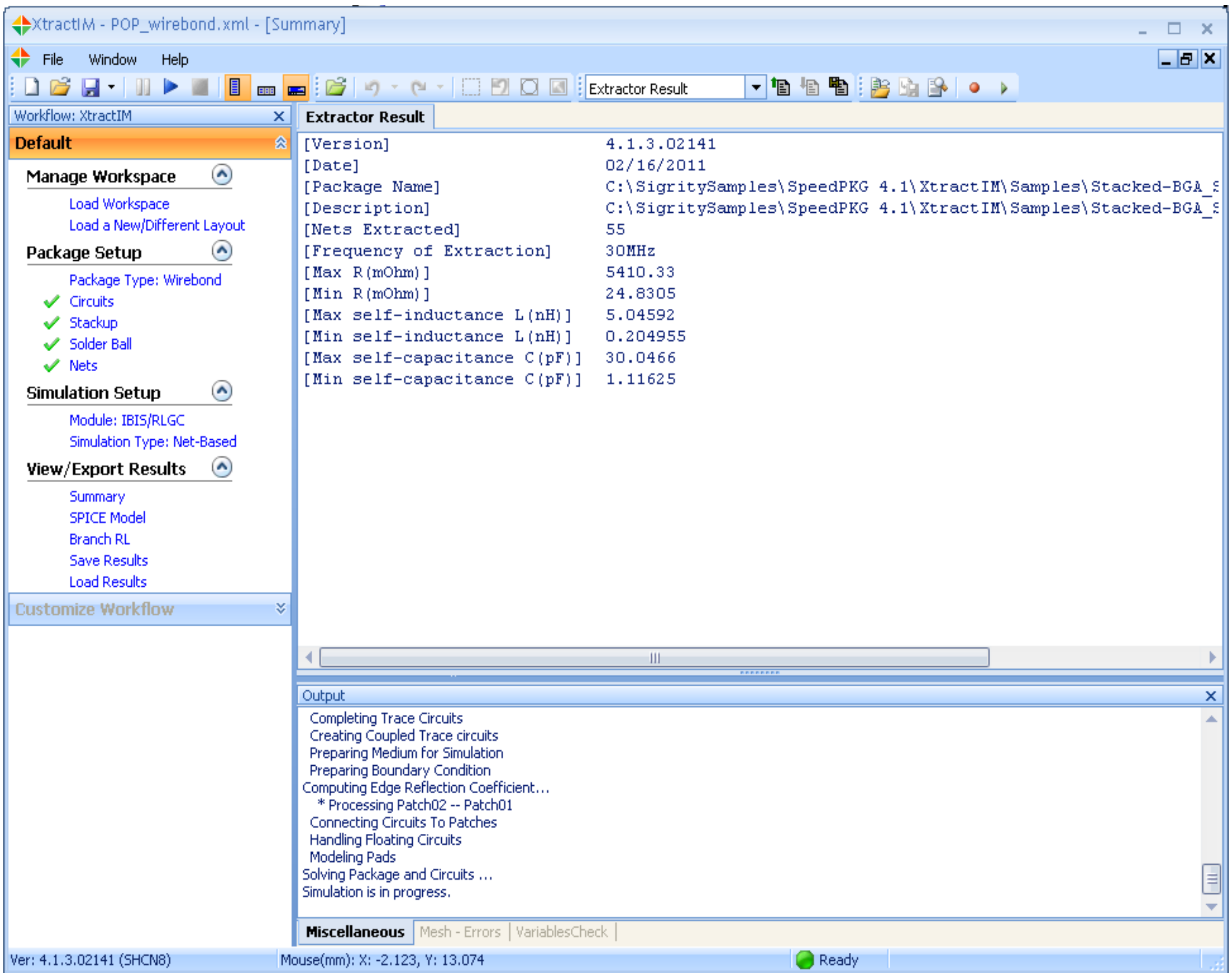
   The default percentage threshold for ignoring mutual capacitance/inductance is 0.005.

If the mutual capacitance / inductance is less than the 0.5% of the minimum of the two self-capacitances / inductances, XtractIM does not output the mutual capacitance / inductance.

View / Export Results

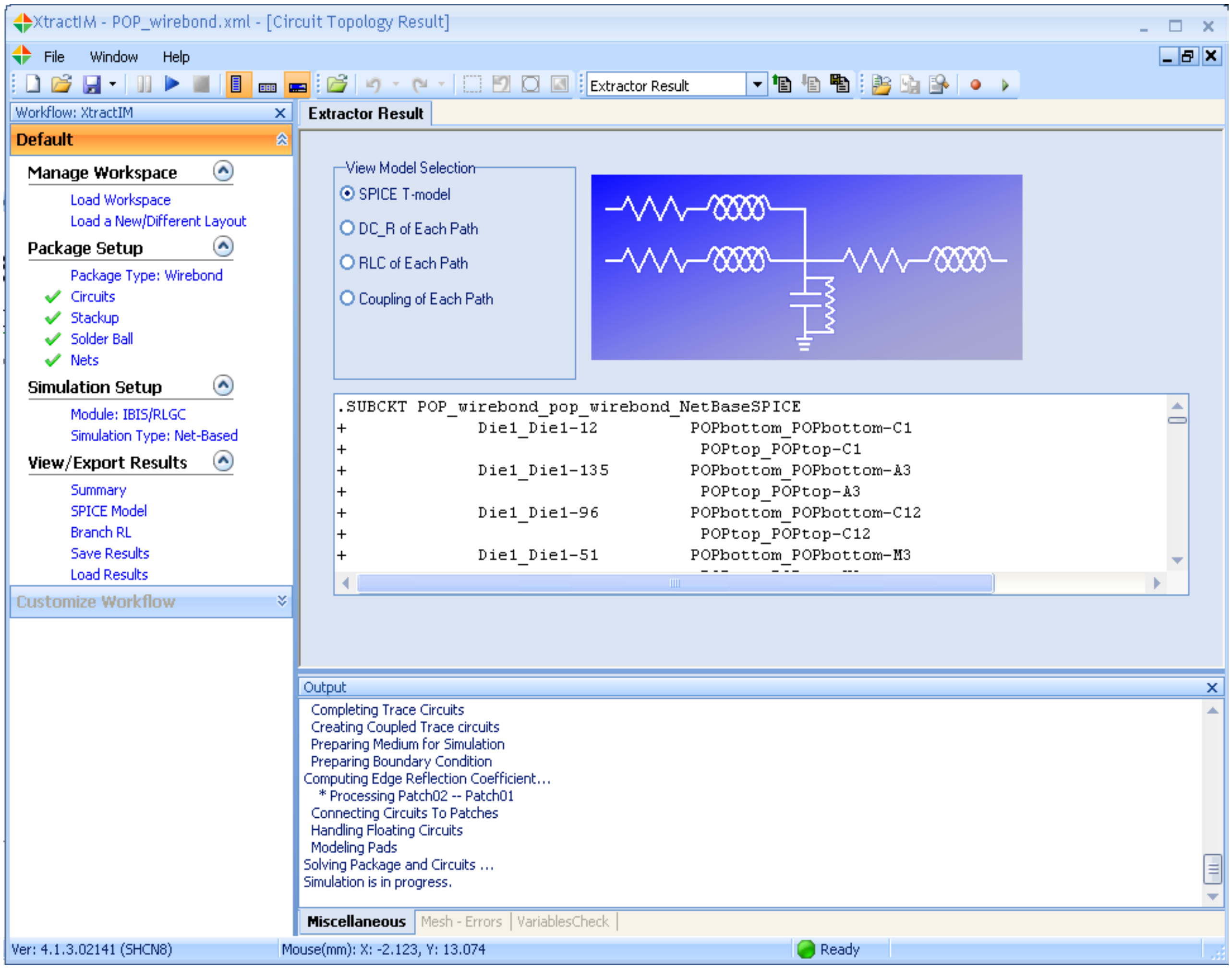
The View/Exports Results options are displayed in the menu bar on the left side of the window.

Click on **Summary** to open the summary that shows the maximum and minimum R, L, C, and other information.



SPICE Model

Click on SPICE Model. The SPICE Model name ***.ckt** is loaded.



Chapter 8

TCL Command Support for Workspace Setup

This chapter introduces TCL command for workspace setup in the XtractIM tool.

Introduction

TCL (Tool Command Language) scripts can be used to configure and automate frequently used command in Allegro Sigrity tools. They can also be launched outside the Sigrity tools in batch mode to automate company design flows.

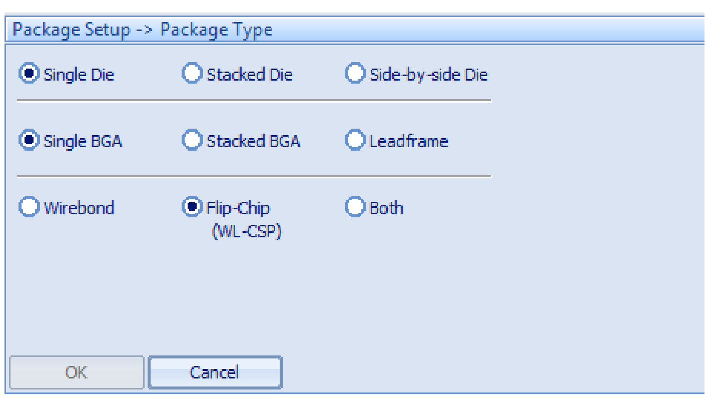
New TCL command for XtractIM is developed to support workspace setting. Three types of new TCL command are available, including Setting up TCL, Doing Simulation TCL, and Creating Report TCL.

For the other existing TCL command, please refer to ***Tcl_Scripting_Reference.pdf*** in <ASI_INSTALL_DIR>\Update3\Doc\Common Documents\ for details.

Setting up TCL

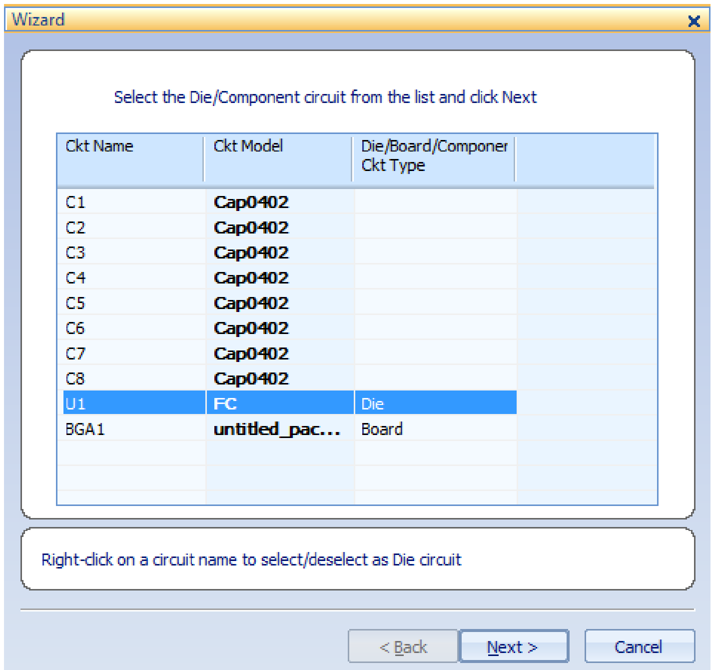
- Update Package Type

  Format: sigrity::update PackageType -dieType|d {0-2} -bgaType|b {0-2} -attachType|a {0-2} -leadType|l {0-2}



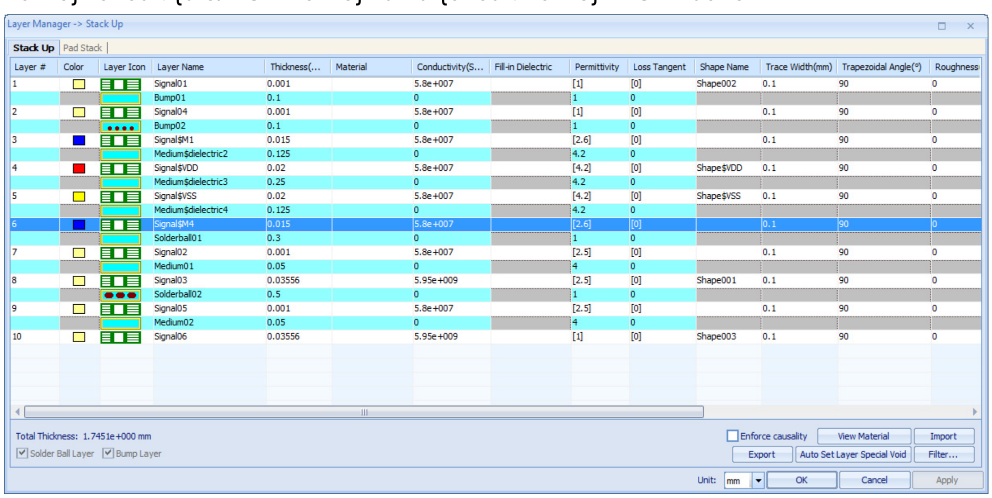
- Update Circuits

Format: sigrity::update Circuits -dieCkts|d {circuit name} -boardCkts|b {circuit name} -capCkts|c {circuit name} -wbCkts|w {circuit name}



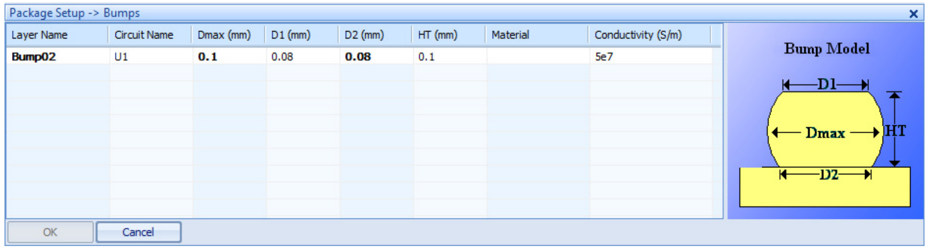
- Add Layer

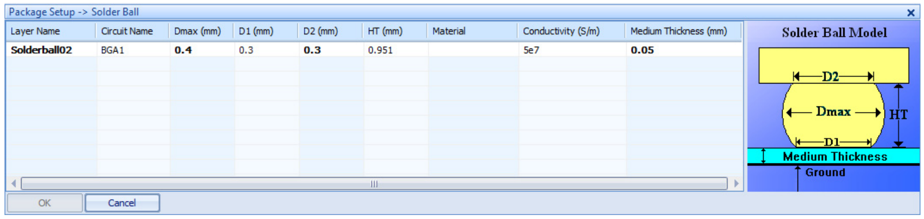
Format: sigrity::add Layer {layer type} -above | -under {layer name} -name {new name} -circuit {die/BGA name} -bind {circuit name} -PCBAbove

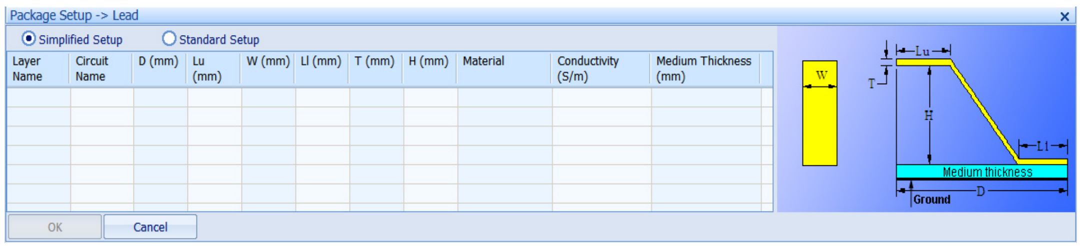


- Update Attributes

Format: sigrity::update Attributes -circuit|c {circuit name} -Dmax {value} -D1 {value} -D2 {value} -HT {value} -conductivity|o {value} -mediumThickness|mt {value} -D {value} -Lu {value} -W {value} -Ll{value} -T {value} -H {value}







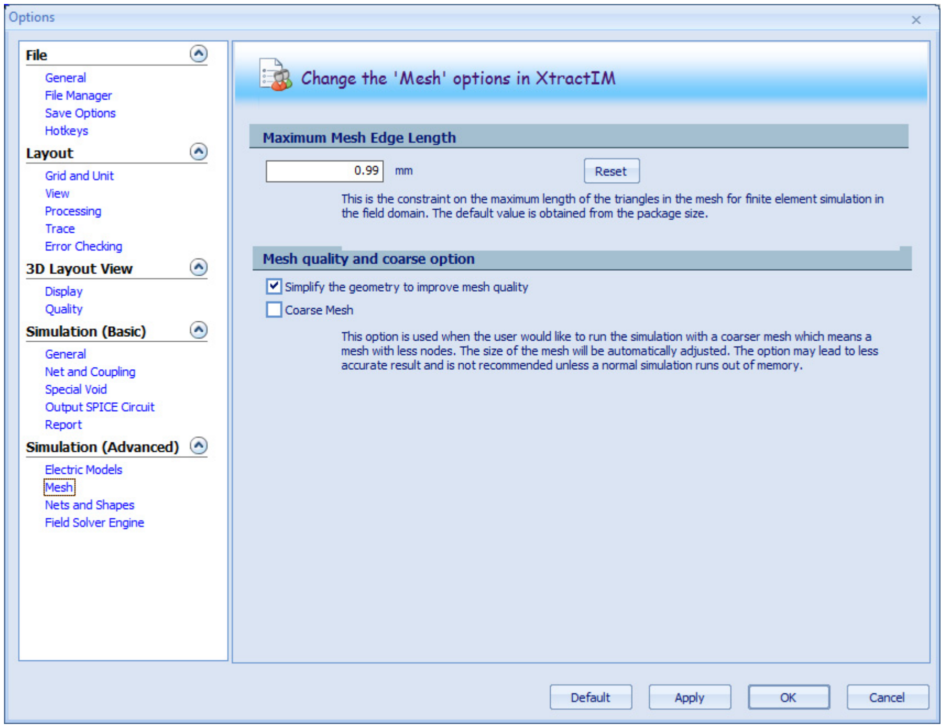
NOTE	The unit for value is **meter**.

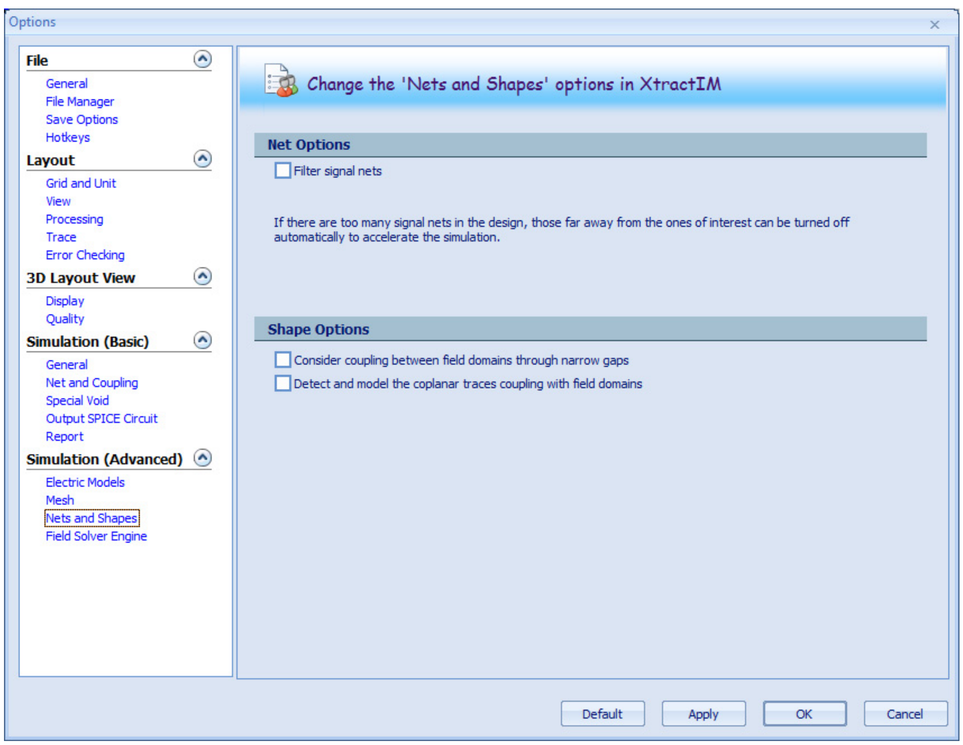
- Update Options

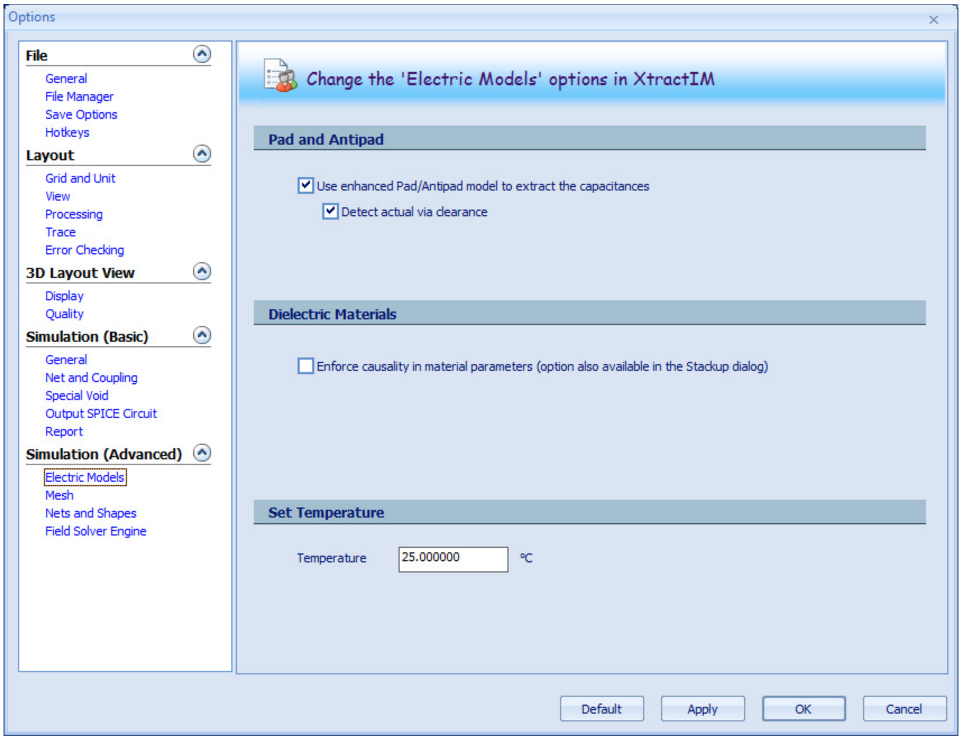
Format: sigrity::update Options -meshEdgeLength|m {value} -simplifyGeometry|s {0|1} -coarseMesh|c {0|1} -narrowGapModeling|n {0|1} -modelCoplanarTraces|pl {0|1} -filterSignalNets|f {0|1} -enforceCausality|e {0|1} -enhancePadAntipad|a {0|1} -detect-ViaClearance|d {0|1} -temperature|t {value} -solver {value}

NOTE	The unit for value is **meter**.

NOTE	The command option "-dieType|d"can be "-dieType" or "-d".

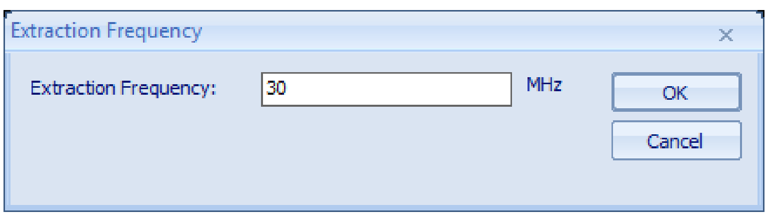

Options
File
General
File Manager
Save Options
Hotkeys
Layout
Grid and Unit
View
Processing
Trace
Error Checking
3D Layout View
Display
Quality
Simulation (Basic)
General
Net and Coupling
Special Void
Output SPICE Circuit
Report
Simulation (Advanced)
Electric Models
Mesh
Nets and Shapes
Field Solver Engine
Change the 'Mesh' options in XtractIM
Maximum Mesh Edge Length
0.99
mm
Reset
This is the constraint on the maximum length of the triangles in the mesh for finite element simulation in the field domain. The default value is obtained from the package size.
Mesh quality and coarse option
Simplify the geometry to improve mesh quality
Coarse Mesh
This option is used when the user would like to run the simulation with a coarser mesh which means a mesh with less nodes. The size of the mesh will be automatically adjusted. The option may lead to less accurate result and is not recommended unless a normal simulation runs out of memory.
Default
Apply
OK
Cancel


Options
File
General
File Manager
Save Options
Hotkeys
Layout
Grid and Unit
View
Processing
Trace
Error Checking
3D Layout View
Display
Quality
Simulation (Basic)
General
Net and Coupling
Special Void
Output SPICE Circuit
Report
Simulation (Advanced)
Electric Models
Mesh
Nets and Shapes
Field Solver Engine
Change the 'Nets and Shapes' options in XtractIM
Net Options
Filter signal nets
If there are too many signal nets in the design, those far away from the ones of interest can be turned off automatically to accelerate the simulation.
Shape Options
Consider coupling between field domains through narrow gaps
Detect and model the coplanar traces coupling with field domains
Default
Apply
OK
Cancel



- Update Extraction Frequency

Format: sigrity::update ExtractionFreq {Value}

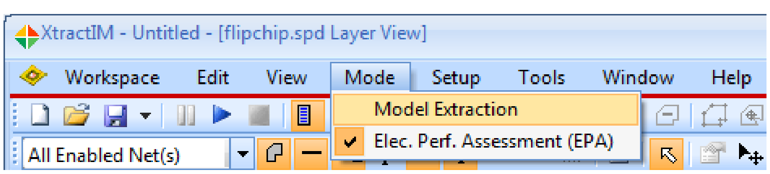


NOTE	The unit for <u>value</u> is **Hz**.

- Update Mode

Format: sigrity::update Mode {Value}

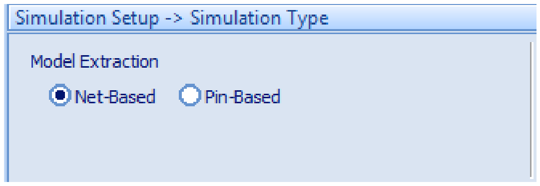
<u>value</u>: "Extraction" | "EPA"



- Update Simulation Type

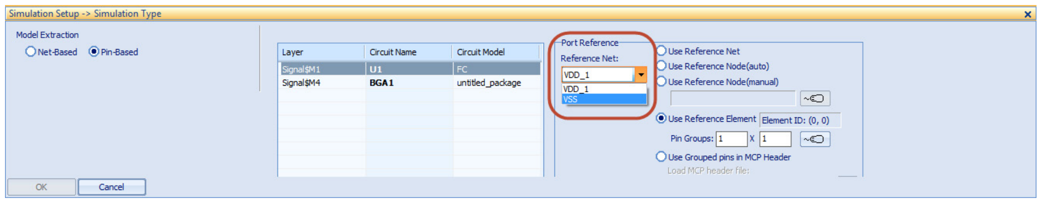
Format: sigrity::update SimType {Value}

<u>value</u>: "Net-based" | "Pin-base"



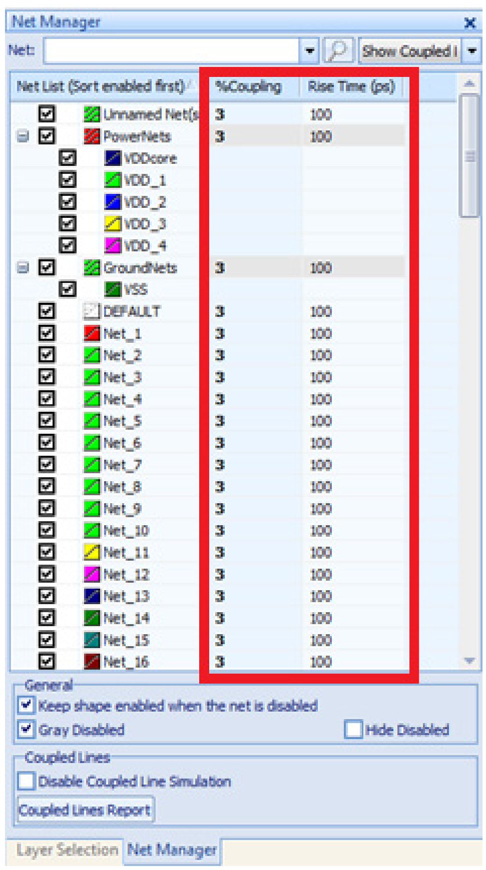
- Update Reference Net

Format: sigrity::update RefNet {Net name}



- Update Coupling

Format: sigrity::update Cpl -risetime {number} -percent {number} -all –group{power, ground, signal, unnamed}



DOING SIMULATION TCL

Format: sigrity::begin simul

Creating Report TCL

Format: sigrity::do GenReport -template {File Name Path}

Format: sigrity::save Report –Filename|F {New File name Path}

Electrical Performance Assessment (EPA) TCL

Format: sigrity::update PGAnalysis -inductanceAndCapacitance|i {0-1} -bbandImpedance|b {0-1} -freq|f {Value in GHz} -groupedPinProps|g {0-1} -dcResistance|d {0-1} -loopInductance|l {0-1} -perPinRLSide|p {0-2} -pinGroupX|x {Value} -pinGroupY|y {Value} -nets|n {Net names} -all

Format: sigrity::update SignalAnalysis -impedance|i {0-1} -coupling|c {0-1} -mutualLC|m {0-1} -loss|l {0-1} -freq|f {Value in GHz}

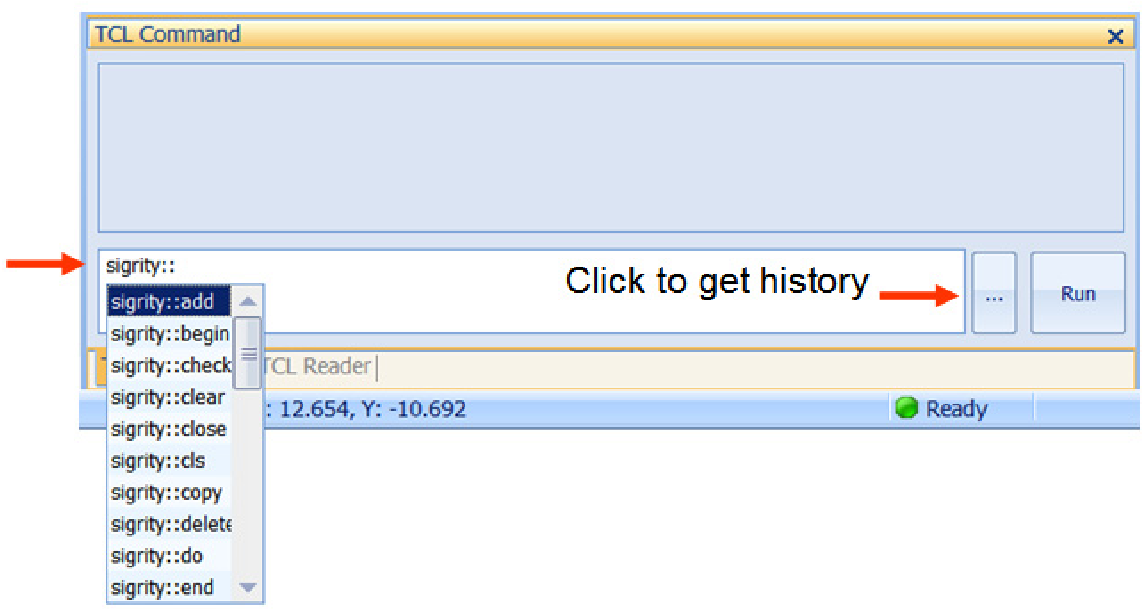
Format: sigrity::update CurrentAnalysis -checkCurrentDensity|c {0-1} -nets|n {Net names} -sinkCurrent|s {Value in A} -all

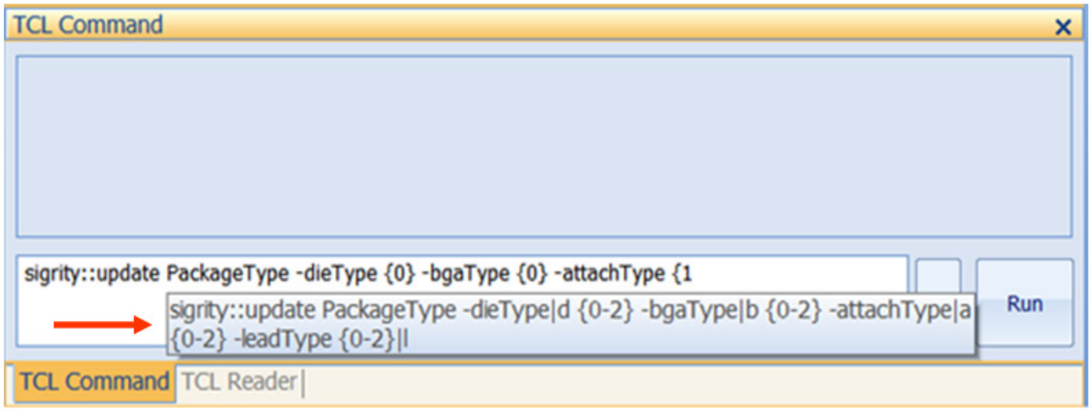
User-Friendly Design

In the **TCL Command** window, three user-friendly functions are designed.

You can:

- Choose TCL command with the same keyword from the pull-down menu
- Click  to get the TCL command history
- Refer to the auto-tips presented when you are typing the TCL command




TCL Command
sigrity::update PackageType -dieType {0} -bgaType {0} -attachType {1
sigrity::update PackageType -dieType|d {0-2} -bgaType|b {0-2} -attachType|a {0-2} -leadType {0-2}|l
Run
TCL Command
TCL Reader

Chapter
9

Error Checking Your Files

Cadence provides a number of tools to help error check your files before running a simulation. Some file errors can be hard to find. For example, you may think a trace is connected to a via — they appear overlapped with each other — but actually, the nodes of the trace and the via may not be connected.

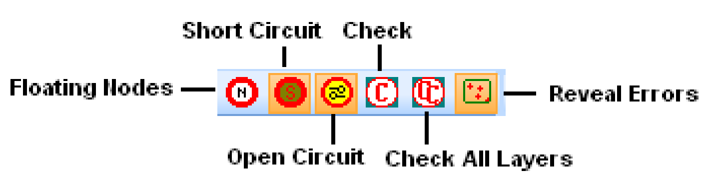
Using the error checking tools of the software, you can easily spot these kinds of drawing problems. Another kind of error is related to our internal computation models and their need to numerically discretize the geometries.

USING THE ERROR CHECKING TOOLBAR

The Error Checking Tools can assist you in finding different types of warnings and errors. Whenever a problem is detected during error checking procedures, an error or warning symbol appears in the problem area.

Error Symbols

The error symbols are similar to the button icons in the toolbar. There are four types of warnings and two types of errors.



Display the Error Check Toolbar

Select

View > Toolbar > Checking

UNDERSTANDING THE OUTPUT WINDOW

The Output window allows you to view warnings and errors at a glance whenever you open a .spd file. These tabs are located located at the left-side of the lower window.

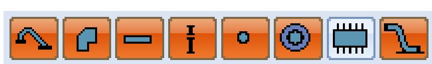
- **Mesh Errors** — Lists all the GUI related errors that you can use the Error Checking toolbar to find. This tab lists all the warnings and errors that the application finds.
- **Miscellaneous** — Lists all the errors inherent in a given file, such as an incomplete partial circuit definition or layers with a thickness of **0**.
- **Variables Check** — Lists all the variables checked.

To display the Output Window, select

View > Output Window

Check for Warnings & Errors

1. Select which package elements you want to display or hide. Choose from:
   - Nodes
   - Pads
   - Shapes
   - Traces
   - Vias
   - Wirebonds
2. Use the bottom buttons of the Layer Selection dialog.



3. Choose the types of warnings and errors that you want to find.

   Via Placement and Node Placement errors are the default choices.

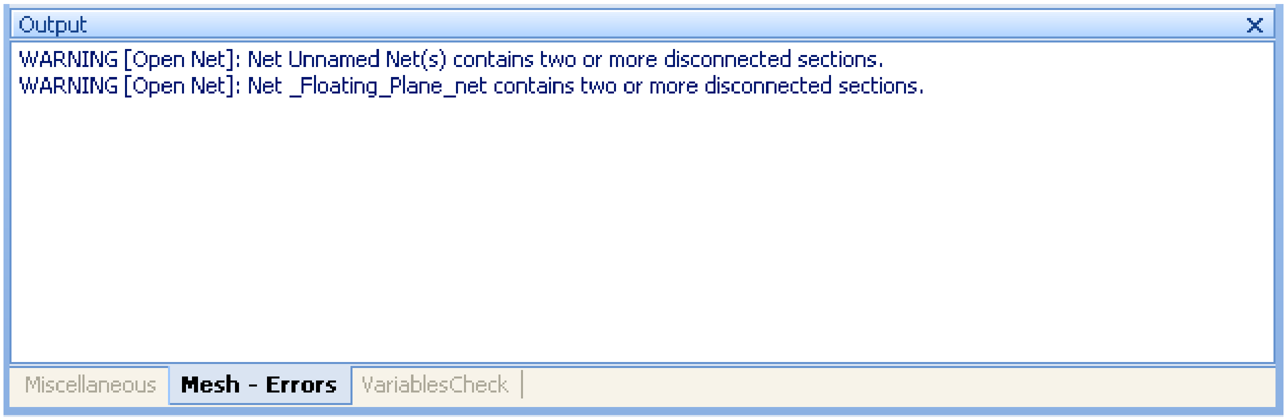
4. Press  to check for errors on the active layer.
5. Press  to check for errors on all layers.

   Warnings and errors found are marked with symbols similar to the buttons on the Checking Toolbar. These errors are listed in the **Output Window** and are marked in the Layer View area.

6. Double-click on any error that you wish to view in the **Output Window**. The Layer View window zooms into the area where the error is located.
7. Correct any errors or warnings.

NOTE!	All errors must be corrected prior to simulation.

Mesh Errors Listed in the Output Window



Check for Short Circuits

This feature lets you check for short circuits in your simulation. Short circuit warnings are displayed using a **yellow** icon. There are three kinds of Short Circuit Nodes:

- Package objects of different nets are connected together.
- Package nodes of different nets are linked to the same circuit.
- A port's positive and negative terminals connected to the same net.

NOTE!	For this type of checking, objects or nodes of unnamed nets are treated as if they belong to the same net, and this net is different from any other net.

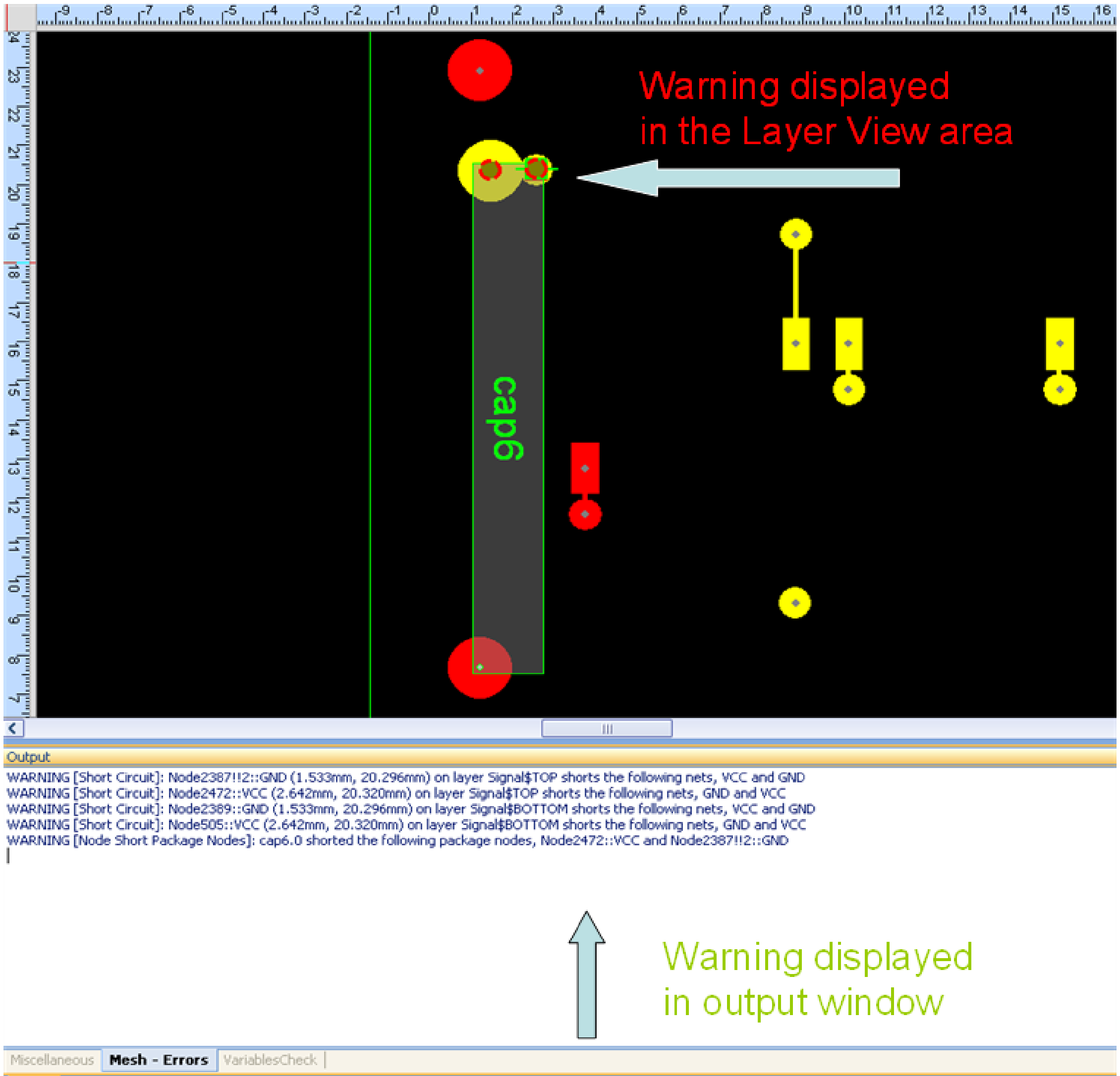
1. To start checking select

   Tools > Check > Check Activated Layer

   or

   Check All Layers

Any warnings found are listed in the Output Window and are shown in the Layer View area.



2. Double-click on any warning in the **Output** window. The Layer View window zooms into the area where the short circuit is located or the Circuit Manager is displayed.

Chapter 10

Case Examples

This chapter outlines some case examples for various sections of the XtractIM User's Guide.

EXTENDING NODES AND VIAS

The***Extending Nodes and Vias*** illustration represents the nodes and vias that are to be extended vertically.

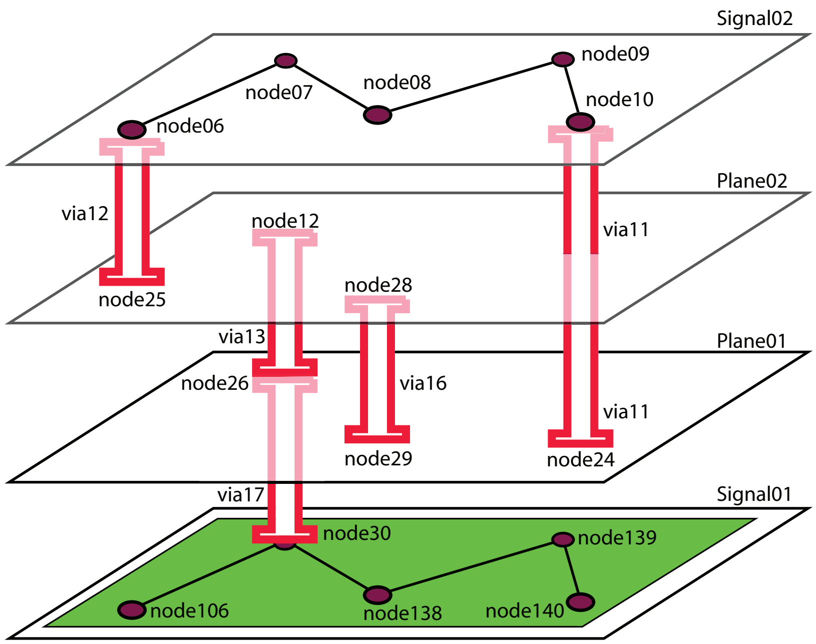
- Nodes: node06, node07, node08, node09 and node10.
- Vias: via12, via17, via13, via16 and via11.
- Via 12 is terminated at node06 on layer Signal02 and node25 on layer Plane02.
- Node07 does not extend vertically through a via but, via13 is in vertical proximity (to node07) as is via17.
- Via17 and via13 share node26.
- Node28 is the upper node of via16.
- Node29 is the lower node which is in vertical proximity to node138 of layer Signal01.
- Via11 is included to complement the example.

Extending Nodes and Vias

The purpose is to insert vias in the following manner:

Isolated node objects extended vertically by the insertion of vias.

Where a via already exists, the via is extended.



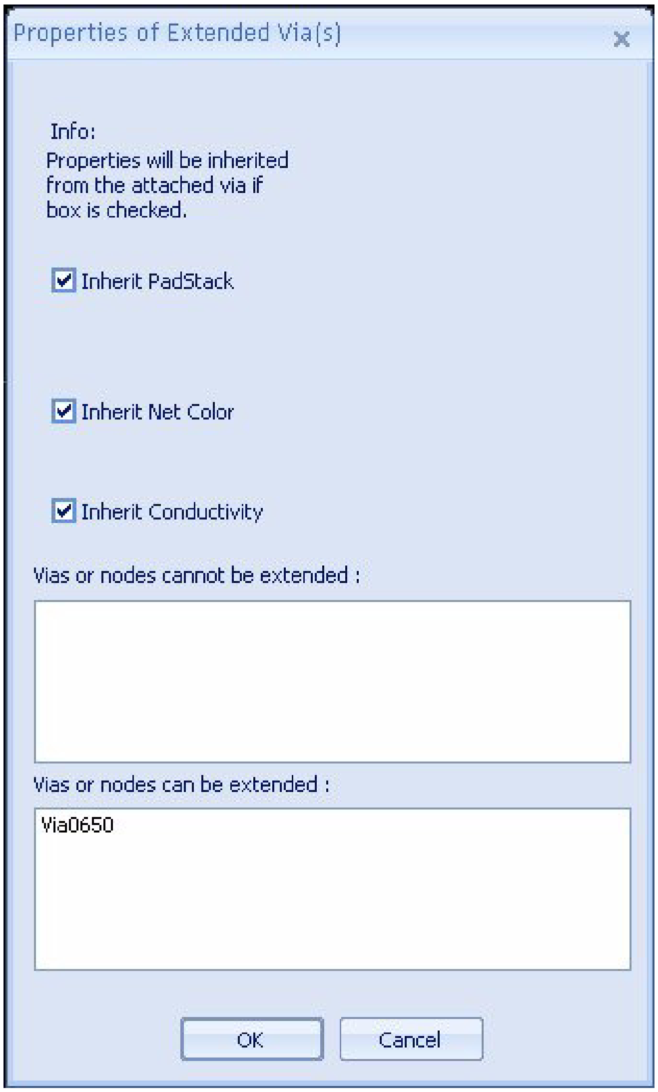
Refer back to this illustration as you study the examples in Case 1 and Case 2.

CASE 1

The yellow via in the Via Extension window shows we want to extend nodes selected from layer Signal02 to layer Signal01.

Only Node09 can be extended as indicated.

All other nodes have existing vias blocking the extension.



CASE 2

The yellow via shows we want to extend all nodes and vias from layer Signal02 to layer Plane02.

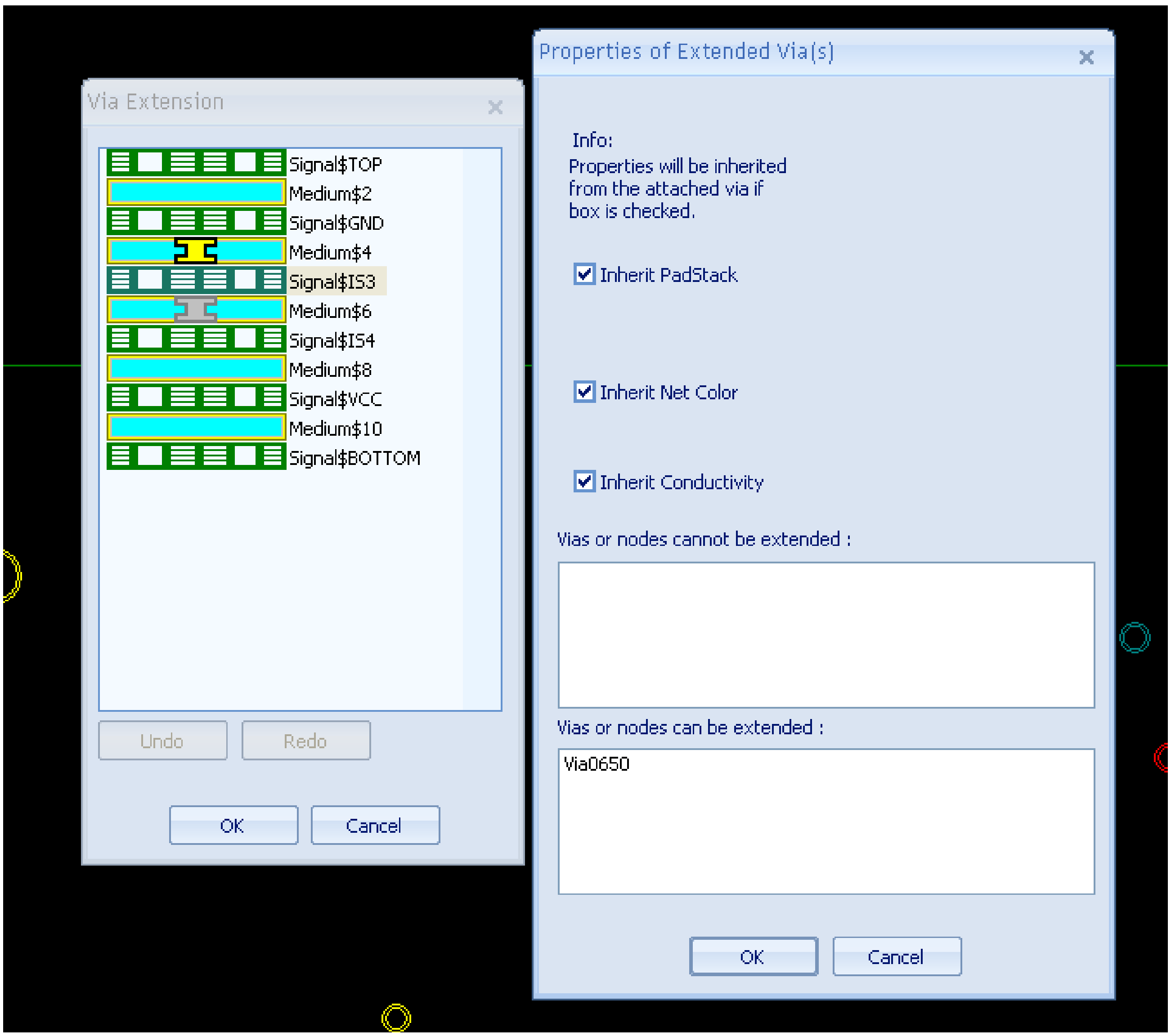
Nodes 9, 8, and 7 can be extended.

Vias 13 and 16 can be extended.

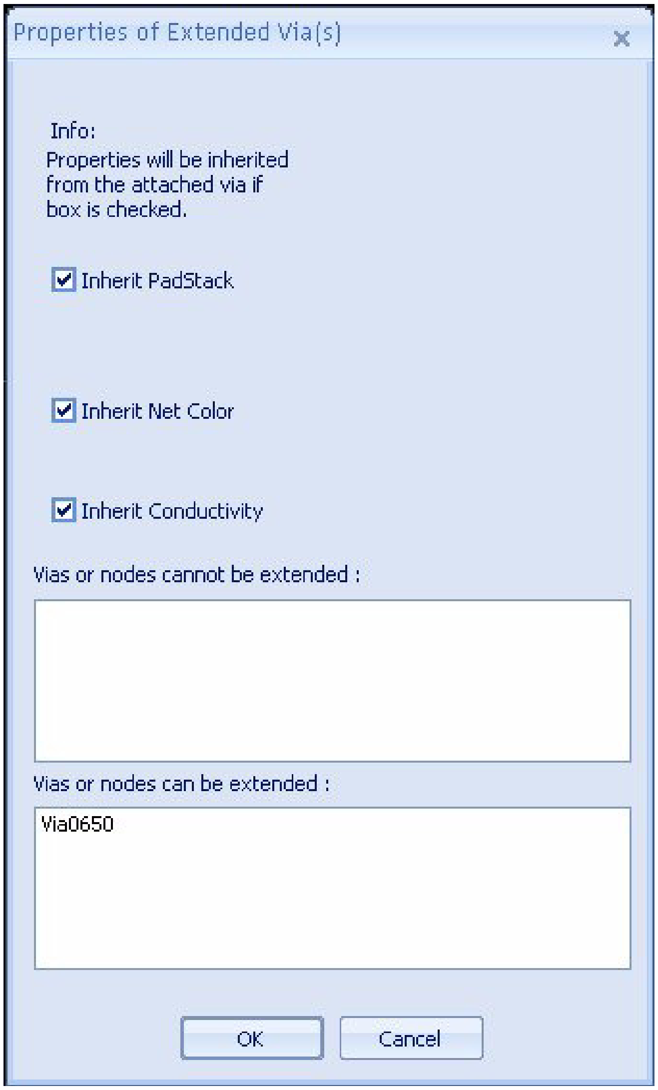
Vias 12, 17 and 11 cannot be extended.

Existing vias are blocking nodes 6 and 10.

Via17 is blocked by via13.



Propterties of Extended Vias Window



Chapter

11

Quick GUI Keys

The Quick GUI Keys are listed and described in the following table.

GUI Key Features

Feature	Keys to Press	Notes
Active layer selection	Up and Down Arrows	Use with the Layer Selection dialog.
Close windows	ESC	Closes any open dialog box that is currently active.
Finding objects, opening the Find dialog box	Ctrl + F	Works when the Layer View window is active.
Show/hide shapes	F7	Works with either Layer View or 3D View windows.
Area zooming	F2	Zooms into an area. Use the mouse to select what area you want to magnify.
Zoom back	F3	Zooms out of an area.
Zooming in	F4	Magnifies a given area. Click the mouse to zoom into an area.
Zooming out	F5	Zooms out of a given area. Click the mouse to zoom out of an area.
Deleting objects	Delete key	Works when the Layer View window is active, select an object, then press the delete key.
Circuit linking “turbo”	Up, Down, Right and Left	Use these keys to iterate through the partial circuit and component name lists and to navigate around the Component Manager.

Feature	Keys to Press	Notes
Create new .spd file	Ctrl + N	XtractIMI must be invoked and the workspace must be empty.
To open a .ximx file	Ctrl + O	XtractIM must be invoked and the workspace must be empty.
To print window contents	Ctrl + P	Use with the Layer View or 3D View window active.
To save the .spd file	Ctrl + S	Use with the Layer View or 3D View window active.
Object Outline Display	Ctrl + Shift + O	Object outlines are toggled.

Chapter 12

Pin Mapping

Pin mapping is used to indicate which power and ground buses a given driver, receiver, or terminator is connected. This chapter covers how to use pin mapping in XtractIM.

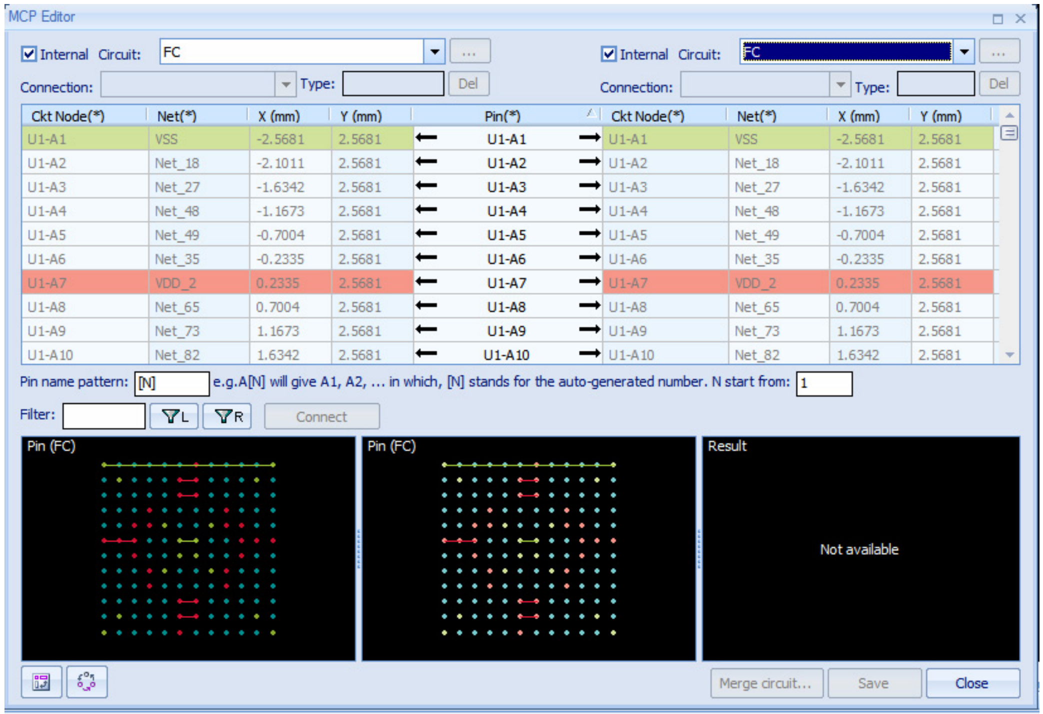
Pin Mapping Dialog

The **Pin Package Nodes Match** dialog shows the result of name matching and coordinate matching when a partial circuit includes an MCP or CPM sub-circuit. When the dialog opens and name matching is failing, you can match coordinates with the default tolerance automatically one time.

When names are matched, the controls used in the manual match are **gray**.

Function	Description
Position Tolerance	The tolerances are used in coordinate matching.
Angle Tolerance	The tolerances are used in coordinate matching.
Default	Set the tolerances to default values.
Match	Play coordinate match.
Detail	Show the result of name matching and coordinate matching.
Use manual match	Select two pairs of points to coordinate match.
Flip pins	Flip the pins to match coordinate.
Coord Match	Select the result of coordinate match as the final result.
Name Match	Select the result of name match as the final result.

Pin Package Nodes Match Dialog



Index

Symbols

Numerics

A

B

C

D

E

T

U

V

W

X

Y

Z