# cādence<sup>®</sup>

# **XtractIM User's Guide**

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# **Table of Contents**

	Table of Contents	i
1	Introduction	1
	System Requirements	1
	How to Use This Guide	
	Additional Documentation	1
	Conventions Used in This Guide	2
		2
	How to Contact Technical Support	2
2	Learning the Basics	3
	Using XtractIM	3
	The Workflow Pane	3
	Using the Workflow Pane	4
	Show and Hide Icons	5
	Net-Based Extraction on Single-BGA Package	
	Net-Based Extraction on Stacked-BGA Package	7
	Pin-Based Extraction	
	Working on a Layout File	
	.spd File Format	10
	File Manager	10
	File Folders	10
	File Name Pattern	11
	Folder Browser	11
	Prepare for Simulation	11
	Save Workspace Files	12
	Save a Workspace	12
	Load Workspace	
	Run the Simulation and View Results	13
3	Learning the Workspace	15
	XtractIM Workspace	15
	New Workspace	16
	Workflow Pane	17
	Editor Pane	17
	The Menu Toolbars	
	Workspace Toolbar	
	Layout Toolbar	19
	Undo and Redo Buttons	19
	Zoom Functions	19
	The Select Toolbar	20
	Select an Object	
	The Object Toolbar	
	Cut Area Rules	
	Shape Toolbar	

	Error Checking Toolbar	
4	Working with SPD Layout	23
5	XtractIM Simulation of a Single BGA Package	25
	About XtractIM	
	Toolbar Icons	
	Simulation Setup	
	Setup the Package Simulation	
	Select Package Type	
	Setup Circuits	
	Setup Stackup	
	Setup Bump	
	Setup Flip-chip Package	
	Setup Nets	
	Set With Default Parameters	
	Rise Time and % Coupling	
	Show Coupled Lines	
	Extraction Frequency and Capacitance/Inductance Output Control	40
	Set Threshold for Exporting Mutual Terms	41
	Save the Workspace and Layout File	41
	Using the Save as Option	43
	Observe and Save Results	43
	Capacitance Matrix	44
	RLC Per Net View	44
	Self Terms View	45
	Mutual Terms View	46
	Summary of the Extracted Results	46
	SPICE and IBIS Models	
	SPICE / IBIS Model Result View	
	Pin Model: Excel Format	
	RLC Distributions	
	Segment RLC	
	Save Results	
	Output Files	
	Load in Saved Results	
	Batch Mode Simulation.	
	Saved Output Files	
	Package Setup	
6	XtractIM Simulation of a Stacked BGA Package	59
	Simulation Setup	59
	Setup the Package Simulation	60
	Select Package Type	61
	Setup Circuits	63
	Setup Stackup	64
	Setup Bumps	65
	Setup Solder Ball	66
	Setup Nets	66

	Extraction Frequency and Capacitance / Inductance Output Control	
	Set Output Factors	
	Save Workspace and Layout File	71
	Save Workspace File	71
	Save Layout File	
	Run the Simulation	
	Observe and Save Simulation Results	
	Display Results	
	Circuit Topology	
	Display Results Example	
	Summary of the Extracted Results	
	Brand RL and Total C	78
	Save Results	78
	Output Files	79
	Load in Saved Results	80
	Batch Mode Simulation	80
	Saved Output Files	
7	XtractIM Pin-Based Simulation of a BGA Package	83
	Simulation Setup	
	Single-BGA Package	
	Stacked-BGA Package	
	Setup Simulation Type	
	Setup Extraction Frequency	
	Setup Threshold for Exporting Mutual Terms	
	View / Export Results	
	SPICE Model	
8	TCL Command Support for Workspace Setup	89
	Introduction	89
	Setting up TCL	89
	Doing Simulation TCL	94
	Creating Report TCL	95
	Electrical Performance Assessment (EPA) TCL	95
	User-Friendly Design	
9	Error Checking Your Files	
		07
	Using the Error Checking Toolbar	
	Display the Error Check Toolbar	
	Understanding the Output Window	
	Check for Warnings & Errors	
	Check for Short Circuits	
10	Case Examples	103
	Extending Nodes and Vias	
	CASE 1	105
	CASE 2	

### XtractIM User's Guide 16.6

	Propterties of Extended Vias Window	
11	Quick GUI Keys	109
	GUI Key Features	
12	Pin Mapping	111
	Pin Mapping Dialog	
	Pin Mapping Dialog Pin Package Nodes Match Dialog	

# Chapter

### Introduction

Welcome to the XtractIM User's Guide. This manual is designed to give you a brief introduction to the XtractIM application by providing real life examples and demonstrations so you can understand some of the basic concepts of the XtractIM application.

### SYSTEM REQUIREMENTS

Please refer to *Installation Guide* to check the system requirements.

### How to Use This Guide

This guide provides descriptions, demonstration examples and step-by-step instructions on how to get the desired results with the XtractIM tool.

### **Additional Documentation**

In addition to this document, refer to the following documentation for additional information.

- *.spd File Format Reference Guide* explains the format of the Sigrity .spd file. Files must either be created as a .spf file or translated from another format into .spd file format.
- *Translators User's Guide* explains how to translate layout data contained in various file formats into the Sigrity .spd file format.

### **CONVENTIONS USED IN THIS GUIDE**

CONVENTION	Use
Bold	GUI text, special names, terms (window names, buttons, menus, etc.)
Arial	Examples
>	Menu hiearchy

### How to Contact Technical Support

We are committed to helping you in using XtractIM. If you have any questions, contact the <u>Cadence</u> <u>Online Support</u>.

# Chapter 2

### **Learning the Basics**

This chapter describes the basics of the XtractIM application.

### **USING XTRACTIM**

- 1. Load a layout file (also called a package file).
- **2.** Create a Workspace.
- 3. Save the workspace for future use. You'll use this workspace to prepare for the simulation.
- Run the simulation. 4.
- 5. View the results.
- Repeat theses steps, as needed, to change your settings. 6.
- 7. Run the simulation as many times as you need.

### **The Workflow Pane**

The workspace is made up of the Workflow pane and the Layout Area. All the workflow tasks are listed in the Workflow pane. Tasks of the same type are sorted and listed together. When a task is clicked, details associated with that task appear in an Editor pane.

- Check results
- Modify a design ٠
- Report results.
- ٠ Run a simulation
- Set up a simulation .



Editor Bar

### Status Bar

### Layout Selection Window

- Editor pane A spreadsheet. Users can easily input information into the pane for simulation setup or check the simulation results in the pane.
- Layout Selection Window Controls the active layer, displayed layers and the object display on or off.
- Layout Window Edit your layout file.
- Status Bar Shows the version information, the current X-Y coordinates of the cursor and the simulation progress.
- Tool Bar Quick access icons for common XtractIM commands.

### **Using the Workflow Pane**

The Workflow pane includes Manage Workspace, Package Setup, Simulation Setup, and View and Export Results.

- **Layout Area** Displays the configuration of the layout file.
- Workflow Tasks For different packages vary slightly.

### **Show and Hide Icons**

When you click on the **Show** and **Hide** icons in toolbar, the selected item is displayed or hidden.

🛟XtractIM - Win	ebond.	.xml ·	- [wirebo	ond.spd L	ayer Vie	w]	
🧇 Workspace E	Edit	View	Setup	Tools	Window	Help	
🗋 💕 🛃 • 🛛				🖬 i 💕	19 -	(° - 1	-7
Toggle	Work	flow	Pane				
		Tog	ggle Edit	or Pane			

**Net-Based Extraction on Single-BGA Package** 

Workflow Task	Description
Manage Workspace	Load workspace and/or layout file.
Load Workspace	Load in an existing workspace.
Load a New/Different Layout	Create a new layout file or remove the current layout file and load in a desired layout file.
Package Setup	Set up all basic parameters for simulation.
Package Type	Wirebond or Flip-chip, Single-BGA or Stacked-BGA.
Circuit	Select/deselect Die circuit or Board circuit.
Stackup	Setup the Stackup parameter of a package.
Bumps	Seup Bumps parameters for a Flip-chip package.
Solder Ball	Set Solder Ball parameters.
Nets	Select the desired nets for RLC extraction.
Simulation Setup	
Module	IBIS/RLGC or Optimized Broadband.
Simulation Type	Choose from Net-based and Pin-based.
View / Export Results	
Summary	View the RLC matrix, the minimum and maximum R, L, C values.
SPICE/IBIS Model	View the SPICE model, IBIS .pkg model and IBIS .ibs Pin model.
RLC Per Net	2D display of R, L and C value for each net.
RLC Distributions	3D display of R, L and C full matrix values.
Segment RLC	View segment RLC on each metal layer.
RLC vs.Net Length	2D Display of R, L, and C, vs. net length for signal nets.

Workflow Task	Description
Crosstalk	View the near-ended and far-ended crosstalk among signal nets.
Save Results	Save the result on hard disk. A text file and a binary file with the extension .xim will be saved.
Load Results	Load in the saved results on display.

### Net-Based Extraction on Stacked-BGA Package

Workflow Task	Description
Manage Workspace	Load workspace and/or layout file.
Load Workspace	Load in an existing workspace.
Load a New/Different Layout	Create a new layout file or remove the current layout file and load in a desired layout file.
Package Setup	Set up all basic parameters for simulation.
Package Type	Wirebond or Flip-chip, Single-BGA or Stacked-BGA.
Circuit	Select/deselect Die circuit or Board circuit.
Stackup	Setup the Stackup parameter of a package.
Bumps	Seup Bumps parameters for a Flip-chip package.
Solder Ball	Set Solder Ball parameters.
Nets	Select the desired nets for RLC extraction.
Simulation Setup	
Module	IBIS/RLGC or Optimized Broadband.
Simulation Type	Choose from Net-based and Pin-based.
View / Export Results	
Summary	View the minimum and maximum R, L, C values.
SPICE Model	View the SPICE model, RLC for each path (Die-toBGA1, Die-to-BGA2, BGA1-to-BGA2).
Branch RL	View each branch R and L of the generalized T-topology circuit.
Save Results	Save the result on hard disk. A text file and a binary file with the extension .xim will be saved.
Load Results	Load in the saved results on display.

### **Pin-Based Extraction**

Workflow Task	Description
Manage Workspace	Load workspace and/or layout file.
Load Workspace	Load in an existing workspace.
Load a New/Different Layout	Create a new layout file or remove the current layout file and load in a desired layout file.
Package Setup	Set up all basic parameters for simulation.
Package Type	Wirebond or Flip-chip, Single-BGA or Stacked-BGA.
Circuit	Select/deselect Die circuit or Board circuit.
Stackup	Setup the Stackup parameter of a package.
Bumps	Seup Bumps parameters for a Flip-chip package.
Solder Ball	Set Solder Ball parameters.
Nets	Select the desired nets for RLC extraction.
Simulation Setup	
Module	IBIS/RLGC or Optimized Broadband.
Simulation Type	Pin-based.
View / Export Results	
Summary	View the minimum and maximum R, L, C values.
SPICE Model	View the SPICE model.

### Working on a Layout File

Working on layout files includes working with package layers, objects, nets, vias, traces, shapes, nodes, wirebonds, stackups, etc.

1. Open the Attach Layout File window.

Attach Layout File	×
Apply current workspace setup	
Please choose the type of layout to load	
<ul> <li>Load an existing SPD file</li> </ul>	
O Load an existing DXF file	
OK Cancel	

- 2. To apply the current workspace setup, click Apply current workspace setup
- To load a desired SPD layout file, click
   Load an existing SPD file
- To load a desired DXF layout file, click
   Load an existing DXF layout

### .spd File Format

The layout file is in Sigrity .spd file format. As part of the Sigrity family of products, XtractIM includes file format translators which translate the following file formats in .spd files for simulation.

- Cadence .brd, .mcm, and .sip files
- Cadvance .dbr files
- Mentor BoardStation ASCII design outputs files
- Mentor Expedition .hkp files
- Mentor PADS .asc files
- P-CAD .pcb files
- Zuken CADStar & Visula .rif files
- Zuken CR5000 .pcf, .ftf, and .mrf files

### **File Manager**

You may specify the directories where output files of different types are placed.

Tools > Options > Edit Options... > File Manager

File	•	
General File Manager		Change the 'General' options in XtractIM
Save Options Hotkeys		Automatically Save The Project File
Layout	$\odot$	
Grid and Unit View Processing Trace		Every 0 minutes Before simulation starts
Error Checking		Save the project file automatically to protect against undesired modifications or unexpected exits. XtractIM allows simulation without saving the file, the auto project file saving is helpful in keeping the
3D Layout View	$\bigcirc$	consistency between the design and the result.
Display Quality		
Simulation (Basic)		
General Net and Coupling Special Void Output SPICE Circuit Report		
Simulation (Advanced)		
Electric Models		
Mesh		
Nets and Shapes		

**File Folders** 

- **Black items** Editable. The default value of the temporary folder is the operating system's temporary folder. Other default values include the directory where the current case is located.
- Gray items Not editable. Indicate current working paths.

### **File Name Pattern**

The names of the output files are customized.

[W]	Workspace Name			
[L]	Layout Design Name			
[Y]	Year			
[M]	Month			
[D]	Day			
[h]	Hour			
[m]	Minute			
[s]	Second			

### **Folder Browser**

The Folder Browser goes through files in special folders. Select:

View > Pane > Folder Browser

Folder Browser	
Folder Type	Path
Tool bin folder	D:\Program Files\Sigrity\SpeedPKG 11.0\Progra
Install folder	
Circuit library folder	
Material library fo	
Script library folder	
Template library	
Tool output folder	
Tool log folder	
Tool temp folder	C:\DOCUME~1\zqfang\LOCALS~1\Temp
Case folder	D:\Program Files\Sigrity\SpeedPKG 11.0\XtractI
Case output folder	D:\Program Files\Sigrity\SpeedPKG 11.0\XtractI
Case log folder	D:\Program Files\Sigrity\SpeedPKG 11.0\XtractI
Case temp folder	C:\DOCUME~1\zqfang\LOCALS~1\Temp
S model checkin	D:\Program Files\Sigrity\SpeedPKG 11.0\XtractI
Layout folder	D:\Program Files\Sigrity\SpeedPKG 11.0\XtractI

Click on a folder in the left side of the window. The folder contents are displayed in the right side of the window.

Double-click on a file in the right list to open the file. A pop-up window displays file information the cursor hovers over the filename.

NOTE!

Currently, Sigrity analysis tools do not offer any folder type containing multiple items.

### **PREPARE FOR SIMULATION**

To prepare for the simulation you need to set all the parameters in the Package setup.

- × Symbol next to an item is a reminder that this item has not been set.
- Symbol next to an item means it has been set.
- 1. Click on an item under **Package Setup** in the Workflow pane. Our example shows Solder Ball selected and displayed.
- **2.** An Editor pane opens across the bottom of the workspace. You can easily input all information for the Solder Ball model.

Package Setup -> S	Package Setup -> Solder Ball X							
Layer Name	Circuit Name	Dmax (mm)	D1 (mm)	D2 (mm)	HT (mm)	Conductivity (S/m)	Medium Thickness (mm)	Solder Ball Model
Solderball01	BGA1	0.5	0.4	0.4	0.4	5.8e7	0.05	
								H D2→H D1→H HT HT HT Ground
ОК	Cancel							

### **Save Workspace Files**

After having gone through each step in the Package setup, you can save the workspace in **\*.ximx format**. This **\***.ximx file includes the **.spd file name** and all the settings in the Package setup.

### **Save a Workspace**

- To save a newly created workspace, select Workspace > Save
- **2.** Enter a name for the new workspace.
- **3.** To save the existing workspace under a different name, select

Workspace > Save as

**4.** Enter the new name.

### **Load Workspace**

**1.** To load an existing workspace and its associated layout file, select

Load Workspace

**2.** If the associated layout file does not exist in the same directory as the workspace file, the following window opens.

Open Layout File	)	? ×
Look in:	🗁 Single-Die_Sample_files 🔹 🌀 🎓 📰 🗸	
My Recent Documents	Contraction Temp	
Desktop		
My Documents		
My Computer		
	File name: pkg_flipchip_600.spd	<u>O</u> pen
My Network	Files of type: Layout File (*.spd)	Cancel

**3.** Choose the desired layout file from the list shown in this new window. For example: pkg\_flipchip\_600.spd.

### **RUN THE SIMULATION AND VIEW RESULTS**

1. Click on the **Start** icon *i* in the Toolbar to run the simulation.

XtractIM only extracts RLCG for the net which has at least one pin at the Die side and at least one pin at the board side.

- **2.** At the beginning of the simulation, if some nets have Die-Board mis-match, a pop-up window asks you to select the next action.
  - **Continue** Continue the simulation.
  - More Information Lists all mis-matched nets.

• **Stop** — Cancel the simulation.

Νοτε	If 30 seconds pass and you have not made a choice, by default, the simulation continues.
------	--

- **3.** Choose **More Information** to investigate mis-matched nets. The information lets you see whether it is a special design or a defective design. You can then decide whether or not to proceed with the simulation.
- 4. To view the results in each selection., select

View > Export Results

# Chapter

## Learning the Workspace

This section describes how to use the Workspace.

### **XTRACTIM WORKSPACE**

When you launch XtractIM for the first time, the **Main Window** opens. From this window, you can create a new workspace. Select

Workspace > New



### **New Workspace**

The new workspace is made up of three major areas:

- Workflow pane Left side of the screen.
- Layout Area Large blank area on the right side of the screen
- Layer Selection and Net Manager Pane Right side of the screen.



### **Workflow Pane**

All Workflow tasks are listed in the Workflow pane. From left to right, the samples show the workflow for Single-BGA net-based, Stacked-BGA net-based, and pin-based extraction, respectively.

Click on the tasks to expand or collapse them. When a task is expanded, details associated with that task appear in an Editor pane, across the bottom of the screen.

When you move the mouse onto a task, a tool-tip appears and provides associated information.

Single-BGA net-based	Multi die or Stacked-BGA net-based	Pin-based
Verkflow: XtractIM 🛛 🗙	Workflow: XtractIM 🗙	Workflow: XtractIM
Model Extraction 🔗	Default 🔗	Default
Manage Workspace 🛛 🙆	Manage Workspace 🕜	Manage Workspace
Load Workspace Load a New/Different Layout	Load Workspace	Load Workspace
Package Selup 🙆		
Package Type: Flip-Chip	Package Secup	Package Setup
✓ Circuits	✓ Circuits	
Stactup	🗸 Stackup	Stackup
Solder Ball	V Bumps	V Bumps
Nets	🖌 Solder Ball	🗸 Solder Ball
Simulation Setup	🗸 Nets	Nets
Module: IBIS/RLGC	Simulation Setup 🕜	Simulation Setup 🛛 🙆
Simulation Type: Net-Based	Madule: IBIS/RLGC	Module: IBIS/RLGC
View/Export Results 🛛 🙆	Simulation Type: Net-Based	Simulation Type: Pin-based
Summary	View/Export Results 🛛 🙆	View/Export Results 🛛 🙆
SPICE/IBIS Model	Summary	Summary
RLC Per Net	SPICE Madel	SPICE Model
Segment PLC	Branch RL	Save Results
RIC vs. Net Length	Save Results	Load Results
CrossTalk	Load Results	Puetoniza Workflow
3D View	Customize Workflow	CUSCOMIZE WORKHOW
Histogram View		
Save Results		
Load Results		
ustomize Workflow	5	

#### **Editor Pane**

When you click on a task, the corresponding detail information of the task is displayed in the **Editor** pane (the horizontal section along the bottom of the screen).

- **1.** Input information into the pane.
- 2. Highlight an item listed in the Editor pane.
- 3. View the item in the Layer View window.

### **THE MENU TOOLBARS**

**1.** To see the all the toolbars available to you, select:

View > Toolbars

- **2.** Use the Status Bar to view:
  - Current X, Y coordinates of the cursor
  - Simulation progress
  - Version information
- 3. Use the commands on the pull-down menus.
  - Check results
  - Modify a design
  - Report results
  - Run the simulation
  - Setup installation



**NOTE** Once a tool is selected, it remains in use until you select another tool. Right-click to deselect the tool and return to non-drawing mode.

### **Workspace Toolbar**

The Workspace Toolbar provides quick access to common XtractIM commands. Use this easy access to perform some of the more basic functions of XtractIM.



### **Layout Toolbar**

The Layout Toolbar also allows you to perform some of the more basic functions of XtractIM.

### **Undo and Redo Buttons**

You can undo or redo any action that you have performed for package editing. The Undo and Redo buttons allow you to choose from the last few actions you have performed.



### **Zoom Functions**

Use the zoom functions to view various parts of the package.

- 1. Select Area to display a magnified view of a rectangular area selected by mouse dragging.
- 2. Zoom in to a selected area.
- 3. Zoom-out to display the window contents in reduced size.
- 4. Select Fit to display the entire curve graph or package in the window.



You can use two hot keys for the zoom-in and zoom-out function: F2 for area zoom in; F3 for zoom-out.

### **The Select Toolbar**

At times, the object you want to select for a procedure is so close to another object on a layer that it is difficult to select the object you want. A special toolbar exists to help you select specific objects.

### Select an Object

- 1. Click on the button for the type of objects you want to select.
- **2.** Select an operation button.
- **Delete** Move the cursor to the objects of interest. Left-click. Hold and drag to select an object or objects. Click the **Delete** key to remove objects.
- Move Move the cursor to the objects of interest. Left-click. Selected objects move.
- **Property** Move the cursor to the object of interest. Left-click to select an object. Click on the **Property** button to see the **Property Report** for the object.
- Select Move the cursor to the objects of interest. Left-click. Hold and drag to select objects.
- Unselect Hold down the CTRL key. Click on the selected object.



### **The Object Toolbar**

Use the Object Toolbar to add or cut package objects (vias, shape vertices and Traces). View the different areas of this toolbar.

These buttons provide quick access to the tasks you will frequently perform.



- **Cut Objects** Cut out objects on all layers in an area that you specify. This function cuts all objects including: nodes, vias, Traces, shapes, and pads.
- Node Tools Add a node to the package.
- Trace Operations Add or split a Trace and setup a current observation.
- Via Operations Add, copy, or extend vias.

### **Cut Area Rules**

When cutting an area, the following rules apply:

- Objects are cut, regardless if the object's net is enabled or disabled.
- If a node is used in a circuit link, the node is unlinked prior to being cut.

### **Shape Toolbar**

Use the Shape Toolbar to draw and work with shapes.

Three kinds of shape tools are provided with both add and cut features:

- Box
- Circle
- Polygon

The shape tools can be applied to plane layers or patches on signal layers.



### **Error Checking Toolbar**

Use the Error Checking Toolbar to find short circuit warnings prior to running simulations.

	Open Çircu	iit Che	ck All I	Layers
Floating Nodes -	Checking	<mark>9</mark> C (	× 0	— Reveal Errors
Sh	ort Circuit	Check		

# Chapter

## Working with SPD Layout

For SPD layout settings, please refer to the common document **SPD Layout UG**. It introduces the common GUI capabilities and operations of Sigrity analysis tools.

# Chapter 5

## **XtractIM Simulation of a Single BGA Package**

This chapter takes you through the steps to use the XtractIM tool in the simulation of a single BGA (Board Grid Array) package.

### **ABOUT XTRACTIM**

XtractIM extracts the most common electrical models of IC packages according to IBIS (I/O Buffer Information Specification) as well as SPICE netlist of electrical models.

These models can be used for system-level analysis including drivers, receivers and interconnects; as well as for assessing the electrical performance of IC packages. XtractIM functionality provides the user with capability to:

- Generate IBIS package pin RLC model.
- Generate IBIS package RLC matrix model with coupling between signal, power and ground nets.
- Generate net length, DC\_R, delay of each signal net.
- Generate SPICE equivalent circuits of package RLGC models of different topologies (Pi or T), including coupling between signal, power and ground nets.
- 2D and 3D display of RLC curves and distributions, including coupling between nets.

XtractIM can handle both flip-chip packages and wirebond packages with 3D bonding wire profiles. XtractIM handles both single and stacked BGA packages.

It can extract models of full packages or selected nets of a package. The interface is compatible with data files in various formats, including UPD (Unified Package Designer), MCM, .brd, .sip, NA2, DSN and SPD.

**Related Topics** 

- The Workflow Pane
- Using the Workflow Pane
- Save a Workspace

### **Toolbar Icons**

- **Toggle Workflow pane** Workflow pane appears or hides.
- Toggle Edit pane Status Bar appears or hides.
- **Toggle Output Pane** Output Pane appears or hides.

XtractIM - Wirebond.xml - [wirebond.spd Layer View]								
۰	Workspace	Edit	View	Setup	Tools	Window	Help	
	📔 🚽 🕶				📼 i 💕	19 - 1	(° - I 🛄	-7
Toggle Workflow Pane   Toggle Output Pane								
Toggle Editor Pane								

### SIMULATION SETUP

A typical workflow in Interaction mode includes the following steps.

- Create a new workspace file or load an existing file (.ximx file).
- Open a layout file (.spd file).
- Select a package type: wirebond or flip-chip, single BGA or stacked BGA.
- Setup the circuits: select / deselect Die-circuit and Board circuit.
- Setup the Stackup: set parameters for the C4 Bump/Solderball medium layer.
- Set the Bump data if it is a flip-chip package.
- Set the Solder Ball data.
- Select the nets for extraction.
- Setup extraction frequency and capacitance or inductance output control.

### **Setup the Package Simulation**

1. Launch XtractIM.

Two icons are available: New and Open 🤷 .

The New icon creates a new workspace.

The **Open** icon allows users to load an existing workspace file.

- To create a new workspace click on the New icon; or select Workspace > New
- To load the Package Structure, click on Load a New/Different Layout

### **Related Topic**

• Working on a Layout File

### Select Package Type

1. Select a Package Type.

The default package type is Single Die, Single BGA, wirebond package.

2. Click on

Wirebond

or

Flip-chip

Our example shows the Flip-chip selected.



- 3. Click **OK** to save your selection.
- 4. Click Cancel if you want to change your selection, start over and cancel your session.

### **Setup Circuits**

1. Click on **Circuits** in the Workflow pane to setup the Circuit data for a Flip-Chip package. A new pane opens up in the left side of the workspace.



- **2.** Right-click on the desired circuit.
- 3. Select it as a **Die** circuit (or a Capacitor circuit).

XtractIM - FlipChip.xml - [pkg_flipchip_6.spd Layer View]	- 0 ×
♦ Workspace Edit View Mode Setup Tools Window Help	
	Extractor Result ▼ The time from U1 ▼ To U1 ▼ To U1 ▼
All Enabled Net(s) 🔽 🗗 📥 🖬 🕈 🔹 🗰 🐒 🕟 😭 🏎 🖓 💷 📼	▋▝▝▝▋▋▁▆▁▆▁▆▁▆▁▆▁▆▁▆▁▆▁▆▁▆▁▆▁▆▁▆
Wizard X 12 -11 -10	
	Net:
Select the Die/Component circuit from the list and click Next	Default Mode 👻
	Net List (Sort enabled first) / Interface ~
Ckt Name Ckt Model Die/doard/Lompo	
C2 Ca Select as Die circuit	V Net.62
C4 Ca Deselect as Die circuit	
C5 Ca Select as Capacitor circuit	
C7 Ca Deselect as Capacitor circuit	• 2 1942_05
C8 Cap0402	☑ <b>2</b> Net_67
BGA1 untitled_pac Board	
OT	
	✓ Met. 79
2	☑ International
0	
	🗹 🖉 Net_88
	✓ Met_89
4 m	✓ ✓ ✓ ✓ ✓ ✓ ✓ ✓ ✓ ✓ ✓ ✓ ✓ ✓ ✓ ✓ ✓ ✓ ✓
6	☑ Net_97
- Zangara	
	<pre></pre>
Right-click on a circuit name to select/deselect as Die circuit	General
· · · · · · · · · · · · · · · · · · ·	Keep shape enabled when the net is disat
	Grav Daabled
< <u>Back</u> <u>N</u> ext > Cancel	UII Laver Selec I Circuit/Linka Net Manager
Vec 12.0 x0.11172 (SHCN0) Mountainer: Y	

- 4. Click Next.
- **5.** Right-click on another desired circuit.
- 6. Select it as a **Board** circuit.
| <b></b>  | actiM - Untitle     | ed - [pkg_flipchip_6      | .spd Layer View]         |                         |   |               |                                       |      | - 🗆 X                       |
|----------|---------------------|---------------------------|--------------------------|-------------------------|---|---------------|---------------------------------------|------|-----------------------------|
| 🧇 W      | /orkspace Edit      | : View Setup <sup>-</sup> | Tools Window Help        |                         |   |               |                                       |      | _ & ×                       |
|          | 🎽 🛃 🔹 🗍 🚺           |                           | B 19 - 10 - 10           | 🗐 🖸 🚺 Extrac            | tor Result  | - 🖿 🕆 👘 🧯 🚱   | • • • • • • • • • • • • • • • • • • • | )    | - 🤫 🖸 🔕 🕲 🕫 🗉               |
| Ø        | • • • •             |                           | 🕘 🕢 🛛 All Enabled Net(s) | - C - 🔊                 | I 🗕 Ŧ   | • 🗰 🖉 🔼 😭 🏎 🕽 | × 🗅                                   |      |                             |
| *        | • 📼 🚥 冒             | ■  🗄 間 🖪   ④              | X AA                     | - 🖓 🗹 🕹                 | 1 🕢 🖸 🚳   |               |                                       |      |                             |
| Wizaro   |                     |                           |                          | ×                       | -10   |               | 2 4 6 8                               | 10 🔺 | Layer Selection ×           |
| C        |                     |                           |                          |                         |   |               |                                       |      | 🍉 Signal02 🔲                |
|          | Select th           | e Board circuit from the  | list and click Finish    |                         | 16  |               |                                       |      | 🥗 Signal\$M1 📃              |
|          |                     |                           |                          |                         | 14  |               |                                       |      | Signal\$VDD                 |
|          | Ckt Name            | Ckt Model                 | Die/Board/Compo          |                         |   |               |                                       |      | Signal\$V55                 |
|          | U1                  | FC                        | Die                      |                         | 12  |               |                                       |      | Signal01                    |
|          | C8                  | Cap Select as             | Board circuit            |                         |   |               |                                       |      |                             |
|          | C6                  | Cap Deselect              | as Board circuit         |                         |   |               | 1                                     |      |                             |
|          | C5<br>C4            | Caporoz<br>Cap0402        |                          |                         | 0   |               |                                       |      |                             |
|          | C3                  | Cap0402                   |                          |                         |   |               |                                       |      |                             |
|          | C1                  | Cap0402                   |                          |                         |   |               |                                       |      |                             |
|          |                     |                           |                          |                         | 4   |               | 11/1/1/1/1                            |      |                             |
|          |                     |                           |                          |                         |   |               |                                       |      |                             |
|          |                     |                           |                          |                         | 2   |               |                                       | =    |                             |
|          |                     |                           |                          |                         | -   |               |                                       |      |                             |
| <u> </u> |                     |                           |                          |                         | 1   |               |                                       |      |                             |
|          |                     |                           |                          |                         | -2  |               |                                       |      |                             |
|          |                     | l                         | < <u>Back</u> Finish     | Cancel                  | The second se |               |                                       |      |                             |
|          |                     |                           |                          |                         | <b>1</b>  |               |                                       |      |                             |
|          |                     |                           |                          |                         | 6   |               |                                       |      |                             |
|          |                     |                           |                          |                         |   |               | 1 10 - C                              |      |                             |
|          |                     |                           |                          |                         | 8   |               |                                       |      |                             |
|          |                     |                           |                          |                         | 1-1-1-1   |               |                                       |      | View Only Active Layer      |
|          |                     |                           |                          |                         |   |               |                                       |      |                             |
|          |                     |                           |                          |                         | -12   |               |                                       |      | ⊙ Net Color ◯ Layer Color   |
| _        |                     |                           |                          |                         | 4   |               |                                       |      |                             |
| Ri       | aht-click on a circ | uit name to select/desel  | ect as Board circuit     | )                       |   |               |                                       |      | ∧ C — † • © \   \           |
| Ľ        |                     |                           |                          |                         |   |               |                                       | •    | Layer Selection Net Manager |
| Ver: 4.  | 1.2.12213 (SHCN     | 18)                       | 🔥 Mouse(mm               | ): X: -11.76, Y: 14.934 | ł   |               | Ready                                 |      |                             |

7. Click **Finish** to finish the setup.

#### **Setup Stackup**

- 1. Click on Stackup. The Stackup window opens.
- 2. Right-click on the bottom signal layer. You can insert layers above or under.

Stack	up									×
Layer Icon	Layer Name	Thickness(mm)	Conductivity(S/m)	Color	Trace Width(mm)	Shape Name	Permittivity	Loss Tangent	From File	Mater
	Signal02	5.0000e-003	5.000000e+007		1.0000e-001					
	Bump01	1.0000e-001					1.0000	0.0000		
	Signal\$M1	1.5000e-002	5.800000e+007		1.0000e-001					
	Medium\$di	1.2500e-001					4.2000	0.0000		
	Signal\$VDD	2.0000e-002	5.800000e+007		1.0000e-001	Shape\$VDD				
	Medium\$di	2.5000e-001					4.2000	0.0000		
	Signal\$VSS	2.0000e-002	5.800000e+007		1.0000e-001	Shape\$VSS				
	Medium\$di	1.2500e-001					4.2000	0.0000		
	Signal\$M4	1 5000e-002	5.800000e+007		1.0000e-001					
		Insert Above	•							
		Insert Under	Signal Lay	er						
		Delete	Medium La	yer						
			Plane Laye	r						
			Solderball	Mediu	m Layer, Signal	)1 Layer, and	Medium01 La	ayer BGA	1	
<			L	111						>
Total Thickness: 6.7500e-001 mm View Material										
Solder Ba	ll Layer 🗹 Bump	Right- Layer layer.	click on a dielectric(o	r signal	) layer to insert a b	ump or solder ba	Import	ОК	Cano	el

You can insert:

- Solder Ball Medium Layer
- Empty Signal Layer
- Medium Layer standing for a PCB Medium Layer

All layers are inserted under the bottom signal layer as shown in the example below. The added signal layer is the end of the solder ball.

#### **Setup Bump**

The example shows the setup for a Flip-chip package.

1. Click on **Bumps** in the Workflow pane. A new window opens up in the Editor pane.

Package Setup -> Bu	umps						X
Layer Name	Circuit Name	Dmax (mm)	D1 (mm)	D2 (mm)	HT (mm)	Conductivity (S/m)	
Bump01	U1	0.1	0.1	0.1	0.1	5.8e7	Bump Model
							DI T Dmax HT HT
ОК	Cancel						
Ver: 4.1.3.02141 (SI	G4)					0	Ready

**2.** Input the settings for the Bumps.

Maximum Diameter: Dmax (mm)

D1 (mm)

D2 (mm)

Height: HT (mm)

Conductivity (S/m)

3. Click OK to save your entries or click Cancel if you do not want to save your changes.

#### **Setup Flip-chip Package**

1. To setup the Solder Ball data for a Flip-Chip package, click Solder Ball in the Workflow pane under Package Setup, A new pane opens up in the bottom portion of the window.



**2.** Input the settings for the C4 Bumps.

Maximum Diameter: Dmax (mm)

D1 (mm) D2 (mm) Height: HT (mm) Conductivity (S/m)

3. Click OK to save your entries or Cancel if you do not want to save your changes.

#### **Setup Nets**

1. Click on Nets in the Workflow window. The Net Manager window opens.



2. Choose any desired nets for RLC extraction.

You can also move the signal net into and out of PowerNets and Ground Nets.

- At least one Ground Net must be selected to act as a reference ground net.
- Only choose the desired Ground Net as the reference ground net.
- **3.** To set up *Extraction Frequency and Capacitance/Inductance Output Control* for identfying coupled Trace, click

Auto Coupled Line

Net Manager		_ 🗆 ×
Net:	- 🔎	Show Coupled I 🔻
Net List (Sort enabled first)	Rise Time (ps)	%Coupling
Unnamed Net(s)		
😑 🗹 🎽 PowerNets	100	5
VDDcore	100	5 =
VDD_1	100	5
VDD_2	100	5
✓ ✓ VDD_3	100	5
VDD_4	100	5
🖃 🗹 🏾 🌌 GroundNets	100	5
VSS	100	5
DEFAULT	100	5
✓ Met_1	100	5
✓ Met_2	100	5
✓ Met_3	100	5
Net_4	100	5
✓ ✓ Net_5	100	5
Net_6	100	5
✓ ✓ Net_7	100	5
✓ ✓ Net_8	100	5
✓ ✓ Net_9	100	5
✓ ✓ Net_10	100	5
✓ ✓ Net_11	100	5
✓ ✓ Net_12	100	5
✓ ✓ Net_13	100	5
✓ Net_14	100	5
✓ Net_15	100	5
▶ Net_16	100	5 🚽
General		
Keep shape enabled when t	he net is disabled	ł
Gray Disabled		Hide Disabled
Coupled Lines		
Disable Coupled Line Simulat	ion	
Coupled Lines Report		
Layer Selection   Circuit/Linkage	Manager Net N	lanager

- **4.** Select the nets you wish to edit.
- **5.** Right-click to open the pop-menu.

Image: Net in the selected Ne	
Net     Disable Selected Nets     Inable All Nets	
🗹 🗾 Net Enable All Nets	
✓ Net_ Disable All Nets	
Net_	
Edit Coupling Parameters	
✓ Net_ Delete Coupling Parameters	
✓ Net_ Set With Default Parameters	
Detect Associated Nets	<b>_</b>
General New	
	abled
Delete Sa	ableu
Coupled Lines Rename	
Disable Coupled Import	
Coupled Lines Rep Merce Selected Nets	
Laver Selection I Ci Solit Open Nete	
Spin Open Nets	
3D View Walk Through	
Property .d	ler Ball I

#### **Set With Default Parameters**

- **1.** Select the net to be edited.
- 2. Right-click

A pop-up menu opens.

Net -	100 5	
Net	Enable Selected Nets	
Net	Disable Selected Nets	
🗹 🗾 Net	Enable All Nets	
🗹 🗾 Net_	Disable All Nets	
🗹 🗾 Net_		-
🗹 🗾 Net_	Edit Coupling Parameters	
Net_	Delete Coupling Parameters	
Net_	Set With Default Parameters	
Net_		
Net_	Classify	
Net_	Detect Associated Nets	
General		
Keep shape en	New	
Gray Disabled	Delete	sabled
Coupled Lines	Rename	
Disable Coupled	Import	
Coupled Lines Rep		-
Coopies surger top	Merge Selected Nets	
Layer Selection   Ci	Split Open Nets	
	3D View Walk Through	
	Presenter	der Ball N
	Froperty	

3. Select

Set With Default Parameters

#### **Rise Time and % Coupling**

When Traces are identified as coupled lines, the crosstalk between these lines are calculated during the simulation.

Coupled lines are treated as multi-conductor transmission lines, whereas an isolated Trace is modeled by the single transmission line algorithm. Coupled lines can be selected after the relevant Traces have been placed.

- **Rise Time Value** Must be greater than 0. Default value is 200 ps.
- %Coupling Value Must be 0 < value < 100. Default value is 5%.

**NOTE!** If the coupling parameters—%Coupling and Rise Time—are left blank, the trace-to-trace coupling is not calculated during simulation.

Based on electrical threshold parameters, Traces belonging to several nets are automatically identified and analyzed as coupled transmission line sections.

Two Traces are said to be coupled if their reverse crosstalk exceeds the %Coupling.

For a given Rise Time, the accumulated coupled section lengths between Trace nets should be long enough for forward crosstalk to exceed the %Coupling.

# **Show Coupled Lines**

1. Select

Net Manager > Show coupled line > Coupled lines report

A progress window appears to show you the progress.

Auto Coupled Line Formation in Progress	
Processing traces	
23%	
Cancel	

2. The Trace identified as coupled lines is displayed as shown in the following example.

�Coupled Line Navigation		×
Net: Net_4	- 14 4	1 of 3
Electrical Param. X-S	ection 🔽 Highlight	Report
Phy 3CPL06 N = 2 Coupled Section Len	sical Parameters gth = 0.17748mm	
Trace	Layer Name	Separation(Hori.)
Trace537_Auto_70::Net_31~SVL1 Trace597::Net_4~SVL1	Signal\$M1 Signal\$M1 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	N/A 0.16163mm
<		Þ

# **EXTRACTION FREQUENCY AND CAPACITANCE/INDUCTANCE OUTPUT CONTROL**

You can change the extraction frequency. The default value is 30MHz. Use the window shown in the exaple to change the default value.

Follow these steps:

1. Select

Setup > Extraction Frequency

The Extraction Frequency window opens.

Extraction Frequency X						
Extraction Frequency:	100	MHz	OK Cancel			

2. Set frequency in the pop-up window.

#### **Set Threshold for Exporting Mutual Terms**

XtractIM captures all the coupling during the extraction stage. It has options to reduce the size of the output circuit during the export stage.

1. Open

Setup-> Threshold for Exporting Coupling Terms

A pop-up window opens.

Threshold for Exporting Coupling Terms	×
Number of strongest neighbors to export 10	
In addition,	
Ignore mutual C if the ratio of mutual over self terms is less than 0.	005
Ignore mutual L if the ratio of mutual over self terms is less than 0.	.005
OK Cancel	

2. Enter the number of strongest coupling neighbors to be kept in the circuit model.

The default of number of strongest coupling neighbors is 10; which means only outputting the 10 strongest neighbors (including self).

**3.** Ignore mutual capacitance or inductance if the ratio of mutual terms over self term is less than a percentage.

The default percentage threshold for ignoring mutual capacitance or inductance is 0.005.

If the mutual capacitance/inductance is less than the 0.5% of the minimum of the two selfcapacitances/inductances,

XtractIM will not output the mutual capacitance/inductance.

#### Save the Workspace and Layout File

On the Toolbar, click the next to the **Save** button , the drop-down list shows up. You can choose to save workspace file or layout file.

	Work	spac	е	Edit	View	Sel	tup
)	6	H	•		•		=:::
1	-		Sa	/e Worl	kspace	File	6
ī	Enable		Sa	/e Layc	out File		

- Select Save Workspace File, the workspace file is saved.
- Select Save Layout File, or click the Save button , the XtractIM Layout File Saving Options dialog opens.

XtractIM Layout File Saving Options	×
Shape Processing	
Error Checking	
Skip Warnings in Error Log File	
OK Cancel	

#### **Using the Save as Option**

The example below shows another way to save the workspace and layout file using the **Save as** option. Saving the workspace does not automatically save the .spd file. Similarly, saving the .spd file does not save the workspace file.

1. Select

Workspace > Save As...

The Save Workspace File window opens.

Save Workspace	File ?	×
Save in:	🔁 Stacked-BGA_Sample_files 🔹 🕥 🤣 📂 📰 -	
My Recent Documents	PoP_flipchip PoP_flipchip-1 POP_wirebond	
Desktop		
My Documents		
My Computer		
	File name:	e
My Network	Save as type: Extractor Workspace XML Files (*.xml)  Cance	el j

- 2. Enter a name.
- 3. Click Save.

# **OBSERVE AND SAVE RESULTS**

XtractIM calculates each net resistance, self loop inductance, conductance, self capacitance as well as its mutual loop inductance and mutual capacitance with other nets.

In the Inductance Matrix, the Diagonal Element is the Self Inductance of each net; the off-diagonal elements are mutual Inductance. The inductance and capacitance are matrices. For example, a simple group of four nets has the following inductance and capacitance matrix.

$\begin{bmatrix} L_{11} & L_{12} & L_{13} & L_{14} \end{bmatrix}$	$C_{11}$	$C_{12}$	$C_{13}$	$C_{14}$
$L_{21}$ $L_{22}$ $L_{23}$ $L_{24}$	$C_{21}$	$C_{22}$	$C_{23}$	C <sub>24</sub>
$L_{31}$ $L_{32}$ $L_{33}$ $L_{34}$	$C_{31}$	$C_{32}$	$C_{_{33}}$	C <sub>34</sub>
$\begin{bmatrix} L_{41} & L_{42} & L_{43} & L_{44} \end{bmatrix}$	$C_{41}$	$C_{42}$	$C_{43}$	$C_{44}$

#### **Capacitance Matrix**

The two concepts of capacitance matrix: Maxwell capacitance matrix and SPICE capacitance matrix.

- Maxwell Capacitance Matrix Each diagonal element is the loading capacitance (i.e., capacitance to ground when other nets are grounded which represents the worst-case capacitive loading). Off-diagonal elements are mutual capacitance with negative values.
- **SPICE Capacitance Matrix** Each diagonal element is capacitance to ground. Off-diagonal elements are mutual capacitance with positive values.

The relationship between Maxwell capacitance and SPICE capacitance matrix is shown here:

#### **Capacitance Example**

$$\begin{split} C_{ij}(SPICE) &= -C_{ij}(Maxwell) \\ C_{ii}(Maxwell) &= \sum_{j} C_{ij}(SPICE) \\ C_{ii}(SPICE) &= \sum_{j} C_{ij}(Maxwell) \end{split}$$

#### **RLC Per Net View**

Choose to view resistance, self-inductance, self-capacitance or mutual for each net. Usually conductance is very low; so there is no view for conductance.

- Mutual Term View Mutual inductance or SPICE mutual capacitance.
- Self Term View Resistance, self-inductance or Maxwell diagonal capacitance.

#### **Self Terms View**



#### **Mutual Terms View**



#### Summary of the Extracted Results

Click on Summary to open the summary and tabulated data for R, L and C.

- **Bottom right window** Displays a complete row of the R / L / C matrices when a certain net is chosen. You can also reorder the list.
- **Top right window** Displays the overall results including package name, nets extracted, extraction frequency, maximum / minimum R, L, C and the full RLC matrix.

Click on  $\mathbf{R} / \mathbf{L} / \mathbf{C}$  heading. The values are listed in increase or decrease order. The Table Content (RLC Full matrix) is automatically saved on hard disk in .csv format.

XtractIM Summary.

XtractIM - FlipChip.xml - [Sum	mary	]									x
🛟 File Window Help										_ 8	×
: D 😂 🔲 - L III 🕨 🔳 🔳		- C - C - C	+		Extractor Result	- 1B	len 🛱	n i de 📭 🗛 I	• •		
			1		Excidecol Result						
WORKFIOW: Xtractim	×	Extractor Result									
Default	*	[Version]			4.1.2.1221	.3					
Manage Workspace		[Date]	Date] 0			01/20/2011					
		[Package Name]	]		C:\Sigrity	C:\SigritySamples\SpeedPKG 4.1\XtractIM\Samples\Single-Di				_	
Load Workspace		[Description]			C:\Sigrity	C:\SigritySamples\SpeedPKG 4.1\XtractIM\Samples\Single-				les\Single-Die	
Load a New/Different Layout		[Nets Extract	ed	]	105						
Package Setup 🛛 🙆		[Frequency of	E	xtraction]	30MHz						
Package Type: Flip-Chip		[Max R(mOhm)]			312.408						$\equiv$
Circuits		[Min R(mOhm)]			3.99941						
🗸 Stackup		[Max self-ind	uc	tance L(nH)]	8.70872						
V Bumps		[Min self-ind	uc	tance L(nH)]	0.306726						
V Solder Ball		[Max self-cap	ac	itance C(pF)	39.0554						
Nets		[Min self-cap	ac	itance C(pF)	0.495727						
Simulation Setun											+
		4			111						
Module: IBIS/REGC			_								
Simulation Type: Net-based		Net		Net	R(mOhm)	L(nH)		C(pF)			-
View/Export Results 🛛 🙆		VDD_1		VDD_1	11.1517	1.01241		18.2667			
Summary		VDD_2		VDD_2	0	0		0			
SPICE/IBIS Model		VDD_3	=	VDD_3	0	0		0			=
RLC Per Net		VDD_4 VDDcore		VDD_4 VDDcore	0	0		0			
RLC Distributions		Net 1	_	Net 1	ů 0	0		0			
Segment RLC		Net_2		Net_2	0	0		0			
RLC vs. Net Length		Net_3		Net_3	0	0.179736		0.414133			
CrossTalk		Net_4		Net_4	0	0.389996		0.446551			
Save Results		Net_5		Net_5	0	0.777261		0.536162			
Load Results		Net_6		Net_6	0	0.643644		0.552145			
Customize Workflow	×	Net 8		Net 8	0	0 186633		0 339077			
Customize Worknow	×	Net 9		Net 9	0	0		0.007077			
		Net_10		Net_10	0	0		0			
		Net_11		Net_11	0	0		0			
		Net_12		Net_12	0	0		0			
		Net_13		Net_13	0	0		0			
		Net_14		Net_14	0	0.751382		0.700147			
		Net 16		Net 16	0	0 451408		0 686555			
		Net 17		Net 17	0	0		0			
		Net 18		Net 18	0	0		0			
		Net_19		Net_19	0	0		0			
	_	Net 20	*	Net 20	0	0	_	0			-
Ver: 4.1.2.12213 (SHCN8)	Mo	use(mm): X: -13.787, '	Y: 1	0.089			🔵 Rea	ady			

File Example

×	Microso	ft Exce	l - pkg_	flipchip	5_6_T		X
N H	] <u>F</u> ile <u>E</u> di elp	t <u>V</u> iew ;	Insert F <u>o</u> r	mat <u>T</u> ool	ls <u>D</u> ata	Window _ &	×
	i 💕 🖬 🔒	3 8 9	- (° - )	E - ĝ↓ X		🙄 i 💩	• =
	220	1 🧠 🦄 I	533				
_	A1	+	∱ Neti				
	A	В	С	D	E	F	
1	Net i	Net j	Rij (mOhm	Lij (nH)	Cij (pF)		-
2	VDD_1	VDD_1	375.523	1.33335	17.3092		-
3	VDD_1	Net_5		1.08321	0.398697		
4	VDD_1	Net_14		1.051	0.518955		
5	VDD_1	Net_32		1.01675	0.397362		
6	VDD_1	Net_6		0.861468	0.41072		
7	VDD_1	Net_41		0.800441	0.204633		
8	VDD_1	Net_16		0.602553	0.509207		
9	VDD_1	Net_31		0.540265	0.0607		
10	VDD_1	Net_4		0.526196	0.328424		
11	VDD_1	Net_15		0.334126	0.0241		
12	VDD_1	Net_8		0.288975	0.244139		
13	VDD_2	VDD_2	353.296	1.186	18.519		
14	VDD_2	Net_35		0.940149	0.606868		
15	VDD_2	Net_55		0.894187	0.494193		
16	VDD_2	Net_50		0.889056	0.398466		
17	VDD_2	Net_45		0.858216	0.457411		
18	VDD_2	Net_54		0.856756	0.403705		
19	VDD_2	Net_62		0.847576	0.533051		
20	VDD_2	Net_49		0.673875	0.179802		
21	VDD_2	Net_65		0.673127	0.178135		
22	VDD_2	Net_43		0.537349	0.290531		
23	VDD_2	Net_63		0.489275	0.374008		
24	VDD_2	Net_72		0.345013	0.329168		*
М	• • • \ [	okg_flipchi	p_6_Table	Conte <		>	
Dr	aw - 🗟   /	AutoShapes	· \ × [		🖻 🖪 👶	8	**
-		( ) (			10 10 10	ji ji	

#### **SPICE and IBIS Models**

Upon completing the simulation both are in the same directory as the .spd file.

- SPICE Model is saved as a SPICE sub-circuit with the extension .ckt.
- IBIS Model is saved as an IBIS package model with the extension .pkg.

The total number of each element in the circuit is displayed along the bottom of the window.

- R
- L
- M
- C
- G where M is the mutual inductance



## **SPICE / IBIS Model Result View**

Below is the SPICE / IBIS Model result view.

- The SPICE model is a PI-circuit.
- The IBIS model is shown with coupling.



#### **Pin Model: Excel Format**

In the SPICE/IBIS Model window, click

#### Pin Model: Excel format

A .csv file is loaded. It includeds this information for each net. Self-C is the Maxwell Capacitance.

- DC\_R
- Net length
- Net name
- Pin name
- Self-C
- Self-L
- Self-R

XtractIM - FlipChip.xml - [Circuit	Торо	ogy Result]						- 🗆 X
🔶 File Window Help								_ 8 ×
		C≤   0 + 0 +		Extractor Decult		Re i de de d		
				Extractor Result				
		Result						
Default	<u>^</u>							
Manage Workspace 🛛 🙆		View Model Selection	on					
Load Workspace		O SPICE T-model						
Load a New/Different Layout		O CDICE Disertel			A A A	000		
Package Setun		O SPICE PHILODE			-~~~a	<u>,</u>		
Deckage Sectop		OIBIS .pkg model					_	
Package Type: http-chip		O Dis sus del LIDIO (						
Stackup		Pin moder: IBIS fo	Jinat					
<ul> <li>Bumps</li> </ul>		Pin model: Excel	format					
Solder Ball		O DC Registeres						
Nets		UC nesistance						
Simulation Setun		PinName	NetName	NetLenath(mm)	SelfR(0hm)	SelfL(nH)	SelfC(pF)	Delav(pS)
Module: IRIS/RI GC		BGA1-C1: BGA1	VDD 1		0.0111517	1.01241	18,2667	135.99
Simulation Type: Net-Based		BGA1-A3; BGA1	VDD_2		0.0102248	0.907861	19.8208	134.144
Simulation Type. Net based		BGA1-C12; BGA	VDD_3		0.0106824	0.960092	19.1304	135.525 =
View/Export Results		BGA1-K6; BGA1	VDD_4		0.0103718	0.928585	19.7203	135.322
Summary		BGA1-C3; BGA1	VDDCore	9 78878	0.00399941	6.433	39.0004	80.8017
SPICE/IBIS Model		BGA1J3	Net 2	7.03801	0.140301	4,2693	0.849707	60.23
RLC Per Net		BGA1-J1	Net_3	12.6627	0.295479	7.89193	1.33262	102.552
RLC Distributions		BGA1-H2	Net_4	8.50694	0.182736	5.93211	0.922568	73.9782
Segment RLC		BGA1-G2	Net_5	7.88406	0.165153	5.22156	0.89004	68.1718
RLC vs. Net Length		BGA1-E2	Net_b	8.35208 e.5e27e	0.176814	5.51613	0.922112	71.3196
CrossTalk		BGA1-D2	Net 8	8.62617	0.185649	5 68008	0.949029	73 4204
Save Results		BGA1-C2	Net_9	9.0939	0.197461	5.89651	0.953805	74.9942
LUdu Results		BGA1-M2	Net_10	11.3715	0.263713	7.74321	1.18475	95.7797
Customize Workflow	×	BGA1-L1	Net_11	12.0044	0.278254	7.84506	1.25644	99.2815
		BGA1-H4 BGA1-G5	Net_12 Net_13	5.448/5	0.0977836	3.1543	0.724434	47.8025
		BGA1-F1	Net 14	10.1332	0.225123	6.49432	1.0865	20.7040
		BGA1-F5	Net 15	3.63951	0.0486726	2.0824	0.550119	33.8463
		BGA1-D1	Net_16	10.9788	0.247073	7.15291	1.14137	90.3554
		BGA1-D3	Net_17	8.12152	0.169652	4.71835	0.990793	68.3733
		BGA1-B2	Net_18	10.0307	0.222467	6.79938	1.04455	84.2749
		BGA1J3	Net_19 Net_20	4.80254	0.0809202	2.90123	0.641788	43.1506
		DCAT UE	Not 21	E EOEOC	0.21302	2 07007	0 004070	10 0E
					III			
Ver: 4.1.2.12213 (SHCN8)	Mouse	(mm): X: -13.787, Y: 10	0.089		🥏 R	eady		

#### **RLC Distributions**

To see the full matrix value of R, L and C, click

**RLC** Distributions

RLC Distributions offers eight kinds of views.



#### Segment RLC

For each signal net, XtractIM outputs the segment RLC of each metal layer.

Click on **Segment RLC** in the workflow pane (under View / Export Results). The Segment RLC values are shown at the bottom of the window.

There are three bars for Resistance, Inductance or Capacitance. Click on the Resistance, Inductance or Capacitance bar. The related values are displayed.

XtractIM - FlipChip.xml - [Segment	RLC Result]						- 🗆 X
💠 File Window Help							_ 8 ×
E D 😂 🖃 - 1 01 🕨 🔳 🔳 🚥 🖬	- C - C	- 1 🗂 🖻 🗖 🖬	Extractor Result	- <b>1</b>	Pa : 22 Pa 19		
Workflow: XtractIM	Extractor Besult						
Defuilt							
Default	PinName	SignalNetName	Signal@M1(Obm)	Signal@VDD(0hm)	Signal@VSS(().hm)	Signal\$M4(Obm)	
Manage Workspace 🛛 🙆	BGA1J 2	Net 1	0.180109	0.0111254	0.00946193	0.0119596	
Load Workspace	BGA1J3	Net 2	0.11236	0.010766	0.00340133	0.0119596	
Load a New/Different Lavout	BGA1J1	Net 3	0.246925	0.010766	0.00949127	0.0119596	
Dudues Ontaria	BGA1-H2	Net_4	0.147416	0.010766	0.00949127	0.0119596	
Package Setup	BGA1-G2	Net_5	0.133487	0.0107647	0.00949005	0.011958	
Package Type: Flip-Chip	BGA1-E2	Net_6	0.144806	0.010766	0.00949127	0.0119596	
Circuits	BGA1-E3	Net_7	0.100455	0.0106971	0.0094925	0.0119613	=
🗸 Stackup	BGA1-D2	Net_8	0.151882	0.0107647	0.00949005	0.011958	
V Bumps	BGA1-C2	Net_9	0.163308	0.0107647	0.00946071	0.011958	
✓ Solder Ball	BGA1-M2	Net_10	0.220419	0.010/64/	0.00949005	0.011958	
V Nets	BGAT-LI DCA1.UA	Net_11	0.235636	0.0107673	0.0094925	0.0119613	
	BGA1-H4	Net_12	0.0703525	0.010766	0.00343127	0.0113336	
Simulation Setup	PGALE1	Net_13	0.00042362	0.00040337	0.00736766	0.0124000	
Module: IBIS/RLGC	BGA1-F5	Net 15	0.023299	0.0134646	0.00343127	0.011958	
Simulation Type: Net-Based	BGA1-D1	Net 16	0.209214	0.010766	0.00049127	0.0119596	
View/Eurort Deculto	BGA1-D3	Net 17	0.137268	0.010766	0.00949127	0.0119596	
	BGA1-B2	Net 18	0.176829	0.0178275	0.00946193	0.0119596	
Summary	BGA1-J5	Net 19	0.0565564	0.0107647	0.00949005	0.011958	
SPICE/IBIS Model	BGA1-L3	Net_20	0.178104	0.0107673	0.00946315	0.0119613	
RLC Per Net	BGA1-H5	Net_21	0.071978	0.00613949	0.00509164	0.026999	
RLC Distributions	BGA1-K2	Net_22	0.20084	0.0107647	0.00946071	0.011958	
Segment RLC	BGA1-H3	Net_23	0.123366	0.0107673	0.00946315	0.0119613	
RLC vs. Net Length	BGA1-E4	Net_24	0.0815806	0.0106953	0.00949127	0.0119596	
CrossTalk	BGA1-B1	Net_25	0.24245	0.0107673	0.0094925	0.0119613	
Save Results	BGA1-A2	Net_26	0.23/424	0.0107647	0.00949005	0.011958	
Load Results	BGA1-C4 BGA1.K5	Net_27	0.112401	0.0107647	0.00343005	0.011998	
2000 NOSOCO	BGA1-KS	Net 29	0.168097	0.010766	0.00343003	0.0119596	
Customize Workflow ¥	BGA1-K4	Net 30	0.138505	0.0107647	0.00343127	0.011958	
	BGA1-G4	Net 31	0.0842866	0.0106953	0.00946071	0.011958	
	BGA1-F2	Net 32	0.163217	0.0107647	0.00949005	0.011958	
	BGA1-B3	Net 33	0.193488	0.0107673	0.00946315	0.0119613	
	BGA1-D5	Net_34	0.0715071	0.0107647	0.00949005	0.011958	
	BGA1-A4	Net_35	0.218258	0.0107647	0.00949005	0.011958	
	BGA1-J6	Net_36	0.0506351	0.0116911	0.00949127	0.0119596	
	BGA1-H6	Net_37	0.0226582	0.0122219	0.0085416	0.0119613	
	BGA1-L5	Net_38	0.166616	0.010766	0.00949127	0.0119596	-
	DEAT MA	MAL 90	11-2200EE	0.0107647	IT HOMOTOR	1111060	
	Resistance(Ohm)	Inductance(nH) C	apcitance(pF)				
Ver: 4.1.3.02141 (SIG4) Mo	ouse(mm): X: -15.127, \	(: 12.805		0	Ready		

# SAVE RESULTS

1. In the Workflow pane (under View / Export Results), click

#### Save Results

The Save Extractor Result window appears.

Save Extractor R	lesult As				? X
Save in:	🚞 Single-Die_Sa	mple_files	- 3	1 🕫 🖽	•
My Recent Documents Desktop My Documents	<ul> <li>CPU_Info</li> <li>FlipChip</li> <li>FlipChip_pkg_fli</li> <li>ibis_flipchip_pkg</li> <li>ibis_flipchip_pkg</li> </ul>	pchip_6_DCResistance pchip_6_PinModel pchip_6_SegmentC pchip_6_SegmentL pchip_6_SegmentR pchip_6_signal_Xtalk pchip_6_SPICE_t.ckt pchip_6_TableContent g_flipchip_6.pkg g_flipchip_6_pin.ibs			Result_FlipChip_pk Result_FlipChip_pk Result_FlipChip_pk Result_FlipChip_pk Result_FlipChip_pk Result_FlipChip_pk Result_FlipChip_pk Result_FlipChip_pk Result_FlipChip_pk Result_FlipChip_pk Result_FlipChip_pk Result_FlipChip_pk
My Computer	pkg_flipchip_6 ResourceProfile	2_XtractIM			Jntitled_pkg_flipcf Jntitled_pkg_flipcf
	File name:	Result		-	Save
My Network	Save as type:	All File (*.*)		-	Cancel :

- 2. Enter a file name.
- Click on Save. The results are saved in a binary file named as result and result\_spd\_file\_name.xim
- 4. Click on Cancel if you do not want to save the results in the file name you entered.

# **Output Files**

The SPICE file and two IBIS files are automatically saved by the tool. The result file is only if the user chooses to save. The **result** and **result\*.xim** files save all the output data including:

- SPICE circuit
- Summary
- Two package model files.

The output files on hard disk include:

- One IBIS Package Model File \*.pkg file. Both L and C include coupling elements.
- One Pin Model in Excel Format \*.csv file. Including each signal net length, self-R, self-L, self-C, and time delay. No coupling elements are included.
- One Pin Model in IBIS Fomat \*.ibs file. Including self-R, self-L and self-C for each signal net. No coupling element is included.
- One Summary Content in Excel Format \*.csv file. Including RLC Full Matrix.
- Three Segment RLC in Excel Format Segment RLC of each metal layer with \*.csv files.
- Two SPICE Circuit Files Pi-model named \*.ckt and T-model named \* t.ckt.

#### **Load in Saved Results**

Saved results can be loaded by selecting Load Results in the workflow pane.

- Loaded Curves Shows the loaded results.
- Main window Shows the selected result.
- **Present Curves** Present extraced results.

Choose to view present results or the loaded results. A loaded result can be unloaded by clicking on the Unload Extractor Result icon in the toolbar. The Load and Unload Result buttons are indicated.



#### **BATCH MODE SIMULATION**

To run a simulation in Batch Mode, follow these steps.

- 1. Click
  - Start -> Run
- 2. Change to the directory where the XtractIM.exe file is located.

**Batch Mode Example** 

- If you want to use the project (.spd file) defaulted in the workspace file (.ximx file), enter: ExtralM -b "Full\_path\_toMy\_workspace\_File\*workspace filename*"
- If you want to use a different project file other than the one in the .xml file, enter:
  - ExtralM -b "Full\_path\_toMy\_workspace\_File\workspace filename"

"Full\_path\_toMy\_workspace\_File\new\_spd-filename"

#### **Saved Output Files**

Upon completing the simulation, all output files are saved automatically in the same directory as the \*.spd file. Saved files include:

- \*.ckt
  - \*.csv
- \*.ibs
- \*.pkg

#### Package Setup

XtractIM can handle both flip-chip packages and wirebond packages with 3D bonding wire profiles. It can extract models of full packages or selected nets of a package.

Open the XtractIM main window. There are only two icons available: New and Open.

- New icon Creates a new workspace.
- Open icon Allows users to load an existing workspace file.

You'll setup the following items to prepare for a simulation.

- 1. Select a package type: wirebond or flip-chip.
- 2. Set the C4 Bump data if it is a flip-chip package.
- **3.** Set the Solder Ball data.
- 4. Setup the circuits.
- 5. Select or deselect Die-circuit and Board circuit.
- 6. Setup the Stackup.
- 7. Set parameters for the C4 Bump and Solderball medium layer.
- **8.** Select the nets for extraction.

There are four options to define the extraction frequency and extraction result output.

- Set Extraction Frequency.
- Set Mutual Capacitance Output Filter Factor.
- Set Mutual Inductance Output Filter Factor.
- Set Strongest Coupling Neighbors.

# Chapter

# **XtractIM Simulation of a Stacked BGA Package**

This chapter takes you through the steps to use the XtractIM tool in the simulation of a stacked BGA Package.

# SIMULATION SETUP

A typical workflow in interaction mode includes the following steps.

- Create a new workspace file or load an existing file (.ximx file).
- Open a layout file (.spd file).
- Select a package type: wirebond or flip-chip, single BGA or stacked BGA.
- Set up the circuits: select or deselect Die-circuit and Board circuit.
- Set up the Stackup: set parameters for the C4 Bump/Solderball medium layer.
- Set the Bump data if it is a flip-chip package.
- Set the Solder Ball data.
- Select the nets for extraction.
- Setup extraction frequency and capacitance / inductance output control.

#### **Setup the Package Simulation**

- **1.** Start in the Workspace.
- 2. Open the XtractIM main window.

There are only two icons available: New and Open.

The new icon creates a new workspace.

The open icon allows users to load an existing workspace file.

- **3.** Select appropriate icon (new  $\square$  or open  $\square$  ). Click.
- 4. To create a new workspace, click on the New icon;

or select

Workspace > New



 To load the Package Structure, click on Load a New / Different Layout The Attach Layout File window opens.

Attach Layout File	×						
Apply current workspace setup							
Please choose the type of layout to load							
<ul> <li>Load an existing SPD file</li> </ul>							
O Load an existing DXF file							
OK Cancel							

#### Select Package Type

**1.** Select a Package Type.

The package type settings are displayed in the Editor pane.

The example show a package type that is

Single Die, Stacked BGA, Flip-Chip



- 2. Click **OK** to save your selection.
- 3. Click **Cancel** if you want to change your selection, start over or cancel your session.

# **Setup Circuits**

1. Click on **Circuits** in the Workflow pane to setup the Circuits data for a Flip-Chip package. A new pane opens up in the left side of the workspace.

Ckt Name	Ckt Model	Die/Board/Compo
POPtop	POP_top	Board
POPbottom	POP_bot	Board
Die1	Die2	Die
C8	Cap0402	
C7	Cap0402	
C6	Cap0402	
C5	Cap0402	
⊂4	Cap0402	
C3	Cap0402	
C2	Cap0402	
⊂1	Cap0402	

**2.** Right-click on the desired circuit.

Ikt Name	Ckt Mod	del	Die/Board/Compo	
OPtop	POP_to	op	Board	
OPbottom	POP_b	ot	Board	
)ie1	Die2		Die	
:8	Cap040	02		
.7	Cap040	02		
.6	Capf			
5	Capt	Select as	Die circuit	
4	Capt	Deselect	as Die circuit	
3	Capt	Select or	Conneitor circuit	
2	Capt	Select as	Capacitor circuit	
1	Capt	Deselect	as Capacitor circuit	

- **3.** Select it as a **Die** circuit.
- 4. Click Next.

- 5. Right-click on another desired circuit.
- 6. Select it as a **Board** circuit.
- 7. Setup the second Board circuits.
- 8. Click Finish to finish the setup.

#### **Setup Stackup**

- 1. Click on Stackup. The Stackup window opens.
- 2. Right-click on the Signal\$Bottom layer.

Layer Man	ager -> S	Stack Up							<b>— ×</b>
Stack Up	Pad Stac	:k							
Layer #	Color	Layer Icon	Layer Name	Thickness(mm)	Material	Conductivity(S/m)	Permittivity	Loss Tangen	t   Fill-in Dielect
1			Signal03	0.005		5e+007			
			Bump01	0.1			1	0	
2			Signal\$136C4D7	0.015		1.81429e+006			
			Medium\$136C4	0.125			4.2	0	
3			Signal\$136C4DF	0.015		1.81429e+006			
			Medium\$136C4	0.125			4.2	0	
4			Signal\$136C4E7	0.02		1.81429e+006			
			Medium\$12F371	0.125			4.2	0	
5			Signal\$136C4EF	0.015		1.81429e+006			
			]	insert Above 🕨					
			]	nsert Under 下	Signal Layer				
				Delete	Medium Layer				
					Plane Laver				
					Solderball Medium	Layer, Signal01 Laye	r, and Mediu	m01 Layer 🔰	POPbottom
									POPtop
			111						P
Unit: mm	🔻 Tot	al Thickness:	5.4500e-001 mm					View Material	Import
Solder I	Ball Layer	🕑 Bump Lay	/er				_		
								ок	Cancel

For a PCB medium layer you can insert:

- A Solder Ball Medium Layer
- An empty signal layer
- A medium layer standing

All layers are inserted under Signal\$Bottom. The added signal layer is located at the end of the solder ball.

# **Setup Bumps**

The example shows the setup for a Flip-chip package.

1. Click on **Bumps** in the Workflow pane. A new window opens up in the Editor pane.

Package Setup -> Bu	mps						×
Layer Name	Circuit Name	Dmax (mm)	D1 (mm)	D2 (mm)	HT (mm)	Conductivity (S/m)	
Bump01	U1	0.116727	0.116727	0.116727	0.1	5.8e7	Bump Model
							H D1 H HT
ок	Cancel						
Ver: 4.1.3.02141 (SIG	54)	Mouse(mm	): X: -15.76, Y:	12.594			

- Input the settings for the C4 Bumps. Maximum Diameter: Dmax (mm) D1 (mm) D2 (mm) Height: HT (mm) Conductivity (S/m)
- 3. Click OK to save your entries or click Cancel if you do not want to save your changes.

#### **Setup Solder Ball**

1. Click Solder Ball in the Workflow pane. A new pane opens up in the Editor pane.

Package Setup -> Solder Ball X								
Layer Name	Circuit Name	Dmax (mm)	D1 (mm)	D2 (mm)	HT (mm)	Conductivity (S/m)	Medium Thickness (mm)	Solder Ball Model
Solderball01	POPbottom	0.397115	0.397115	0.397115	0.5	5.8e7	0.05	
Solderball02	POPtop	0.397115	0.397115	0.397115	0.65929	5.8e7	0.05	
								H D2 →
								← Dmax → HT ← D1 → ↓ ← D1 → ↓ ← D1 → ↓ Ground
OK Cancel								
Ver: 4.1.2.12213 (SHCN8) 🔥 Mouse(mm): X: -12.206, Y: 0.627								

2. Input the settings for each Solder Ball.

Maximum Diameter: Dmax (mm) D1 (mm) D2 (mm) Height: HT (mm) Conductivity (S/m) Medium Thickness

**3.** Click **OK** to save your entries.

Click Cancel if you do not want to save your changes.

**NOTE** Set up two solder balls for each stacked BGA package.

#### **Setup Nets**

- 1. Click on Nets in the workflow window. The Net Manager window opens.
- 2. Choose any desired nets for RLC extraction.

Users can also move the signal net into and out of PowerNets and Ground Nets.

- At least one Ground Net must be selected to act as a reference ground net.
- Only choose the desired Ground Net as the reference ground net.
| Net Manage                            | r                                      |                 | ×    |
|---------------------------------------|--|-----------------|------|
| Net:                                  |  | -               | ρ    |
| Defau                                 | lt Mode                                | -               |      |
| Net List (So                          | ort enabled first) 斗                   | Interface       | -    |
|                                       | 🖉 Unnamed Net(s)                       |                 |      |
|                                       | PowerNets                              |                 |      |
|                                       | VDDcore                                |                 |      |
|                                       | VDD_1                                  |                 | Ξ    |
|                                       | VDD_2                                  |                 |      |
|                                       | VDD_3                                  |                 |      |
|                                       | VDD_4                                  |                 |      |
|                                       | GroundNets                             |                 |      |
|                                       | VSS                                    |                 |      |
|                                       | DEFAULT                                |                 |      |
|                                       | Net_1                                  |                 |      |
|                                       | Net_2                                  |                 |      |
|                                       | Net_3                                  |                 |      |
|                                       | Net_4                                  |                 |      |
|                                       | Net_5                                  |                 |      |
|                                       | Net_6                                  |                 |      |
|                                       | Net_7                                  |                 |      |
|                                       | Net_8                                  |                 |      |
|                                       | Net_9                                  |                 |      |
|                                       | Net_12                                 |                 |      |
|                                       | Net_13                                 |                 |      |
|                                       | Net_14                                 |                 | _    |
|                                       | Net_15                                 |                 |      |
|                                       | Net_16                                 |                 | _    |
|                                       | Net_17                                 |                 | -    |
|                                       | Net_19                                 |                 | _    |
|                                       | ✓ Net_21                               |                 |      |
|                                       | Net_23                                 |                 | _    |
|                                       | Net_24                                 |                 | -    |
| I I I I I I I I I I I I I I I I I I I | 111                                    | →               |      |
| -General-                             |  |                 |      |
| Keep sh<br>Hide Dis<br>Gray Dis       | ape enabled when ti<br>abled<br>:abled | ne net is disab | oled |
| Layer Selec                           | tion Net Manager                       |                 |      |

 To set up *Rise Time and %Coupling* for identifying coupled Trace, click Auto Coupled Line



- 4. Select the nets you wish to edit.
- 5. Right-click to open the pop-menu.

Net M	anager			×		
Net:				- 2		
	Show Coupled Line <					
NetL	.ist (Sor	t enabled first) 🛆	Rise Tin	ne (p: 🔶		
	2 🗾	Unnamed Net(s)				
	3 🔰	PowerNets				
	$\checkmark$	VDDcore				
	$\checkmark$	VDD_1	100	=		
		VDD_2				
		VDD_3				
		VDD_4				
	<u>ت</u> ک	GroundNets	400	_		
		VSS DEFENSE	100			
			100			
	Ena	ble Selected Nets				
	Disa	able Selected Nets				
	Ena	ble All Nets				
	Disz	able All Nets				
	2100					
	Edit	Coupling Parameter	ers			
	Dele	ete Coupling Param	neters			
	Set With Default Parameters					
	Clas	ssify	+			
	Det	ect Associated Net	ts			
	Nev	N				
	Del	ete				
	Ren	name				
•6	Imp	ort				
Ge	Mer	ge Selected Nets				
	Split Open Nets disabled					
	3D	View Walk Throug	h			
<b>C</b>	Prop	perty				
Coup	led Line	es Report	uon			
Layer	Selecti	ion Net Manager				

6. Select

Set With Default Parameters

7. Click

Net Manager > Coupled Lines > Show Auto Coupled Lines The Trace identified as coupled lines appear.

#### **EXTRACTION FREQUENCY AND CAPACITANCE / INDUCTANCE OUTPUT CONTROL**

You can change the extraction frequency. The default value is 30MHz. Use the window shown in the example to change the default value. Follow these steps:

1. Select

Setup > Frequency of Extraction

2. Update the data in the pop-up window.

#### **Set Output Factors**

XtractIM captures all the coupling during the extraction stage. It has options to reduce the size of the output circuit during the export stage.

1. Open

Setup > Threshold for Exporting Coupling Terms

A pop-up window opens.

Threshold for Exporting Coupling Terms	×
Number of strongest neighbors to export 10	
In addition,	
Ignore mutual C if the ratio of mutual over self terms is less than	0.005
Ignore mutual L if the ratio of mutual over self terms is less than	0.005
OK Cancel	

2. Choose the number of strongest coupling neighbors to be kept in the circuit model. In addition, ignore mutual capacitance or inductance if the ratio of mutual terms over self term is less than a percentage.

The default on number of strongest coupling neighbors is 10; which means

Only outputting the 10 strongest neighbors (including self)

The default percentage threshold for ignoring mutual capacitance /inductance is 0.005; which means

If the mutual capacitance or inductance is less than the 0.5% of the minimum of the two self-capacitances / inductances,

XtractIM will not output the mutual capacitanceor inductance.

#### **Save Workspace and Layout File**

You can see the save and open icons on the toolbar menu.



#### **Save Workspace File**

Method 1

Select

Workspace > Save As

The Save Workspace File dialog opens.

Save Workspace	File	? ×
Save in:	🔁 Stacked-BGA_Sample_files 💿 🥑 😰 📰 🗸	
My Recent Documents	PoP_flipchip PoP_flipchip-1 POP_wirebond	
My Documents		
My Computer		
	File name:	<u>S</u> ave
My Network	Save as type: Extractor Workspace XML Files (*.xml)	Cancel

	Method 2 Click on  next to the Save  button, select Save Workspace File from the drop-down menu.
	Save Workspace File Save Layout File
Save Layout I	File
	Click on 🔹 next to the Save 📃 button, select <b>Save Layout File</b> from the drop-down menu.
	Save Workspace File
	Save Layout File

#### **RUN THE SIMULATION**

Click on the Play button at the top of the window to start the extraction (simulation).

XtractIM only extracts RLCG for the net which has at least one pin at the Die-side and at least one pin at the board side. At the beginning of the simulation, if some nets have Die-Board mis-match, a pop-up window asks you to select the next action.

- **Continue** Continue the simulation.
- More Information Examine what nets are mis-matched.
- **Stop** Cancel the simulation.

The **More Information** window lists all the mis-matched nets. You can investigate them to see whether it is a special design or a defective design. You can then decide whether or not to proceed with the simulation.



Choose Continue, Stop or More Information. If 30 seconds pass and the user has not made a choice, by default, the simulation continues.

#### **OBSERVE AND SAVE SIMULATION RESULTS**

XtractIM calculates each net's resistance, self loop inductance, conductance, and self capacitance as well as its mutual loop inductance and mutual capacitance with other nets.

The inductance and capacitance are matrices. For example, a simple group of four nets has the following inductance and capacitance matrix.

$\begin{bmatrix} L_{11} & L_{12} & L_{13} & L_{14} \end{bmatrix}$	$\begin{bmatrix} C_{11} & C_{12} & C_{13} & C_{14} \end{bmatrix}$
$L_{21}$ $L_{22}$ $L_{23}$ $L_{24}$	$C_{21}$ $C_{22}$ $C_{23}$ $C_{24}$
$L_{31}$ $L_{32}$ $L_{33}$ $L_{34}$	$C_{31}$ $C_{32}$ $C_{33}$ $C_{34}$
$\begin{bmatrix} L_{41} & L_{42} & L_{43} & L_{44} \end{bmatrix}$	$\begin{bmatrix} C_{41} & C_{42} & C_{43} & C_{44} \end{bmatrix}$

In the Inductance Matrix, the Diagonal Element is the Self Inductance of each net, and the off-diagonal elements are mutual Inductance.

There are two concepts of capacitance matrix: Maxwell capacitance matrix and SPICE capacitance matrix.

- Maxwell Capacitance Matrix Each diagonal element is the loading capacitance (for example, capacitance to ground when other nets are grounded which represents the worst-case capacitive loading). Off-diagonal elements are mutual capacitance with negative values.
- SPICE Capacitance Matrix Each diagonal element is capacitance to ground. Off-diagonal elements are mutual capacitance with positive values.

The relationship between Maxwell capacitance and SPICE capacitance matrix is shown below.

$$C_{ij}(SPICE) = -C_{ij}(Maxwell)$$

$$C_{ii}(Maxwell) = \sum_{j} C_{ij}(SPICE)$$

$$C_{ii}(SPICE) = \sum_{j} C_{ij}(Maxwell)$$

In RLC Per Net view, there are two options:

- Mutual Term View Mutual inductance or SPICE mutual capacitance.
- Self-Term View Resistance, self-inductance or Maxwell diagonal capacitance.

You can choose to view resistance, self-inductance, self-capacitance for each net.

You can also view mutual terms if inductance and capacitance are desired. Usually conductance is very low, so there is no view for conductance.

#### **Display Results**

Upon finishing the simulation, the defaulted result display is a SPICE model.

XtractIM - POP_wirebond.xml - [Cir	rcuit Topology Result]	
🔶 File Window Help		_ 8 ×
🗄 🗋 💕 🛒 🔹 🔰 🕨 🚺 💼 🖬	📰 😂 🤊 - (** - 🔄 🖸 🖸 🖪 Extractor Result 🔍 🏗 🕆 🛸 🛸 🛸 🚱 🔹 🕨	
Workflow: XtractIM ×	Extractor Result	
Default *		
Manage Workspace 📀	View Model Selection	
Load Workspace	© SPICE T-model	
Load a New/Different Layout	O DC_R of Each Path	
Package Setup	RLC of Each Path	
Package Type: Wirebond		
✓ Circuits ✓ Stackup		
V Solder Ball		
Nets		
Simulation Setup 🛛 🙆		
Module: IBIS/RLGC	.SUBCKT POP_wirebond_pop_wirebond_NetBaseSPICE	<b>a</b>
Simulation Type: Net-Based	+ Diel_Diel-12 POPtop-C1 + DOPottom_DOPottom_C1	
View/Export Results 🛛 🙆	+ Diel Diel-135 POPtop POPtop-A3	
Summary	+ POPbottom POPbottom-A3	
SPICE Model	+ Die1_Die1-96 POPtop_POPtop-C12	
Branch RL	+ POPbottom_POPbottom-C12	
Save Results	+ Die1_Die1-51 POPtop_POPtop-M3	-
Load Results		
Customize Workflow ¥		
	Output	×
	Completing Trace Circuits	
	Creating Coupled Trace circuits	
	Preparing Medium for Simulation	
	Computing Edge Reflection Coefficient	
	* Processing Patch02 Patch01	
	Handling Elocing Circuits	
	Modeling Pads	_
	Solving Package and Circuits	=
		-
	Miscellaneous Mesh - Errors VariablesCheck	
Ver: 4.1.2.12213 (SHCN8)	Mouse(mm): X: -8.161, Y: 12.735	1.15

#### **Circuit Topology**

The circuit topology for stacked-BGA is shown in the following illustration. Here we see one net and three branches for Die, BGA1 and BGA2.



#### **Display Results Example**

1. Click on

RLC of Each Path

2. Click to view the Net Length, DC R, Self R, Self L, Self C, or Delay of a Signal Net.

In the example, these path names are used for each of the three paths. The actual Die or BGA circuit name is given to describe each of the three paths.

Die-toBGA1 — U1 ::: POPtop Die-toBGA2 — U1 ::: POPbottom BGA1-toBGA2 — POPtop ::: POPbottom **Extractor Results Display** 



#### **Summary of the Extracted Results**

Click on **Summary** to open the brief summary about the extracted R, L, and C. It shows the maximum (Max) and minimum (Min) values and other information.

XtractIM - POP\_wirebond.xml - [Summary] - 🗆 X 🛟 File Window Help \_ 8 × 🔳 📘 🚥 🔜 🤅 😭 🖤 🗸 (\*\* 🗸 🛄 🗹 🖾 🗄 Extractor Result 🗋 💕 📙 🔹 🔽 🎦 📲 📑 📑 💁 🍳 🕨 Workflow: XtractIM × Extractor Result Default [Version] \$ 4.1.2.12213 [Date] 02/15/2011 0 Manage Workspace [Package Name] C:\SigritySamples\SpeedPKG 4.1\XtractIM\Samples\Stacked-BGA S Load Workspace [Description] C:\SigritySamples\SpeedPKG 4.1\XtractIM\Samples\Stacked-BGA\_S Load a New/Different Layout [Nets Extracted] 55 30MHz Package Setup 0 [Frequency of Extraction] [Max R(mOhm)] 5410.33 Package Type: Wirebond [Min R(mOhm)] 24.8305 Circuits [Max self-inductance L(nH)] 5.04592 Stackup [Min self-inductance L(nH)] 0.204955 🗸 Solder Ball [Max self-capacitance C(pF)] 30.0466 Nets [Min self-capacitance C(pF)] 1.11625 0 Simulation Setup Module: IBIS/RLGC Simulation Type: Net-Based View/Export Results 🛛 🙆 Summary SPICE MOpen the window to view summary. Branch RL Save Results Load Results **Customize Workflow** ¥ • Output х Completing Trace Circuits Creating Coupled Trace circuits ...... Preparing Medium for Simulation Preparing Boundary Condition Computing Edge Reflection Coefficient... \* Processing Patch02 -- Patch01 Connecting Circuits To Patches Handling Floating Circuits Modeling Pads Solving Package and Circuits ... Simulation is in progress. Miscellaneous Mesh - Errors VariablesCheck Ver: 4.1.2.12213 (SHCN8) Nouse(mm): X: -8.161, Y: 12.735 🥚 Ready

A typical Summary display is shown below.

#### **Brand RL and Total C**

Click **Branch RL** to open up a .csv file and display the branch R, L, and C of each net.

If a branch is missing from a net, the cells are left empty.

XtractIM - POP_wirebond.xml - [Bra	nch RL Result]						-	
🛟 File Window Help							_	. 8 ×
: 🗋 📂 💭 - 🛛 🕨 🔳 📘 🚥 🖬	■ 10 - 0	- 🖸 🖸 🖸	Extractor Resu	ut 🔽 🎦 📲	) 🌇 i 🧦 📴 😭	• • •		
Workflow: XtractIM X	Extractor Result							
Default *								
Managa Workenaca	Net Name	C-total (pF)	R Die1(Ohm)	R POPtop(Ohm)	R POPbottom(0	L Die1(nH)	L POPtop(nH)	
	VDD_1	26.748	0.270805	0.027912	0.0251395	0.525405	0.244054	
Load Workspace	VDD_2	27.3953	0.234721	0.0288817	0.025519	0.497138	0.247703	
Load a New/Different Layout	VDD_3	26.6997	0.272649	0.028121	0.0248305	0.526889	0.245555	
Package Setup 🔗	VDD_4	26.9447	0.251421	0.0290218	0.0256632	0.508934	0.248386	
	VDDcore	30.0466	0.135419	0.0504598	0.0490484	0.225419	0.307221	
Package Type: Wirebond	Net_3	1.40488	4.41619	0.665091	0.783387	3.99476	1.05829	
<ul> <li>Circuits</li> </ul>	Net_4	1.16228	3.86269	0.386106	0.386296	3.46211	0.780797	
🗸 Stackup	Net_5	1.11623	3.57821	0.332636	0.33455	3.28026	0.728336	
🗸 Solder Ball	Net_b	1.10024	3.82643	0.377003	0.37666	3.42034	0.76334	
Nets	Net_0	1.00003	4.33303	1.07740	0.00020	4.00434	1.40270	
Cimulation Cotum	Net 10	1.61075	5 26024	1.27270	1.0529	4.33204	1.07007	
Simulation Setup	Net 11	1.49602	1 7/83	0.733669	0.96347	4.33313	1 10822	=
Module: IBIS/RLGC	Net 14	1.40002	4.7403	1 20459	0.30347	4.40030	1.73/11	
Simulation Type: Net-Based	Net 16	1.34963	4.38604	0.562134	0.721594	4.0074	0.94495	
View/Export Results	Net 22	1.62869	4.83984	1 30514	0.803448	4.46348	1 71253	
	Net 25	1 63535	4.82982	0.894715	1 21656	4 43345	1 28396	
Summary	Net 26	1 72337	5 33217	1 33126	1.09529	4 93932	1 74835	
SPICE Model	Net 29	1 22406	4.06227	0 468012	0.467184	3 67226	0.883643	
Branch RL	Net 32	1.2758	3.85571	0.674777	0.457732	3.45881	1.05847	
Save Results	Net 33	1.66076	4.75275	1.29399	0.785142	4.34833	1.67938	
Load Results	Net 35	1.35651	4.55983	0.67165	0.665505	4.17161	1.07761	
	Net_38	1.16016	3.83255	0.384784	0.384587	3.43831	0.775592	
Customize Workflow 🛛 🕹	Net_39	1.36341	4.59499	0.683428	0.677411	4.20605	1.09126	
	Net_40	1.50452	4.4288	1.08353	0.661726	4.03756	1.49004	
	Net_45	1.15811	3.83758	0.380752	0.380407	3.43912	0.773939	
	Net_46	1.28821	4.33734	0.564761	0.561182	3.94382	0.96108	
	Net_47	1.12862	3.71556	0.346689	0.347215	3.32331	0.749508	
	Net_48	1.22499	4.05749	0.469919	0.469022	3.66882	0.884014	
	Net_50	1.11707	3.69161	0.331052	0.331842	3.29201	0.730968	
	Net_51	1.12769	3.72152	0.346351	0.347255	3.3244	0.744237	
	Net_53	1.23698	4.11071	0.486221	0.485359	3.71975	0.903089	
	Net_54	1.13227	3.73696	0.350212	0.350834	3.34174	0.755183	
	Net_55	1.28/16	4.34203	0.562411	0.558506	3.94604	0.958274	
	Net_56	1.2007	4.02094	0.436802	0.436177	3.62003	0.834067	
	Net_61	1.25699	4.17884	0.516009	0.015342	3.79051	0.936123	
	Net_62	1.35094	4.51639	0.662345	0.657402	4.13345	1.06876	-
				111			J	•
Ver: 4.1.2.12213 (SHCN8)	Mouse(mm); X; -8.161	1. Y: 12.735			Readv			

#### **Save Results**

1. In the Workflow pane under View/Export Results, select

#### Save Results

The Save Extractor Result window appears.

Save Extractor R	Result As	? ×
Save in:	🔁 Stacked-BGA_Sample_files 🔹 🌀 🤌 📂 🖽 🗸	
My Recent Documents	<ul> <li>CPU_Info</li> <li>XtractIMRunTimeErro</li> <li>pop_flipchip</li> <li>PoP_flipchip</li> <li>PoP_flipchip-1</li> <li>pop_wirebond</li> <li>POP_wirebond</li> <li>POP_wirebond</li> <li>POP_wirebond_pop_wirebond_CouplingofEachPath</li> <li>POP_wirebond_pop_wirebond_DCResistance</li> </ul>	or
My Documents	POP_wirebond_pop_wirebond_NetBaseSPICE.ckt     POP_wirebond_pop_wirebond_RLCofEachPath     POP_wirebond_pop_wirebond_TableBranchRL     ResourceProfile_XtractIM     Result POP_wirebond_pop_wirebond_021511_141319	
My Computer	Result_POP_wirebond_pop_wirebond_102610_095156  Xtracted_PinNode_Info	>
	File name: Result	ave
My Network	Save as type: All File (*.*)	ncel

- **2.** Enter a file name
- 3. Click on Save. The results are saved in a binary file named Result.
- 4. Click on Cancel if you do not want to save the results in the file name you entered.

#### **Output Files**

The result and result\*.xim files save all the output data The output files on hard disk include:

- One SPICE Circuit File Named \*.ckt.
- **RLC of Each Path File** An .xls file including each Signal Net's Name, Length, DC R, Self R, Self L, Self C and Delay.
- Branch RL File An .csv file including the branch R, L, and total C of each net.

#### **Load in Saved Results**

Saved results can be loaded by selecting

#### Load Results

Load Extractor R	Result(s) From			? X
Look in:	🚞 Stacked-BGA	_Sample_files	🔽 🥝 🤌 🔛 🗔	•
My Recent Documents Desktop	CPU_Info CPU_Info Pop_flipchip POP_flipchip-1 POP_wirebond POP_wirebond POP_wirebond POP_wirebond	pop_wirebond_CouplingofEac pop_wirebond_DCResistance	E XtractIMR	unTimeError
My Documents	POP_wirebond_ POP_wirebond_ POP_wirebond_ POP_wirebond_ ResourceProfile ResourceProfile Result_POP_wire Resul	pop_wirebond_NetBaseSPICE pop_wirebond_RLCofEachPat pop_wirebond_TableBranchR _XtractIM rebond_pop_wirebond_02151 rebond_pop_wirebond_10261	E.ckt th L 1_141319 0_095156	
My Computer	Xtracted_PinNo	de_Info	witchend 102010	<b>&gt;</b>
My Network	Files of type:	All File (*.*)	wirebonia_102610	Cancel

Choose to view present results or the loaded results.

To unload a loaded result, click on the Unload Extractor Result Icon.



#### **BATCH MODE SIMULATION**

To run a simulation in Batch Mode, follow these steps.

1. Click

Start -> Run

2. Change to the directory where the XtractIM.exe file is located.

Example

If you want to use the project (.spd file) defaulted in the workspace file (.ximx file), enter:

ExtraIM -b "Full\_path\_toMy\_workspace\_File\workspace filename"

If you want to use a different project file other than the one in the .xml file, enter:

ExtraIM -b "Full\_path\_toMy\_workspace\_File\*workspace filename*" "Full\_path\_toMy\_workspace\_File\*new\_spd-filename*"

#### **Saved Output Files**

Upon completing the simulation, all output files, including \*.xls and .csv files are saved automatically in the same directory as the \*.spd file.

# Chapter

## **XtractIM Pin-Based Simulation of a BGA Package**

This chapter takes you through the steps to use the XtractIM tool in the simulation of a BGA package with pin-based Extraction.

#### SIMULATION SETUP

A typical workflow in interaction mode is the same as net-base extraction.

#### **Single-BGA Package**

A qualified net is the one which has at least one pin in each of the die- and BGA- circuits. In addition, no open circuit exists for these pairs of pins.

#### **Stacked-BGA Package**

A qualified net is the one which has at least one pin in each of the die-, BGA-top, and BGA-bottom circuits. In addition, no open circuit exists for these three pins.

XtractIM automatically checks to see if a net is qualified to be a reference net.

#### **Setup Simulation Type**

The Simulation Setup options are located in the menu bar on the left side of the window.

1. Click

Simulation Type

Simulation Setup ->	Simulation Type		
onnaidhonr oordp 7	omaidaon nypo		
10000		1	
Model Extraction			
Hodel Excludedon			
0.0.0	0.000		
<ul> <li>Net-Based</li> </ul>	O Pin-Based		
<b></b>			
OK I	Cancel		

**2.** Select

Pin-based

Simulation Setup -> Simulation Type Model Extraction					
○ Net-Based	Layer	Circuit Name	Circuit Model	Port Reference Reference Net:	O Use Reference Net
	Signal\$136C4EF0M4 Signal\$136C4EF0M4 Signal\$136C4D70M1	POPbottom POPtop	POP_bot POP_top		OUse Reference Node(auto) OUse Reference Node(manual)
					Use Reference Element Element ID
					Pin Groups: 1 X 1

- 3. In the **Reference Net** field, all qualified reference nets are displayed in a list.
- 4. Select **Reference Net** for each layer.

Port Reference Reference Net: VSS VSS	O Use Reference Net  O Use Reference Node(auto)  Use Reference Node(manual)  O Use Reference Element Element ID: (0, 0)  Pin Groups: 1 X 1 ~€	
Ready		

5. Select a ground net as the reference net for a pin-based simulation.

#### **Setup Extraction Frequency**

- **1.** To change the extraction frequency, select
  - Setup > Extraction Frequency

Extraction Frequency			×
Extraction Frequency:	30	MHz	OK Cancel

- 2. Update the data in the pop-up window.
- **3.** Use the Threshold for Exporting Coupling Terms window to change the default value. The default value is 30MHz.

#### **Setup Threshold for Exporting Mutual Terms**

Use the XtractIM options to reduce the size of the output circuit during the export stage. XtractIM captures all the coupling during the extraction stage.

1. Open

Setup > Threshold for Exporting Coupling Terms

A pop-up window opens.

Threshold for Exporting Coupling Terms	×
Number of strongest neighbors to export 10	
In addition,	
Ignore mutual C if the ratio of mutual over self terms is less than	0.005
Ignore mutual L if the ratio of mutual over self terms is less than	0.005
OK Cancel	

2. Choose the number of strongest coupling neighbors to be kept in the circuit model.

The default number of strongest coupling neighbors is 10 (including self).

**3.** Ignore mutual capacitance or inductance if the ratio of mutual terms over self term is less than a percentage.

The default percentage threshold for ignoring mutual capacitance/inductance is 0.005.

If the mutual capacitance / inductance is less than the 0.5% of the minimum of the two self-capacitances / inductances, XtractIM does not output the mutual capacitance / inductance.

#### **VIEW / EXPORT RESULTS**

The View/Exports Results options are displayed in the menu bar on the left side of the window.

Click on **Summary** to open the summary that shows the maximum and minimum R, L, C, and other information.

+XtractIM - POP_wirebond.xml - [Su	immary] _ 🗆 🗙
🛟 File Window Help	_ <i>6</i> ×
🗄 🗋 💕 🛃 📲 🔰 🕨 🕨 📕 🔳 👘	🚃 📴 🤟 - 🔍 - 💭 🖸 🚺 Extractor Result 💿 🖬 📲 📲 🐉 🚱 💿 🕨
Workflow: XtractIM ×	Extractor Result
Default 🔗	[Version] 4.1.3.02141
Manage Workspace         Load Workspace         Load Workspace         Load New/Different Layout         Package Setup         Package Type: Wirebond         Circuits         Stackup         Solder Ball         Nets         Simulation Setup         Module: IBIS/RLGC         Simulation Type: Net-Based         View/Export Results         Summary         SPICE Model         Branch RL         Save Results         Load Results	[Version]4.1.3.02141[Date]02/16/2011[Package Name]C:\SigritySamples\SpeedPKG 4.1\XtractIM\Samples\Stacked-BGA_S[Description]C:\SigritySamples\SpeedPKG 4.1\XtractIM\Samples\Stacked-BGA_S[Nets Extracted]55[Frequency of Extraction]30MHz[Max R(mOhm)]5410.33[Min R(mOhm)]24.8305[Max self-inductance L(nH)]5.04592[Min self-capacitance C(pF)]30.0466[Min self-capacitance C(pF)]1.11625
Customize Workflow ¥	
	Output     X       Completing Trace Circuits     Freparing Coupled Trace circuits       Preparing Medium for Simulation     Preparing Boundary Condition       Computing Edge Reflection Coefficient     *       * Processing Patch02 Patch01     Connecting Circuits To Patches       Handling Floating Circuits     Modeling Package and Circuits       Solving Package and Circuits     Image: Solving Package and Circuits       Simulation is in progress.     Image: Solving Package and Circuits
Ver: 4.1.3.02141 (SHCN8) M	louse(mm): X: -2.123, Y: 13.074

#### **SPICE Model**

Click on SPICE Model. The SPICE Model name \*.ckt is loaded.



# Chapter

## **TCL Command Support for Workspace Setup**

This chapter introduces TCL command for workspace setup in the XtractIM tool.

#### INTRODUCTION

TCL (Tool Command Language) scripts can be used to configure and automate frequently used command in Allegro Sigrity tools. They can also be launched outside the Sigrity tools in batch mode to automate company design flows.

New TCL command for XtractIM is developed to support workspace setting. Three types of new TCL command are available, including Setting up TCL, Doing Simulation TCL, and Creating Report TCL.

For the other existing TCL command, please refer to *Tcl\_Scripting\_Reference.pdf* in <ASI\_INSTALL\_DIR>\Update3\Doc\Common Documents\ for details.

#### **SETTING UP TCL**

• Update Package Type

**Format:** sigrity::update PackageType -dieType|d {0-2} -bgaType|b {0-2} -attachType|a {0-2} -leadType|l {0-2}

Package Setup ->	Package Type		
<ul> <li>Single Die</li> </ul>	O Stacked Die	O Side-by-side Die	
Single BGA	O Stacked BGA	OLeadframe	
O Wirebond	Flip-Chip (WL-CSP)	OBoth	
ОК	Cancel		

• Update Circuits

**Format:** sigrity::update Circuits -dieCkts|d {circuit name} -boardCkts|b {circuit name} - capCkts|c {circuit name} -wbCkts|w {circuit name}

		Ckt Type	
1	Cap0402		
2	Cap0402		
3	Cap0402		
24	Cap0402		
:5	Cap0402		
6	Cap0402		
.7	Cap0402		
.8	Cap0402		
	FC	Die	
GAI	untited_pac	Board	

Add Layer

**Format:** sigrity::add Layer {layer type} -above | -under {layer name} -name {new name} -circuit {die/BGA name} -bind {circuit name} -PCBAbove

Layer Mana	ger -> Sta	ick Up											□ ×
Stack Up	Pad Stac	k											
Layer #	Color	Layer Icon	Layer Name	Thickness(	Material	Conductivity(S	Fill-In Dielectric	Permittivity	Loss Tangent	Shape Name	Trace Width(mm)	Trapezoidal Angle(°)	Roughness
1			Signal01	0.001		5.8e+007		[1]	[0]	Shape002	0.1	90	0
			Bump01	0.1		0		1	0				
2			Signal04	0.001		5.8e+007		[1]	[0]		0.1	90	0
			Bump02	0.1		0		1	0				
3			Signal\$M1	0.015		5.8e+007		[2.6]	[0]		0.1	90	0
			Medium\$dielectric2	0.125		0		4.2	0				
4			Signal\$VDD	0.02		5.8e+007		[4.2]	[0]	Shape\$VDD	0.1	90	0
			Medium\$dielectric3	0.25		0		4.2	0				
5			Signal\$VSS	0.02		5.8e+007		[4.2]	[0]	Shape\$VSS	0.1	90	0
			Medium\$dielectric4	0.125		0		4.2	0				
6			Signal\$M4					[2.6]					
			Solderball01	0.3		0		1	0				
7			Signal02	0.001		5.8e+007		[2.5]	[0]		0.1	90	0
			Medium01	0.05		0		4	0				
8			Signal03	0.03556		5.95e+009		[2.5]	[0]	Shape001	0.1	90	0
			Solderball02	0.5		0		1	0				
9			Signal05	0.001		5.8e+007		[2.5]	[0]		0.1	90	0
			Medium02	0.05		0		4	0				
10			Signal06	0.03556		5.95e+009		[1]	[0]	Shape003	0.1	90	0
1					111								•
										_			
Total Thick	ness: 1.7	451e+000 mm	n							Enfo	rce causality	View Material	Import
Solder I	Ball Layer	Bump La	yer							Ð	port Auto Set	Layer Special Void	Filter
										Unit: mm	ОК	Cancel	Apply

Update Attributes

•

**Format:** sigrity::update Attributes -circuit|c {circuit name} -Dmax {value} -D1 {value} -D2 {value} -HT {value} -conductivity|o {value} -mediumThickness|mt {value} -D {value} -Lu {value} -W {value} -Ll{value} -T {value} -H {value}

Package Setup -	> Bumps									×
Layer Name	Circuit Name	Dmax	(mm) D	1 (mm)	D2 (mm)	HT (mm)	Material	Condu	uctivity (S/m)	
Bump02	U1	0.1	0.	.08	0.08	0.1		5e7		Bump Model
										⊌—D1⊌
ОК	Cancel	1								
Package Setup ->	Solder Ball	Denen (mer)	D1 (mm)	D2 (mm	) IT (mm)	Madavial	Candust	uites (C (m)	Madi m Thidman (ma)	X (III D BALL)
Calderhall02	Circuit Name	Dinax (mm)	0.2	0.2	0.051	Material	Conduca 5-7	vity (S/m)	Medium miccress (mm)	Solder Ball Model
Solder Dalloz	DOMI	0.4	0.5	0.5	0.951		Jer		0.05	
										Dmax -
										Medium Thickness
										Ground
OK	Cancel									
Package Setup	-> Lead									

Package S	etup -> Lea ified Setup	d Os	itandard S	etup								×
Layer Name	Circuit Name	D (mm)	Lu (mm)	W (mm)	LI (mm)	T (mm)	H (mm)	Material	Conductivity (S/m)	Medium Thickness (mm)	w	
												Ξ. H
												Medium thickness
												Ground
OK		Cancel										



Update Options

•

**Format:** sigrity::update Options -meshEdgeLength|m {value} -simplifyGeometry|s {0|1} -coarseMesh|c {0|1} -narrowGapModeling|n {0|1} -modelCoplanarTraces|pl {0|1} -filterSignalNets|f {0|1} -enforceCausality|e {0|1} -enhancePadAntipad|a {0|1} -detect-ViaClearance|d {0|1} -temperature|t {value} -solver {value}

Νοτε	The unit for <u>value</u> is <b>meter</b> .
Νοτε	The command option "-dieType d" can be "-dieType" or "-d".

File 🙆		
Conoral	<pre>2</pre>	Change the 'Mark' entions in VtnestTM
File Manager		- So change the Mesh options in Atractim
Save Options		
Hotkeys		Maximum Mesh Edge Length
Layout 🤇		
Grid and Unit	-	0.99 mm Reset
View		This is the constraint on the maximum length of the triangles in the mech for finite element simulation in
Processing		the field domain. The default value is obtained from the package size.
Trace		
Error Checking		Mesh quality and coarse ontion
3D Layout View 🤄	2	
Display		Simplify the geometry to improve mesh quality
Quality		Coarse Mesh
Simulation (Basic) 🛛 🤇		This option is used when the user would like to run the simulation with a coarser mesh which means a
General		mesh with less nodes. The size of the mesh will be automatically adjusted. The option may lead to less
Net and Coupling		accurate result and is not recommended unless a normal simulation runs out of memory.
Special Void		
Output SPICE Circuit		
Report		
Simulation (Advanced)	2	
Electric Models		
Mesh		
Nets and Shapes		
Field Solver Engine		
		Default Apply OK Cancel
tions		
File 🤅	•	
General		🙀 Change the 'Nets and Shapes' options in XtractIM
File Manager		
· · · · · · · · · · · · · · · · · · ·		
Save Options		
Save Options Hotkeys		Net Options
Save Options Hotkeys Layout	2	Net Options
Save Options Hotkeys Layout ( Grid and Unit	<u></u>	Net Options
Save Options Hotkeys Layout ( Grid and Unit View	<u>&gt;</u>	Net Options Filter signal nets
Save Options Hotkeys Layout ( Grid and Unit View Processing	<u>&gt;</u>	Net Options           Filter signal nets           If there are too many signal nets in the design, those far away from the ones of interest can be turned off
Save Options Hotkeys Layout ( Grid and Unit View Processing Trace	<u>&gt;</u>	Net Options           Filter signal nets           If there are too many signal nets in the design, those far away from the ones of interest can be turned off automatically to accelerate the simulation.
Save Options Hotkeys Layout ( Grid and Unit View Processing Trace Error Checking	<u>&gt;</u>	Net Options           Filter signal nets           If there are too many signal nets in the design, those far away from the ones of interest can be turned off automatically to accelerate the simulation.
Save Options Hotkeys Grid and Unit View Processing Trace Error Checking 3D Layout View	<u>)</u>	Net Options           Filter signal nets           If there are too many signal nets in the design, those far away from the ones of interest can be turned off automatically to accelerate the simulation.
Save Options Hotkeys .ayout Grid and Unit View Processing Trace Error Checking 3D Layout View Display	2	Net Options           Filter signal nets           If there are too many signal nets in the design, those far away from the ones of interest can be turned off automatically to accelerate the simulation.
Save Options Hotkeys .ayout ( Grid and Unit View Processing Trace Error Checking 3D Layout View ( Display Quality	<u>)</u>	Net Options         Filter signal nets         If there are too many signal nets in the design, those far away from the ones of interest can be turned off automatically to accelerate the simulation.
Save Options Hotkeys Layout ( Grid and Unit View Processing Trace Error Checking 3D Layout View ( Display Quality Simulation (Basic) (	<u>)</u> ) )	Net Options         Filter signal nets         If there are too many signal nets in the design, those far away from the ones of interest can be turned off automatically to accelerate the simulation.         Shape Options
Save Options Hotkeys Layout ( Grid and Unit View Processing Trace Error Checking 3D Layout View ( Display Quality Simulation (Basic) ( General	<u>ଚ</u> ଚ ଚ	Net Options         Filter signal nets         If there are too many signal nets in the design, those far away from the ones of interest can be turned off automatically to accelerate the simulation.         Shape Options         Consider coupling between field domains through narrow gaps
Save Options Hotkeys Layout Grid and Unit View Processing Trace Error Checking 3D Layout View Display Quality Simulation (Basic) General Net and Coupling	<u>)</u>	Net Options         Filter signal nets         If there are too many signal nets in the design, those far away from the ones of interest can be turned off automatically to accelerate the simulation.         Shape Options         Consider coupling between field domains through narrow gaps         Detect and model the coolanar traces coupling with field domains
Save Options Hotkeys Layout ( Grid and Unit View Processing Trace Error Checking 3D Layout View ( Display Quality Simulation (Basic) ( General Net and Coupling Special Void	<u>)</u>	Net Options         Filter signal nets         If there are too many signal nets in the design, those far away from the ones of interest can be turned off automatically to accelerate the simulation.         Shape Options         Consider coupling between field domains through narrow gaps         Detect and model the coplanar traces coupling with field domains
Save Options Hotkeys Layout ( Grid and Unit View Processing Trace Error Checking 3D Layout View ( Display Quality Simulation (Basic) ( General Net and Coupling Special Void Output SPICE Circuit	<u>)</u> )	Net Options         Filter signal nets         If there are too many signal nets in the design, those far away from the ones of interest can be turned off automatically to accelerate the simulation.         Shape Options         Consider coupling between field domains through narrow gaps         Detect and model the coplanar traces coupling with field domains
Save Options Hotkeys .ayout (* Grid and Unit View Processing Trace Error Checking 3D Layout View (* Display Quality Simulation (Basic) (* General Net and Coupling Special Void Output SPICE Circuit Report	0	Net Options         Filter signal nets         If there are too many signal nets in the design, those far away from the ones of interest can be turned off automatically to accelerate the simulation.         Shape Options         Consider coupling between field domains through narrow gaps         Detect and model the coplanar traces coupling with field domains
Save Options Hotkeys Layout ( Gid and Unit View Processing Trace Error Checking 3D Layout View ( Display Quality Simulation (Basic) ( General Net and Coupling Special Void Output SPICE Circuit Report Simulation (Advanced) (	0 0 0	Net Options         Filter signal nets         If there are too many signal nets in the design, those far away from the ones of interest can be turned off automatically to accelerate the simulation.         Shape Options         Consider coupling between field domains through narrow gaps         Detect and model the coplanar traces coupling with field domains
Save Options Hotkeys Layout ( Grid and Unit View Processing Trace Error Checking 3D Layout View ( Display Quality Simulation (Basic) ( General Net and Coupling Special Vold Output SPICE Circuit Report Simulation (Advanced) (	<u>ଚା</u> ଚା	Net Options         Filter signal nets         If there are too many signal nets in the design, those far away from the ones of interest can be turned off automatically to accelerate the simulation.         Shape Options         Consider coupling between field domains through narrow gaps         Detect and model the coplanar traces coupling with field domains
Save Options Hotkeys Layout ( Grid and Unit View Processing Trace Error Checking 3D Layout View ( Display Quality Simulation (Basic) ( General Net and Coupling Special Void Output SPICE Circuit Report Simulation (Advanced) ( Electric Models Mesh	<u>ତ</u> ବା ବା	Net Options         Filter signal nets         If there are too many signal nets in the design, those far away from the ones of interest can be turned off automatically to accelerate the simulation.         Shape Options         Consider coupling between field domains through narrow gaps         Detect and model the coplanar traces coupling with field domains
Save Options Hotkeys Layout (* Grid and Unit View Processing Trace Error Checking 3D Layout View (* Display Quality Simulation (Basic) (* General Net and Coupling Special Void Output SPICE Circuit Report Simulation (Advanced) (* Electric Models Mesh Nets and Shapes]	0 0 0	Net Options         Filter signal nets         If there are too many signal nets in the design, those far away from the ones of interest can be turned off automatically to accelerate the simulation.         Shape Options         Consider coupling between field domains through narrow gaps         Detect and model the coplanar traces coupling with field domains
Save Options Hotkeys Layout ( Grid and Unit View Processing Trace Error Checking 3D Layout View ( Display Quality Simulation (Basic) ( General Net and Coupling Special Void Output SPICE Circuit Report Simulation (Advanced) ( Electric Models Mesh Nets and Shapes Field Solver Engine	<u>0</u> <u>0</u> <u>0</u>	Net Options         Filter signal nets         If there are too many signal nets in the design, those far away from the ones of interest can be turned off automatically to accelerate the simulation.         Shape Options         Consider coupling between field domains through narrow gaps         Detect and model the coplanar traces coupling with field domains
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Save Options Hotkeys Layout ( Grid and Unit View Processing Trace Error Checking 3D Layout View ( Display Quality Simulation (Basic) ( General Net and Coupling Special Void Output SPICE Circuit Report Report Electric Models Mesh Nets and Shapes Field Solver Engine	<u>ହା</u> ହା	Net Options         Filter signal nets         If there are too many signal nets in the design, those far away from the ones of interest can be turned off automatically to accelerate the simulation.         Shape Options         Consider coupling between field domains through narrow gaps         Detect and model the coplanar traces coupling with field domains
Save Options Hotkeys Layout Grid and Unit View Processing Trace Error Checking 3D Layout View Display Quality Simulation (Basic) General Net and Coupling Special Void Output SPICE Circuit Report Simulation (Advanced) Electric Models Mesh Nets and Shapes Field Solver Engine	<u>()</u> () () ()	Net Options         Filter signal nets         If there are too many signal nets in the design, those far away from the ones of interest can be turned off automatically to accelerate the simulation.         Shape Options         Consider coupling between field domains through narrow gaps         Detect and model the coplanar traces coupling with field domains
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Save Options Hotkeys Layout ( Gid and Unit View Processing Trace Error Checking 3D Layout View ( Display Quality Simulation (Basic) ( General Net and Coupling Special Void Output SPICE Circuit Report Simulation (Advanced) ( Electric Models Mesh Nets and Shapes] Field Solver Engine	<u>0</u> 0 0	Net Options         Filter signal nets         If there are too many signal nets in the design, those far away from the ones of interest can be turned off automatically to accelerate the simulation.         Shape Options         Consider coupling between field domains through narrow gaps         Detect and model the coplanar traces coupling with field domains
Save Options Hotkeys Layout ( Grid and Unit View Processing Trace Error Checking 3D Layout View ( Display Quality Simulation (Basic) ( General Net and Coupling Special Void Output SPICE Circuit Report Simulation (Advanced) ( Electric Models Mesh Nets and Shapes Field Solver Engine	<u>0</u> <u>0</u> <u>0</u>	Net Options         Filter signal nets         If there are too many signal nets in the design, those far away from the ones of interest can be turned off automatically to accelerate the simulation.         Shape Options         Consider coupling between field domains through narrow gaps         Detect and model the coplanar traces coupling with field domains
Save Options Hotkeys Layout ( Grid and Unit View Processing Trace Error Checking 3D Layout View ( Display Quality Simulation (Basic) ( General Net and Coupling Special Void Output SPICE Circuit Report Simulation (Advanced) ( Electric Models Mesh Nets and Shapes] Field Solver Engine	<u>()</u> () () ()	Net Options         Filter signal nets         If there are too many signal nets in the design, those far away from the ones of interest can be turned off automatically to accelerate the simulation.         Shape Options         Consider coupling between field domains through narrow gaps         Detect and model the coplanar traces coupling with field domains
Save Options Hotkeys Layout ( Grid and Unit View Processing Trace Error Checking 3D Layout View ( Display Quality Simulation (Basic) ( General Net and Coupling Special Void Output SPICE Circuit Report Simulation (Advanced) ( Electric Models Mesh Nets and Shapes] Field Solver Engine	<u>0</u> <u>0</u> <u>0</u>	Net Options         Filter signal nets         If there are too many signal nets in the design, those far away from the ones of interest can be turned off automatically to accelerate the simulation.         Shape Options         Consider coupling between field domains through narrow gaps         Detect and model the coplanar traces coupling with field domains

Options	Х
Options  File General File Manager Save Options Hotkeys Layout Grid and Unit View Processing Trace Error Checking 3D Layout View Oisplay Quality Simulation (Basic) General Net and Coupling Special Void Output SPICE Circuit Report Simulation (Advanced) Electric Models Mesh Nets and Shapes Field Solver Engine	×     Change the 'Electric Models' options in XtractIM     Pad and Antipad     ✓ Use enhanced Pad/Antipad model to extract the capacitances     ✓ Detect actual via dearance     Dielectric Materials     Enforce causality in material parameters (option also available in the Stackup dialog)     Set Temperature     Temperature     Z5.000000 °C
	Default Apply OK Cancel

• Update Extraction Frequency

Format: sigrity::update ExtractionFreq {Value}

Extraction Frequency			×
Extraction Frequency:	30	MHz	OK Cancel

NOTE	Ξ
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The unit for <u>value</u> is **Hz**.

Update Mode

Format: sigrity::update Mode {Value}

value: "Extraction" | "EPA"

XtractIM - Untitled - [flipchip.spd	Layer Vie	w]			
🗇 Workspace Edit View	Mode	Setup	Tools	Windo	w Help
🗋 💕 🛃 🕶 🕕 🕨 🔳	Mod	lel Extracti	on	1	3 4€
All Enabled Net(s) 🔻 🖓 🗕	✓ Elec.	. Perf. Asse	essment (E	PA)	s 🖙 🔖

• Update Simulation Type

Format: sigrity::update SimType {Value} value: "Net-based" | "Pin-base"



Update Reference Net

•

Format: sigrity::update RefNet {Net name}

Model Extraction				Port Reference
○ Net-Based	Layer	Circuit Name	Circuit Model	Reference Net:
	Signal\$M1	U1	FC	VDD 1 Use Reference Node(auto)
	Signal\$M4	BGA1	untitled_package	VDD 1 Use Reference Node(manual)
				Use Reference Element Element ID: (0, 0)
				Pin Groups: 1 X 1
				O Use Grouped pins in MCP Header
				Load MCP header file:
OK Cancel				

• Update Coupling

**Format:** sigrity::update Cpl -risetime {number} -percent {number} -all –group{power, ground, signal, unnamed}

Net Manager			×
Net		• P Show Co	supled I 👻
Net List (Sort enabled first)	%Coupling	Rise Time (ps)	A
Unnamed Net(s	3	100	
PowerNets	3	100	
VDDcore			1
✓ VDD_1			
VDD_2			
✓ V00_3			-
VDD_4			
😑 🗹 🛛 🛃 GroundNets	3	100	
🗹 🗹 VSS			
DEFAULT	3	100	
Net_1	3	100	
Net_2	3	100	
Net_3	3	100	
Net_4	3	100	
Net_5	3	100	
Net_6	3	100	
Net_7	3	100	
Net_8	3	100	
Net_9	3	100	
Net_10	3	100	
✓ Net_11	3	100	
✓ Net_12	3	100	
Net_13	3	100	
✓ Net_14	3	100	
✓ Net_15	3	100	
✓ Met_16	3	100	. v
General Keep shape enabled when Gray Disabled	the net is disal	oled	abled
Coupled Lines Disable Coupled Line Simula Coupled Lines Report	ation		
Layer Selection Net Manag	er		

#### **DOING SIMULATION TCL**

Format: sigrity::begin simul

#### **CREATING REPORT TCL**

Format: sigrity::do GenReport -template {File Name Path}

Format: sigrity::save Report –Filename|F {New File name Path}

#### ELECTRICAL PERFORMANCE ASSESSMENT (EPA) TCL

Format: sigrity::update PGAnalysis -inductanceAndCapacitance|i {0-1} -bbandImpedance|b {0-1} -freq|f {Value in GHz} -groupedPinProps|g {0-1} -dcResistance|d {0-1} -loopInductance|l {0-1} -perPinRLSide|p {0-2} -pinGroupX|x {Value} -pinGroupY|y {Value} -nets|n {Net names} -all

Format: sigrity::update SignalAnalysis -impedance|i {0-1} -coupling|c {0-1} -mutualLC|m {0-1} -loss|l {0-1} -freq|f {Value in GHz}

Format: sigrity::update CurrentAnalysis -checkCurrentDensity|c {0-1} -nets|n {Net names} - sinkCurrent|s {Value in A} -all

#### **USER-FRIENDLY DESIGN**

In the TCL Command window, three user-friendly functions are designed.

You can:

- Choose TCL command with the same keyword from the pull-down menu
- Click to get the TCL command history
- Refer to the auto-tips presented when you are typing the TCL command

	TCL Command	ł			
	sigrity::	_		Click to got history	
н	sigrity::add	*		Click to get history	
	sigrity::begin				
	sigrity::check	=	CL Reader		
	sigrity::clear	_	: 12.654, Y: -10.692		Ready
_	sigrity::close				
	sigrity::cls				
	sigrity::copy				
	sigrity::delete				
	sigrity::do				
	sigrity::end	-			

TCL Command	x
sigrity::update PackageType -dieType {0} -bgaType {0} -attachType {1 sigrity::update PackageType -dieType d {0-2} -bgaType b {0-2} -attachType a {0-2} -leadType {0-2} I	
TCL Command TCL Reader	

# Chapter

### **Error Checking Your Files**

Cadence provides a number of tools to help error check your files before running a simulation. Some file errors can be hard to find. For example, you may think a trace is connected to a via — they appear overlapped with each other — but actually, the nodes of the trace and the via may not be connected.

Using the error checking tools of the software, you can easily spot these kinds of drawing problems. Another kind of error is related to our internal computation models and their need to numerically discretize the geometries.

#### **USING THE ERROR CHECKING TOOLBAR**

The Error Checking Tools can assist you in finding different types of warnings and errors. Whenever a problem is detected during error checking procedures, an error or warning symbol appears in the problem area.

#### **Error Symbols**

The error symbols are similar to the button icons in the toolbar. There are four types of warnings and two types of errors.



#### **Display the Error Check Toolbar**

Select

View > Toolbar > Checking

#### **UNDERSTANDING THE OUTPUT WINDOW**

The Output window allows you to view warnings and errors at a glance whenever you open a .spd file. These tabs are located located at the left-side of the lower window.

- Mesh Errors Lists all the GUI related errors that you can use the Error Checking toolbar to find. This tab lists all the warnings and errors that the application finds.
- Miscellaneous Lists all the errors inherent in a given file, such as an incomplete partial circuit definition or layers with a thickness of **0**.
- Variables Check Lists all the variables checked.

To display the Output Window, select

View > Output Window

#### **Check for Warnings & Errors**

- 1. Select which package elements you want to display or hide. Choose from:
  - Nodes
  - Pads
  - Shapes
  - Traces
  - Vias
  - Wirebonds
- 2. Use the bottom buttons of the Layer Selection dialog.



3. Choose the types of warnings and errors that you want to find.

Via Placement and Node Placement errors are the default choices.

- **4.** Press **(C)** to check for errors on the active layer.
- 5. Press (1) to check for errors on all layers.

Warnings and errors found are marked with symbols similar to the buttons on the Checking Toolbar. These errors are listed in the **Output Window** and are marked in the Layer View area.

- 6. Double-click on any error that you wish to view in the **Output Window**. The Layer View window zooms into the area where the error is located.
- 7. Correct any errors or warnings.

**NOTE!** All errors must be corrected prior to simulation.

Mesh Errors Listed in the Output Window

Output X
WARNING [Open Net]: Net Unnamed Net(s) contains two or more disconnected sections. WARNING [Open Net]: Net _Floating_Plane_net contains two or more disconnected sections.
Miscellapeous Mesh - Errors VariablesCheck

#### **Check for Short Circuits**

This feature lets you check for short circuits in your simulation. Short circuit warnings are displayed using a yellow icon. There are three kinds of Short Circuit Nodes:

- Package objects of different nets are connected together.
- Package nodes of different nets are linked to the same circuit.
- A port's positive and negative terminals connected to the same net.



**1.** To start checking select

Tools > Check > Check Activated Layer

or

**Check All Layers** 



Any warnings found are listed in the Output Window and are shown in the Layer View area.

2. Double-click on any warning in the **Output** window. The Layer View window zooms into the area where the short circuit is located or the Circuit Manager is displayed.
# Chapter

## **Case Examples**

This chapter outlines some case examples for various sections of the XtractIM User's Guide.

#### **EXTENDING NODES AND VIAS**

The *Extending Nodes and Vias* illustration represents the nodes and vias that are to be extended vertically.

- Nodes: node06, node07, node08, node09 and node10.
- Vias: via12, via17, via13, via16 and via11.
- Via 12 is terminated at node06 on layer Signal02 and node25 on layer Plane02.
- Node07 does not extend vertically through a via but, via13 is in vertical proximity (to node07) as is via17.
- Via17 and via13 share node26.
- Node28 is the upper node of via16.
- Node29 is the lower node which is in vertical proximity to node138 of layer Signal01.
- Viall is included to complement the example.

**Extending Nodes and Vias** 

The purpose is to insert vias in the following manner:

Isolated node objects extended vertically by the insertion of vias.

Where a via already exists, the via is extended.



Refer back to this illustration as you study the examples in Case 1 and Case 2.

#### CASE 1

The **yellow** via in the Via Extension window shows we want to extend nodes selected from layer Signal02 to layer Signal01.

Only Node09 can be extended as indicated.

All other nodes have existing vias blocking the extension.

Properties of Extended Via(s) 🛛 🗙
Info: Properties will be inherited from the attached via if box is checked. Inherit PadStack
Inherit Net Color
Inherit Conductivity
Vias or nodes cannot be extended :
Vias or nodes can be extended :
VIAUDODU
OK Cancel

#### CASE 2

The **yellow** via shows we want to extend all nodes and vias from layer Signal02 to layer Plane02.

Nodes 9, 8, and 7 can be extended.

Vias 13 and 16 can be extended.

Vias 12, 17 and 11 cannot be extended.

Existing vias are blocking nodes 6 and 10.

Via17 is blocked by via13.

	Properties of Extended Via(s)			
Via Extension   Signal\$TOP   Medium\$2   Signal\$GND   Medium\$4   Signal\$IS3   Medium\$6   Signal\$IS4   Medium\$8   Signal\$VCC   Medium\$10   Signal\$BOTTOM	Info: Properties will be inherited from the attached via if box is checked. ✓ Inherit PadStack ✓ Inherit Net Color ✓ Inherit Conductivity Vias or nodes cannot be extended :			
Undo Redo OK Cancel	Vias or nodes can be extended : Via0650 OK Cancel			

## **Propterties of Extended Vias Window**

Properties of Extended Via(s)	×
Info: Properties will be inherited from the attached via if box is checked. Inherit PadStack	
Inherit Net Color	
Inherit Conductivity	
Vias or nodes cannot be extended :	
Vias or nodes can be extended :	
Via0650	
	6
OK Cancel	

# Chapter

# **Quick GUI Keys**

The Quick GUI Keys are listed and described in the following table.

#### **GUI KEY FEATURES**

FEATURE	KEYS TO PRESS	Notes			
Active layer selection	Up and Down Arrows	Use with the Layer Selection dialog.			
Close windows	ESC	Closes any open dialog box that is currently active.			
Finding objects, opening the Find dialog box	Ctrl + F	Works when the Layer View window is active.			
Show/hide shapes	F7	Works with either Layer View or 3D View windows.			
Area zooming	F2	Zooms into an area. Use the mouse to select wha area you want to magnify.			
Zoom back	F3	Zooms out of an area.			
Zooming in F4		Magnifies a given area. Click the mouse to zoom into an area.			
Zooming out F5		Zooms out of a given area. Click the mouse to zoom out of an area.			
Deleting objects	Delete key	Works when the Layer View window is active, select an object, then press the delete key.			
Circuit linking "turbo" Up, Down, Right and Left		Use these keys to iterate through the partial circu and component name lists and to navigate aroun the Component Manager.			

FEATURE	KEYS TO PRESS	Notes
Create new .spd file	Ctrl + N	XtractIMI must be invoked and the workspace must be empty.
To open a .ximx file	Ctrl + O	XtractIM must be invoked and the workspace must be empty.
To print window contents	Ctrl + P	Use with the Layer View or 3D View window active.
To save the .spd file	Ctrl + S	Use with the Layer View or 3D View window active.
Object Outline Display	Ctrl + Shift + O	Object outlines are toggled.

# Chapter

## **Pin Mapping**

Pin mapping is used to indicate which power and ground buses a given driver, receiver, or terminator is connected. This chapter covers how to use pin mapping in XtractIM.

#### **PIN MAPPING DIALOG**

The **Pin Package Nodes Match** dialog shows the result of name matching and coordinate matching when a partial circuit includes an MCP or CPM sub-circuit. When the dialog opens and name matching is failing, you can match coordinates with the default tolerance automatically one time.

When names are matched, the controls used in the manual match are gray.

Function	Description
Position Tolerance	The tolerances are used in coordinate matching.
Angle Tolerance	The tolerances are used in coordinate matching.
Default	Set the tolerances to default values.
Match	Play coordinate match.
Detail	Show the result of name matching and coordinate matching.
Use manual match	Select two pairs of points to coordinate match.
Flip pins	Flip the pins to match coordinate.
Coord Match	Select the result of coordinate match as the final result.
Name Match	Select the result of name match as the final result.

#### **Pin Package Nodes Match Dialog**

MCP Editor									
✓ Internal Circuit:	FC			<b>T</b>	✓ Internal Circuit	FC			
Connection:		- Type		Del	Connection:		Type:		Del
Ckt Node(*)	Net(*)	X (mm)	Y (mm)	Pin(*)	Ckt Node(*)	Net(*)	X (mm)	Y (mm)	
U1-A1	VSS	-2.5681	2.5681	⊢ U1-A1 →	U1-A1	VSS	-2.5681	2.5681	
U1-A2	Net_18	-2.1011	2.5681	U1-A2 →	U1-A2	Net_18	-2.1011	2.5681	
U1-A3	Net_27	-1.6342	2.5681	← U1-A3 →	U1-A3	Net_27	-1.6342	2.5681	
U1-A4	Net_48	-1.1673	2.5681	U1-A4 →	U1-A4	Net_48	-1.1673	2.5681	
U1-A5	Net_49	-0.7004	2.5681	─ U1-A5 →	U1-A5	Net_49	-0.7004	2.5681	
U1-A6	Net_35	-0.2335	2.5681	U1-A6 →	U1-A6	Net_35	-0.2335	2.5681	
U1-A7	VDD_2	0.2335	2.5681	─ U1-A7 →	U1-A7	VDD_2	0.2335	2,5681	
U1-A8	Net_65	0.7004	2.5681		U1-A8	Net_65	0.7004	2.5681	
U1-A9	Net_73	1.1673	2.5681	U1-A9 →	U1-A9	Net_73	1.1673	2.5681	
U1-A10	Net_82	1.6342	2.5681	← U1-A10 →	U1-A10	Net_82	1.6342	2.5681	-
Pin name pattern:	I e.g.A	[N] will give A	l, A2, in wh	iich, [N] stands for the auto-ge	enerated number. I	N start from: 1			
Pin (FC) Pin (F									
6°1					[	Merge circuit	Save	Clos	e

#### XtractIM User's Guide 16.6

# Index

#### Symbols

.brd 25 .csv file 51, 78, 79, 81 .csv format 46 .sip 25 .spd file 43, 80 .spd file format 10 .spd file format. 10 \*\_t.ckt 54 \*.csv files 54 %Coupling Value 38

#### **Numerics**

3D bonding 25 3D bonding wire profiles 57

#### A

active layer 4 add 20 Add a node 21 added signal layer 64 Angle Tolerance 111 Area 19 areas of this toolbar 20 associated layout file 13 Attach Layout File 8 Attach Layout File window 61

#### В

basic functions 18, 19 Batch Mode 55, 80 Batch Mode Example 56 batch mode simulation 55, 80 beginning of the simulation 73 **BGA1** 75 **BGA2** 75 **BGA-bottom circuits 83** BGA-top 83 binary file 54, 79 Board circuit 30, 64 Board Grid Arra 25 board side 13, 73 Bottom right window 46 Box 21 branch missing from net 78 Branch RL 78 Branch RL file 79

#### С

C4 Bumps settings 34, 65 C4Bump data 57 Cadence 10 can be extended 106 Cancel the simulation 14, 73 cancel your session 62 cannot be extended 106 Capacitance 52 Capacitance Example 44 capacitance matrix 73 capacitance to ground 44, 73 captures all the coupling 85 Case 1 104 Case 2 104 cells are left empty 78 change extraction frequency 40, 70, 85 check errors drawing 97 check results 3, 18 check the simulation results 4 choose from the last few actions 19 Choose the number 41 Circuit data for a Flip-Chip package 29 circuit link 21 circuit model 70 circuit topology 75 Circuits 63 Circuits data 63 circuits setup 29, 63 commands 18 common electrical models 25 common XtractIM commands 18 completing the simulation 57 conductance 43, 73 conductance is very low 74 configuration of the layout file 4 Continue 13 Continue the simulation 73 controls used 111 conventions 2 Coord Match 111 coordinate matching 111 coupled lines 38, 69 coupled transmission line sections 38 coupling 70 coupling element 54 coupling elements 54 coupling neighbors 41, 85 CPM sub-circuit 111

Create a new workspace file 26 Create a Workspace 3 create new workspace 27, 60 created workspace 12 creates a new workspace 60 crosstalk 38 current working paths 10 cut features 21 Cut Objects 21 cut objects 21 cut package objects 20 cuts all objects 21 cutting an area 21 cutting area rules 21

## D

data 70 default choices 98 default number of strongest coupling neighbors 85 default package type 28, 61 default percentage threshold 41, 70, 85 default tolerance 111 default value 85 defective design 14, 73 Delete 20 Delete key 20 deleting objects 109 desired circuit 30, 63 desired Ground Net 66 detail information of the task 17 Diagonal Element 43, 73 diagonal element 44, 73 Die 75 Die circuit 29, 63 Die or BGA circuit name 75 Die side 13 Die-Board mis-match 13, 73 Die-side 73 disabled 21 display 98 display a magnified view 19 Display Results 75 display the Output Window 98 displayed layers 4 Displays a complete row 46 draw 21 DSN 25

#### Ε

easily spot errors/warnings 97

#### Index

Edit Pane 26 Editor Pan 17 Editor pane 4, 12, 17 editor pane 17 educe the size of the output circuit 70 efault value 10 electrical models 25 electrical threshold parameters 38 Empty Signal Layer 32 empty signal layer 64 enabled 21 error 97 symbols 97 error check your files 97 error checking tools 97 Error Checking Toolbar 22 Error Checking toolbar 98 error checking toolbar 22 Error Checking Tools 97 error symbols 97 error that you wish to view 98 errors 98 errors inherent in a given file 98 errors on all layers 98 errors on the active layer 98 Examine what nets are mis-matched 73 Existing vias 106 existing vias 105 export stage 41, 85 Exporting Coupling Terms 85 Exporting Mutual Terms 85 extend all nodes and vias 106 extend nodes 105 extend vias 21 extension .ckt 49 extension .pkg 49 extraced results 55 extract models of full packages 25 extracted R, L, and C 77 **Extraction Frequency 85** extraction frequency 46, 57 extraction stage 41, 70, 85

#### F

File Example 48 file format translators 10 file name 54 finish the setup 64 Fit to display 19 Flip-chip 28 Flip-Chip package 63 Flip-chip package 65 flip-chip packages 25, 57 Folder Browser 11 full RLC matrix 46

#### G

Gray items 10 Ground Nets 35, 66 ground nets 25 GUI related errors 98

## Η

hide 98 Highlight an item 17 hot keys 19, 109

#### 

I/O Buffer Information Specification 25 **IBIS** files 54 **IBIS Model** 49 **IBIS model** 50 IBIS package model 49 IBIS package model files 54 IBIS package pin RLC model 25 IBIS pin model files 54 IC packages 25 ignore mutual capacitance 70 ignoring mutual capacitance or inductance 41 in interaction mode 83 Inductance 52 inductance and capacitance 43 inductance and capacitance matrix 43 Inductance Matrix 43, 73 Input information 17 insert vias 104 Interaction mode 26 interaction mode 59 isolated trace 38

#### L

L and C 54 layer Plane02 103 Layer View window 17 Layout Area 3, 4, 16 layout file 3, 8, 10, 13, 59 layout selection window 4 layout toolbar 19 Layout Window 4 Load a New/Different Layout 27, 60 load an existing file 26, 59 load an existing workspace 27, 57, 60 Load and Unload Result buttons 55 Load Results 55, 80 load saved results 55, 80 Load Workspace 13 loaded result 55 loaded results 55 loaded results 55 loaded results 55

#### Μ

Main Window 15 main window 57 Manage Workspace 4, 5 manual match 111 matrices 43, 73 Maxwell Capacitance 51 Maxwell capacitance and SPICE capacitance matrix 73 Maxwell Capacitance Matrix 73 Maxwell capacitance matrix 44 Maxwell diagonal capacitance 44, 74 **MCM 25** MCP 111 medium layer standing 64 Medium Layer standing for a PCB Medium ILayer 32 menu toolbars 18 Mesh Errors 98 metal layer. 52 mis-matched nets 14, 73 mis-matched nets. 13 modify a design 3, 18 More Information 13, 14 More Information window 73 mouse onto a task 17 **Move 20** multi-conductor transmission lines 38 mutual capacitance 43, 44, 73, 85 mutual capacitance / inductance 86 mutual capacitance /inductance 70 mutual capacitance with negative values 73 mutual capacitance with positive values 73 mutual capacitance/inductance 70 Mutual inductance 44, 74

mutual Inductance 43 mutual inductance 49 mutual loop inductance 43, 73 Mutual Term View 44, 74 mutual terms 85 mutual terms if inductance and capacitance 74 Mutual Terms View 46

#### Ν

Name Match 111 name matching 111 negative terminals 100 negative values 44 net lengt 25 Net Length 75 Net Manager window 35, 66 net resistance 43 net-base extraction 83 Nets 35 nets for extraction 57 nets of a package 57 nets setup 35, 66 New icon 27, 60 new name 12 new pane 63 new pane opens 66 new window 13 new workspace 12, 15, 16, 27 new workspace file 59 no open circuit exists 83 no view for conductance 44 node is unlinked 21 Node Placement errors 98 Node Tool 21 Node07 does not extend vertically 103 Node28 is the upper node 103 Node29 is the lower node 103 nodes and vias that are to be extended vertically 103 number of strongest coupling neighbors 70

#### 0

object display 4 Object Toolbar 20 Objects are cut 21 observe results 43, 73 Off-diagonal elements 44, 73 one pin 83 Open a layout file 26 Open icon 27 open icon 57, 60 open the summary 86 operation button 20 output circuit 41 output control 26 output data 54 output files 10, 54, 57, 79 Output Window 98 Output window 98 overall results 46

#### Ρ

package editing 19 package file 3 package layers 8 package model files 54 Package objects 100 Package Setup 5, 12 Package setup 12 package setup 12 package simulation setup 27, 60 Package Structure 27 Package Type 28, 61 package type 57 package type settings 61 packages 57 packages vary slightly 4 patches on signal layers 21 Path File 79 path names 75 PCB Medium Layer 32 PCB medium layer 64 Pi-circuit 50 pin at the board side 73 pin mapping 111 Pin Model Excel format 51 Pin Model in IBIS Fomat 54 Pin Package Nodes Match 111 Pin Package Nodes Match Dialog 112 Pin-based 84 pin-based extraction 17 plane layers 21 Play button 73 Position Tolerance 111 positive values. 44 PowerNets 35 prepare for a simulation 57 prepare for the simulation 11 project file 56 Property 20

Property Report 20

#### Q

qualified net 83 quick access 18, 20 quick access icons 4 Quick GUI Keys 109

## R

R, L, and C data 46 R/L/C heading 46 R/L/C matrices 46 ratio of mutual terms 70 real life examples 1 rectangular area 19 redo 19 Redo buttons 19 reference ground net 35, 66 reference net 83 related values 52 remove objects 20 reorder the list 46 report results 3, 18 Resistance 44, 52 resistance 73 result 54 result display 74 result file 54 result output file 54, 79 result spd file name.eim 54 result\*.eim file 54, 79 reverse crosstalk 38 Rise Time 38 Rise Time Value 38 **RLC Distributions 52** RLC distributions 52 RLC extraction 35, 66 RLC Full Matrix 54 RLC Full matrix 46 RLC Per Net view 74 RLCG 13, 73 run a simulation 3 run simulation 13, 73 Run the simulation 3 run the simulation 13, 18

#### S

Save as option 43 Save Extractor Result window 53, 78 save layout file 41, 72 save output files 57, 81 save results 43, 53, 73, 78 save the workspace and layout file 43 save workspace 12, 71 saved on hard disk 46 Saved results 80 second Board circuits 64 see the all the toolbars 18 Segment RLC 52, 54 segment RLC 52 Segment RLC in Excel Format 54 Segment RLC values 52 Select 20 Select a package type 26 select an operation 20 select specific objects 20 Select the nets for extraction 26 select the next action 13 select the object 20 select toolbar 20 selected nets of a package 25 selected object 20 selected result 55 self capacitance 43, 73 Self Inductance 73 Self Inductance of each net 43 self loop inductance 43, 73 self term 70 Self Terms View 45 self-C 54 self-inductance 44 self-L 54 self-R 54 Self-Term View 44, 74 set all the parameters 11 Set the C4 Bump data 26 Set the Solder Ball data 26 set up a simulation 3 Set With Default Parameters 69 Setting Output Factors 70 setup a current observation 21 Setup extraction frequency 26 setup installation 18 Setup Solder Ball 66 Setup the circuits 26, 57 Setup the Stackup 57 26 shape toolbar 21 shape tools 21 short circuit checking 100 short circuit is located 101 Short circuit warnings 100 short circuit warnings 22

show/hide icons 5 show/hide shapes 109 signal net 35, 52, 66 signal net length 54 Signal\$Bottom layer 64 simulation 73 simulation progress 4, 18 Simulation Setup 5 simulation setup 26, 59 Simulation Type 83 simulation, prepare 11 single and stacked BGA packages 25 single BGA 26 Single Die, Single BGA, wirebond package 28 single transmission line algorithm 38 Single-BGA net-based 17 single-BGA package 83 size of the output circuit 85 Solder Ball 66 solder ball 64 solder ball data 57 Solder Ball Medium Layer 32 Solder Ball Medium Layer insert 64 Solder Ball model 12 Solder Ball selected 12 Solder Ball settings 66 SPD 25 special design 14 special folders 11 SPICE Capacitance Matrix 73 SPICE capacitance matrix 44 SPICE circuit files 54, 79 SPICE equivalent circuits 25 SPICE file 54 SPICE Model 49 SPICE model 50 SPICE Model name 87 SPICE Model. 87 SPICE mutual capacitance 44, 74 SPICE netlist 25 SPICE sub-circuit 49 SPICE/IBIS Model 51 SPICE/IBIS model 49 SPICE/IBIS Model result view 50 split a trace 21 spreadsheet 4 stacked BGA 26 stacked-BGA 75 Stacked-BGA net-based 17 stacked-BGA package 83 Stackup 32

Stackup window 32 Stackup window opens 64 start icon 13 start the extraction 73 Status Bar 4 status bar 18 Status Bar appears or hides 26 Stop 14 strongest coupling neighbors 41 Summary 46, 54, 77 Summary Content in Excel Format 54 Summary display 77 Summary of Extracted Results 77 Summary, extracted results 46 system requirements 1 system-level analysis 25

#### Т

tabulated data 46 task 17 task is expanded 17 tasks 17 Threshold 85 Threshold for Exporting Coupling Terms 85 T-model 54 Tool Bar 4 tool-tip 17 Top right window 46 total number of each element in the circuit 49 trace 69 Trace nets 38 Trace Operations 21 types of warnings 98

#### U

undo 19 Undo/Redo 19 undo/redo buttons 19 Unload Extractor Result icon 55 Unselect 20 UPD 25 urve graph 19

#### V

Variables Check 98 Version information 18 version information 18 vertical proximity 103

#### Index

Via 12 is terminated at node06 103 Via Extension window 105 Via Operations 21 Via Placement 98 via will be extended 104 Via11 is included 103 Via17 and via13 103 Vias 13 and 16 106 View 20 view 19 View / Export Results 5, 53 view conductance 74 view present results 55 view resistance 44, 74 view results 13 View the item 17 View the results 3 view the results in each selection 14 view warnings and errors 98 View/Exports Results options 86

#### W

warning symbols 97 warnings 97, 98 Warnings and errors 98 warnings prior to running simulations 22 Wirebond 28 wirebond constraints 11 wirebond packages 25, 57 work with shapes 21 Workflow Pane 3, 16, 26 workflow pane 3 Workflow pane appears or hides 26 workflow pane, tasks 17 workflow pane, using 4 Workflow Tasks 4 workflow tasks 3 workspace file 56 Workspace Toolbar 18 workspace toolbar 18 worst-case capacitive loading 44

## X

X, Y coordinates 18 ximx file 80 XtractIM 13, 19, 25, 57, 73 XtractIM commands 4, 18 XtractIM tool. 1 XtractIM.exe file 55

#### Υ

yellow via 100, 105, 106

#### Ζ

zoom functions 19 Zoom in 19 zooming In 109 zooming Out 109 Zoom-out 19