

XtractIM Tutorial

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Table of Contents

1	Introduction	1
	System Requirements	1
	How to Use This Guide	1
	Additional Documentation	1
	Conventions Used in This Guide	1
	How to Contact Technical Support	2
2	Overview	3
	About XtractIM	3
	Model Extraction	4
	RLGC / IBIS Module	4
	Optimized Broadband Module	4
	Electrical Performance Assessment	4
	Power / Ground Distribution System	4
	Signal Distribution System	5
	The XtractIM Window	5
	Using the Toolbar Icons	6
3	IBIS / RLGC Module: Net-Based Simulation Single-Die Single-BGA Packages	7
	Prepare for the Simulation	7
	Lesson One: Simulation Setup	8
	Overview	8
	Load Workspace and Layout File	9
	Select Package Type	9
	Setup Components	11
	Setup Stackup	11
	Setup Bump Medium Layer	12
	Setup Bumps	12
	Setup Solder Ball	13
	Viewing 3D Layout	13
	Setup Nets	16
	Rise Time and %Coupling	17
	Setup Rise Time and %Coupling	17
	Setup Extraction Frequency	18
	Setup Threshold for Exporting Mutual Terms	18
	Lesson Two: Save Work Areas	21
	Tool Bar	21
	Workspace File	21
	Layout File	21
	Lesson Three: Run the Simulation	23
	Start Simulation	23
	Investigate Mis-matched Nets	23
	Lesson Four: Observe and Save Simulation Results	25
	Inductance and Capacitance Matrix Example	25
	Summary of the Extracted Results	26

Save SPICE/IBIS Model Files	27
Save SPICE Model Files	27
Save IBIS Model Files	27
Load Pin Model in Excel Format	28
View DC Resistance	29
View RLC Per Net	31
Save R / L / C Full Matrix	31
View RLC Distributions	33
View Segment RLC	33
Segment RLC Report	35
View RLC vs. Net Length	36
View Signal Nets Crosstalk	36
NEXT and FEXT	36
View Crosstalk Results	38
Change Rise Time	40
Save Simulation Results	40
Simulation Output Files	41
Output Result Displays with Images (PNG or BMP Format)	42
Load in Saved Results	43
Simulation Report with .htm / .html Format	45
Lesson Five: Batch Mode Simulation	47
Lesson Six: Partial Inductance Report for Power/Ground Nets	47
Introduction	47
Lesson Seven: 3D-EM Optional Field Solver in XtractIM	48
Introduction	48
Enabling 3D-EM Field Solver	49
Results Display	51

4 RLG Module: Net-based Simulation of Multi-die Stacked-BGA Packages **53**

Prepare for Simulation	53
Lesson One: Simulation Setup	54
Simulation Overview	54
Setup Package Simulation	54
Setup Package Type	55
Setup Circuits	56
Setup Stackup	57
Setup Bump and Solder Ball Medium Layers	58
Setup Bumps to a Side-by-Side Die Package	59
Output IBIS .pkg Model for Each Die-to-Board Path	61
Lesson Two: Save Work Areas	62
Layout File	62
Workspace	62
Lesson Three: Run the Simulation	63
Investigate Mis-matched Nets	63
Lesson Four : Observe and Save Simulation Results	64
Display SPICE Model Results	64
View DC Resistance	65
Display RLC of Each Path	66
Display Coupling of Each Path	67

Summary of the Extracted Results	68
Branch RL and Total C.....	68
Save Results and Output Files	70
Load in Saved Results and Files.....	71
Lesson Five: Batch Mode Simulation	72

5 Optimized Broadband Module: Net-based Simulation for Single-die Single-BGA Packages or Multi-die, Stacked-BGA Packages- - - - - 73

Lesson One: Setup for the Simulation.....	73
Package and Simulation Setup	73
Simulation Setup.....	74
Output Frequency Range Options	76
Output Original S-parameter with More Format	77
Lesson Two: Save Work Areas.....	78
Layout File.....	78
Workspace	78
Lesson Three: Run the Simulation	79
Investigate Mis-matched Nets	79
Lesson Four : Observe and Save Simulation Results.....	80
About the S - Parameter and Errors.....	80
View S - Parameter and Errors	80
View Net Frequencies	82
View Summaries and Models.....	84
Save and Load Results.....	85
Lesson Five: Broadband Extraction of Existing S-parameter.....	87
Load BNP Files and Setup for Simulation	87
Select Extraction Nets	88
Select Circuit Topology.....	90
Lesson Six: Run a Batch Mode Simulation.....	91

6 RLGC and Optimal Broadband Module: Pin-Based Simulation- - - - - 93

Prepare for the Simulation.....	93
Lesson One: Simulation Setup	94
Simulation Overview	94
Simulation Options	94
Setup Simulation Type	95
Select Reference Node (Manual).....	96
Select Reference Element	97
Select User Grouped Pins in MCP Header	97
Generate MCP Header File.....	100
Setup Extraction Frequency.....	107
Lesson Two: Save Work Areas.....	108
Layout File.....	108
Workspace	108
Lesson Three: Run the Simulation	108
Investigate Mis-matched Nets	109
Lesson Four: Fly-Wirebond Package Model Extraction.....	109
Introduction	109
Workflow.....	109

Result.....	110
View Export Results	111
Optimized Broadband Module	113
Circuit Topology	114
7 IBIS/RLGC Module: Simulation of Leadframe Package - - - - -	115
Prepare for Simulation	115
Lesson One : Simulation Setup	116
Package Type	118
Shape to Trace Conversion.....	120
Setup Circuits and Stackup.....	121
Outer Lead Setup.....	121
Leadframe Data for the Leadframe Package.....	122
Setup Nets.....	124
Extraction Frequency	124
Threshold for Exporting Mutual Terms	124
Lesson Two: Save Work Areas.....	125
Layout File	125
Workspace	125
Lesson Three: Run the Simulation.....	125
Investigate Mis-matched Nets	125
Lesson Four : Observe and Save Simulation Results.....	126
R, L and C	126
Mutual Terms	126
Summary of the Extracted Results	127
SPICE Model Files Saved	127
IBIS Model Saved	127
Pin Model: IBIS Format	127
Pin Model: Excel Format	127
DC Resistance	128
RLC Distributions	128
Segment RLC	128
Save Simulation Results.....	128
Simulation Output Files.....	129
Load in Saved Results	129
Lesson Five: Batch Mode Simulation.....	129
8 Electrical Performance Assessment - - - - -	131
Lesson One: Simulation Setup.....	131
Setup Steps	132
Setup for Power/Ground Analysis.....	132
Setup for Signal Analysis.....	134
Select Automatically Generate and Save Report	136
Save Workspace	137
Lesson Two: Run and Simulation.....	138
Lesson Three: Observe and Save Simulation Results.....	138
Power-Ground Analysis	139
Per Net-Pair Property.....	139
Per Pin Property.....	142
Signal Distribution System Checking	146

Definitions	147
Trace / Wirebond Layout Checking.....	147
Impedance	154
Coupling Coefficient.....	155
Single-Ended and Diff. Pair Net Checking Switching.....	159
Net Couplings	160
Insertion and Return Loss	165
Current Checking.....	166
Save Results.....	173
Load Results	174
Create Report.....	174
Load Previously Saved Results	177
Summary of Electrical Performance Assessment Features	178

9 TCL Command Support for Workspace Setup - - - - - 179

Prepare for the Simulation.....	179
LESSON One: Running TCL Command for Workspace Setup	179
Introduction	179
Single-Die BGA Package Sample	179
Multiple-Die BGA Package Sample.....	185
Stacked-BGA Package Sample	190
LESSON Two: TCL Command Recording Support for Workspace Setup	196
Load Design.....	196
Record TCL Command for Workspace Setup.....	198

10 Network Parameter Viewer - - - - - 201

Load BNP / Touchstone Files	201
Select Matrix Elements.....	202
Hide / Show Matrix Elements	203
Delete Matrix Elements.....	203
Unload Networks	203
Save BNP / Touchstone Files.....	204
Save a Modified Network.....	204
Save Network as Another File	204
Export the Curves to Other Format	204
View Network Properties	205
Customize the Network and Element Display Name	205
Advanced Matrix Operations	206
Copy Network.....	206
Network Re-normalization	207
Port Reduction	208
Passivity Enforcement	209
Edit the Differential Pairs	209
Redefine Mixed Mode Port	210
Show Network Parameters Via Channel Filter	212
New Organization of Mixed Mode Network Parameters	217
View Mixed-mode Network Parameters	218
Frequency Truncation	218
Frequency Re-sampling.....	219
View Total Crosstalk of Network Parameter	221

Curve Operations222

 Load / Save Isolated Curves in PowerSI222

 View and Set Curve Properties222

 Curve Pane Context Menu223

 Copy Curve.....224

 Curve Calculation.....224

 Expression Customization225

Smith Chart View of the S Parameter226

 Overview227

 Manage the Curve View.....231

 Move by Pan.....231

 Zoom In and Out.....232

 Area Select / Zoom Back.....232

 Fit.....232

 Navigator232

 Menu Functionality.....234

 Auto-tip.....234

11 Customize Workflow- - - - -237

 Lesson One: Understanding the Default Workflow.....237

 Lesson Two: Edit Workflow.....239

 Lesson Three: Save the Workflow241

 Load Existing Workflow242

Index243

Introduction

Welcome to the XtractIM Tutorial. This manual is designed to give you a brief introduction to the XtractIM tool by providing real life examples and demonstrations so you can understand some of the basic concepts. The XtractIM tool is part of a complete suite of tools for package design.

SYSTEM REQUIREMENTS

Please refer to *Installation Guide* to check the system requirements.

HOW TO USE THIS GUIDE

The XtractIM Tutorial provides demonstration examples and step-by-step instructions on how to get the desired results.

Go through the sections in each chapter in order. Perform all steps and study the examples.

ADDITIONAL DOCUMENTATION

In addition to this document, refer to the following documentation for additional information.

- *XtractIM User's Guide* describes in detail the features and functionality of XtractIM.
- *Translators User's Guide* describes translations from various types of board and package file formats to Sigrity's SPD format.

CONVENTIONS USED IN THIS GUIDE

CONVENTION	USE
Bold	GUI text, special names, terms (window names, buttons, menus, etc.)
Arial	Examples

CONVENTION	USE
>	Menu hierarchy

HOW TO CONTACT TECHNICAL SUPPORT

We are committed to helping you in using XtractIM. If you have any questions, contact the [Cadence Online Support](#).

Overview

This chapter introduces the functionality of XtractIM.

ABOUT XTRACTIM

XtractIM extracts the most common electrical models of IC packages according to IBIS (I/O Buffer Information Specification) as well as SPICE netlist of electrical models. XtractIM also supports electrical performance assessment on signal and power/ground distribution systems for packages. This feature helps you analyze the quality of the design.

These models can be used for system-level analysis including:

- Assessing the electrical performance of IC packages
- Drivers
- Interconnects
- Receivers

XtractIM can handle lead-frame, flip-chip packages and wirebond packages with 3D bonding wire profiles. The package can be single- or multi-die, and single- or stacked-BGA packages.

It can extract models of full packages or selected nets of a package.

Its interface is compatible with data files in various formats, including UPD, MCM, .BRD, .SIP, NA2, DSN, and SPD formats.

XtractIM has two modules in extraction: IBIS/RLGC and Optimized Broadband. XtractIM supports both net-based and pin-based RLC extraction for single or multi-die and single or stacked BGA packages.

MODEL EXTRACTION

Model Extraction Mode includes

- RLC / IBIS Module
- Optimized Broadband Module

RLGC / IBIS Module

The RLGC / IBIS Module for single-die, single-BGA package provides with the capability to:

- Generate IBIS package pin RLC model
- Generate IBIS package RLC (Resistance, Inductance and Capacitance) matrix model with coupling between signal, power and ground nets
- Generate net length, DC_R, delay of each signal net
- Generate SPICE equivalent circuits of package RLGC models of different topologies (Pi or T), including coupling among signal, power and ground nets
- 2D and 3D display of RLC curves and distributions, including coupling between nets

The RLGC Module for Multi-Die, Stacked-BGA package provides the capability to:

- Generate DC_R of signal, power, and ground nets along each of circuit-to-circuit paths
- Generate self R, self-L, C of signal and power nets along each of circuit-to-circuit paths
- Generate mutual L and C of signal and power nets along each of the circuit-to-circuit paths
- Generate branch RL and total C of signal and power nets
- Generate SPICE equivalent circuits of package RLGC model including coupling among signal, power and ground nets

Optimized Broadband Module

The Optimized Broadband Module works for both single-die, single-BGA and multi-die stacked-BGA packages. It provides users with the following capabilities:

- Display of the original S-parameter and compact circuit model S-parameter
- Export the S-parameter model in Sigrity compact formats (BNP)
- Extract and display of S network parameters
- Optimized Broadband RLC circuit model extraction with options of selecting circuit models

ELECTRICAL PERFORMANCE ASSESSMENT

Electrical Performance Assessment includes two systems.

- Power / Ground Distribution System
- Signal Distribution System

Power / Ground Distribution System

- Net loop inductance of Power Nets referring to each of the Ground Nets
- Broadband Impedance of each Power Net referring to its best Ground Net

- Plane IR drop, Plane current density and Via-current checking
- Per Pin resistance and inductance of power / ground net viewing from die-side

Signal Distribution System

- Trace layout checking: Impedance and strongest coupling of single-ended Net vs. section-by-section Net-length
- Net couplings: mutual inductance and capacitance, total near-ended crosstalk for each Net as a victim
- Broadband Insertion and Return Loss

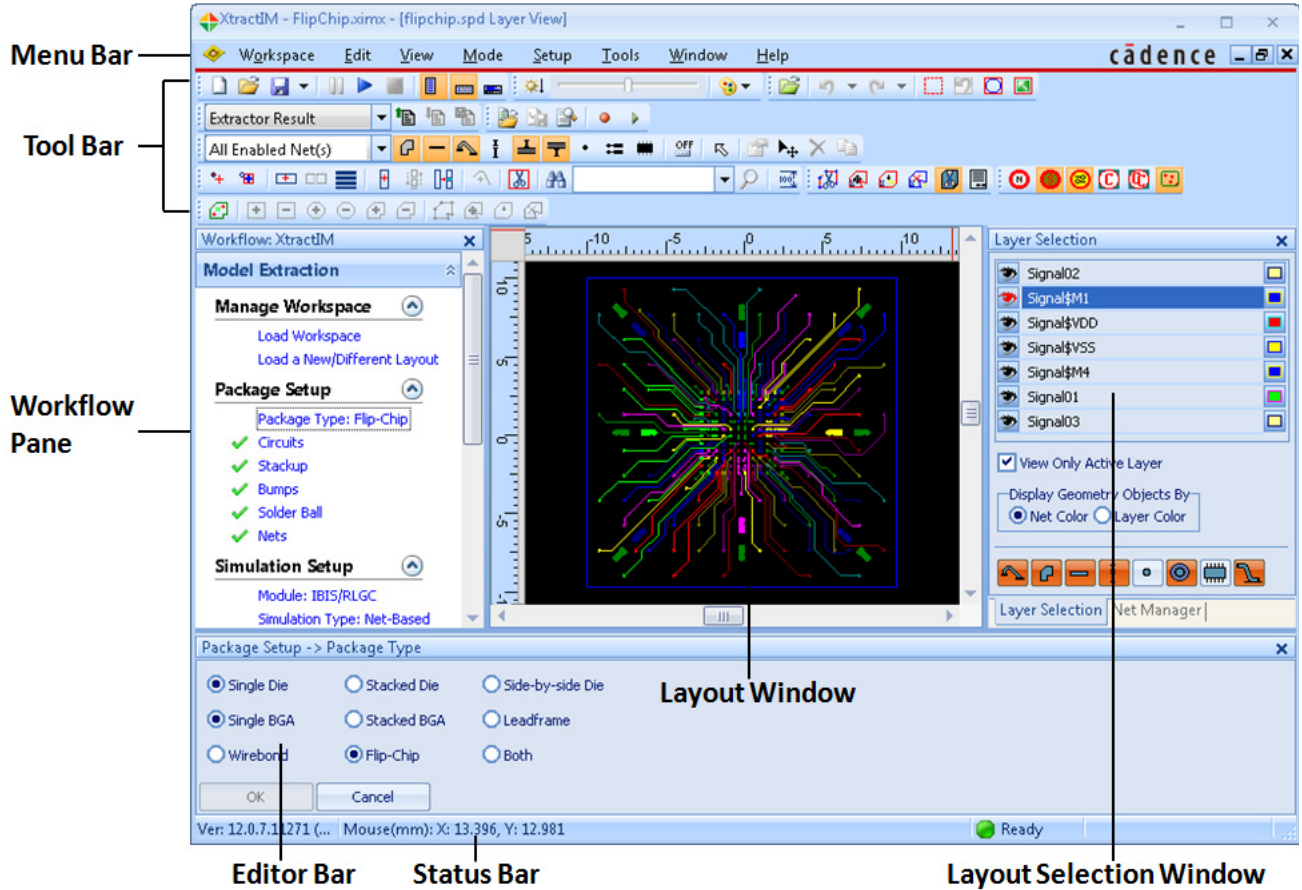
THE XTRACTIM WINDOW

The new workspace is made up of two main areas.




- **Layout Area** — Large area with a black background
- **Workflow Pane** — Left side of the screen

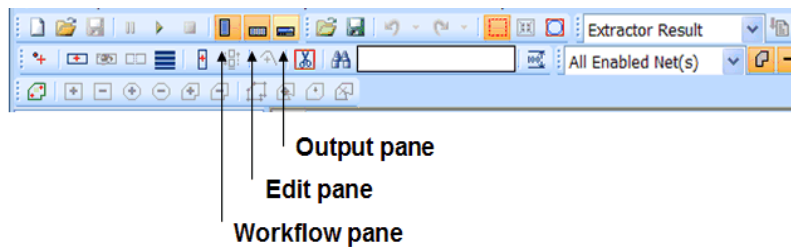
Within these two main areas you'll find toolbars, menus, and smaller, specialized panes. You'll use all the tools on the workspace to create a package simulation.

- **Editor Pane** — A spreadsheet. Users can easily input information into the pane for simulation setup or check simulation results in the pane
- **Layout Selection Window** — Controls the active layer, displayed layers and the object display on or off
- **Layout Window** — Where you edit your layout
- **Menu Bar** — The pull-down menus provide the commands you need to modify a design, set up a simulation, run a simulation, check results and report results
- **Status Bar** — Shows the version information, the current X-Y coordinates of the cursor and the simulation progress
- **Tool bar** — Gives you quick access to common XtractIM commands
- **Workflow Pane** — Lists all the workflow tasks. Tasks of the same type are sorted and listed together. When a task is clicked, details associated with that task appear in an Editor pane



Using the Toolbar Icons

1. Click on **Workflow Pane**  . The Workflow pane pops out or hides.
2. Click on **Edit Pane**  . The Status Bar pops up or hides.
3. Click on **Layout Error Check**  . The layout error messages, if any, are shown or hidden.



IBIS / RLGC Module: Net-Based Simulation Single-Die Single-BGA Packages

This chapter takes you through the steps to use the XtractIM tool IBIS / RLGC Module in the simulation of a single-die, single-BGA package.

PREPARE FOR THE SIMULATION

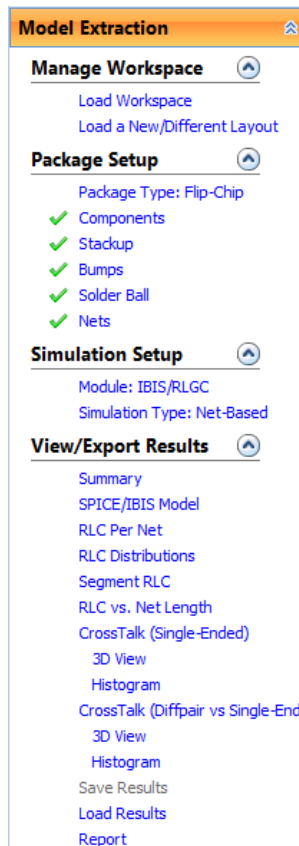
Collect this information before you begin the simulation.

- Have the Bump diameters, length, heights and conductivity ready
- Have the Stackup information ready
- Make sure your files have been translated into SPD format

LESSON ONE: SIMULATION SETUP

Overview

Follow these steps to perform a typical workflow in Interaction Mode.





1. Load an existing workspace file (.xml file).
2. Load a layout file (.spd file).
3. Select a package type. Choose from:
 - Flip-chip
 - Single BGA (Board Grid Array)
 - Stacked BGA
 - Wirebond
4. Setup the components. You can select or deselect **Die component** and **Board component**.
5. Setup the Stackup.
6. Set parameters for the Bump or Solderball medium layer.
 - Set the Bump data if it is a flip-chip package.
 - Set the Solder Ball data.
7. Select the nets for extraction.

- Setup extraction frequency and capacitance or inductance output control.

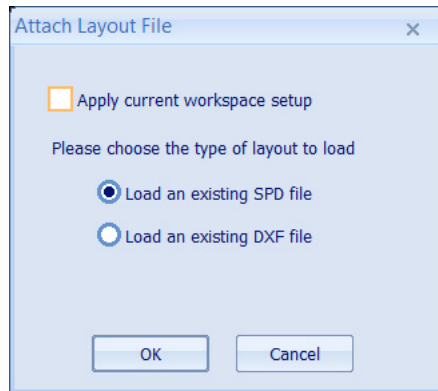
Load Workspace and Layout File

- Launch XtractIM.

The XtractIM main window opens. Two icons are available:

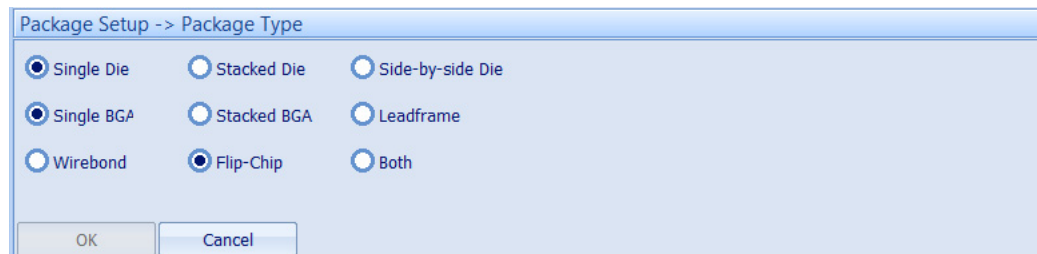
New  and **Open** 

- Click the **New** icon to create a new workspace or select:
Workspace > New
- Click **Load Workspace** in the **Workflow** pane and browse to load an existing workspace file.
- To load the **Package Structure**, click **Load a New/Different Layout** in the **Workflow** pane.
The **Attach Layout File** window opens.



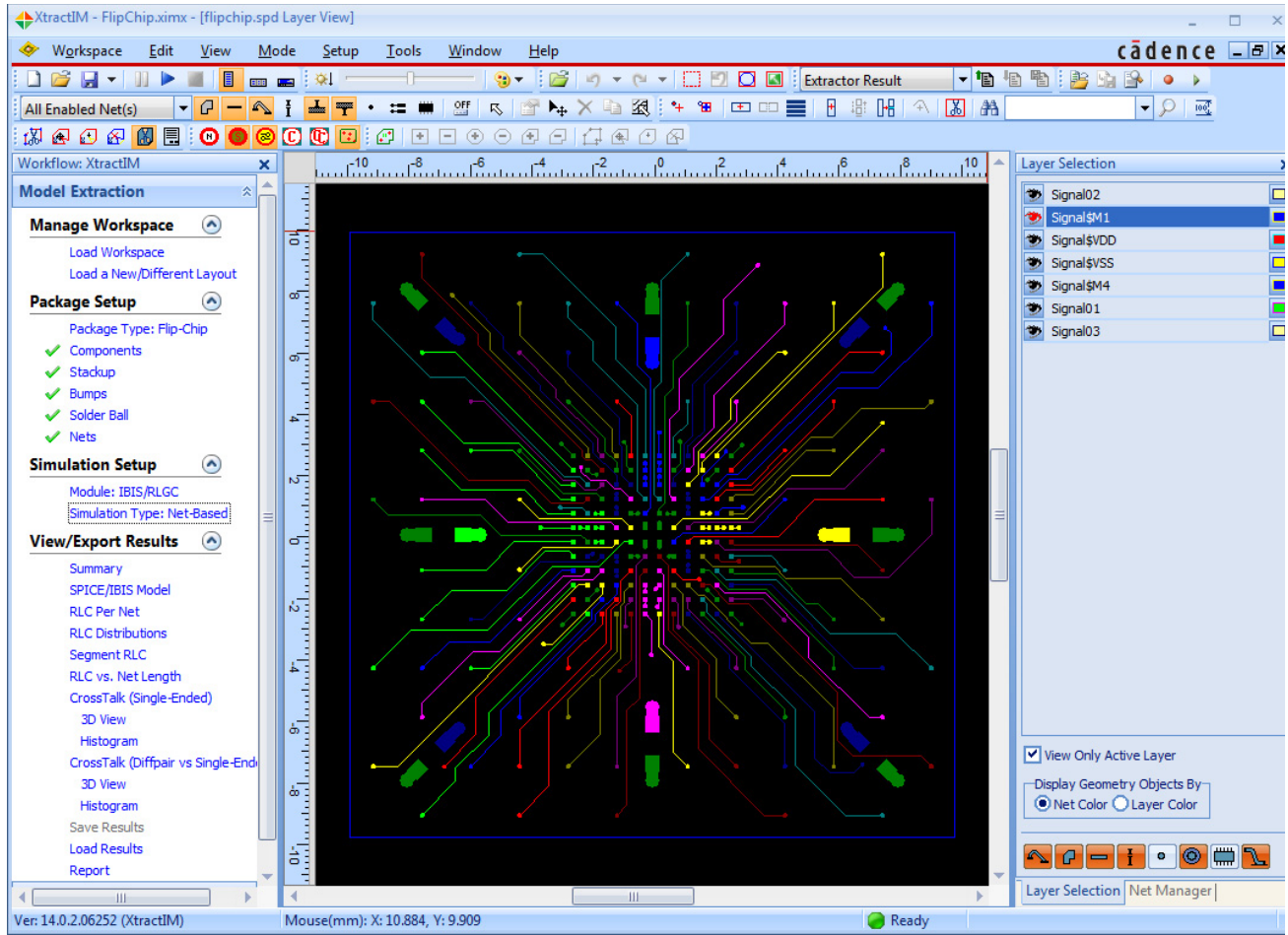
Select Package Type

- Click **Package Type: Flip-Chip** in the **Workflow** pane to select package type.
The **Package Setup -> Package Type** pane appears at the bottom of the window.



- Click **OK** to save your selection.

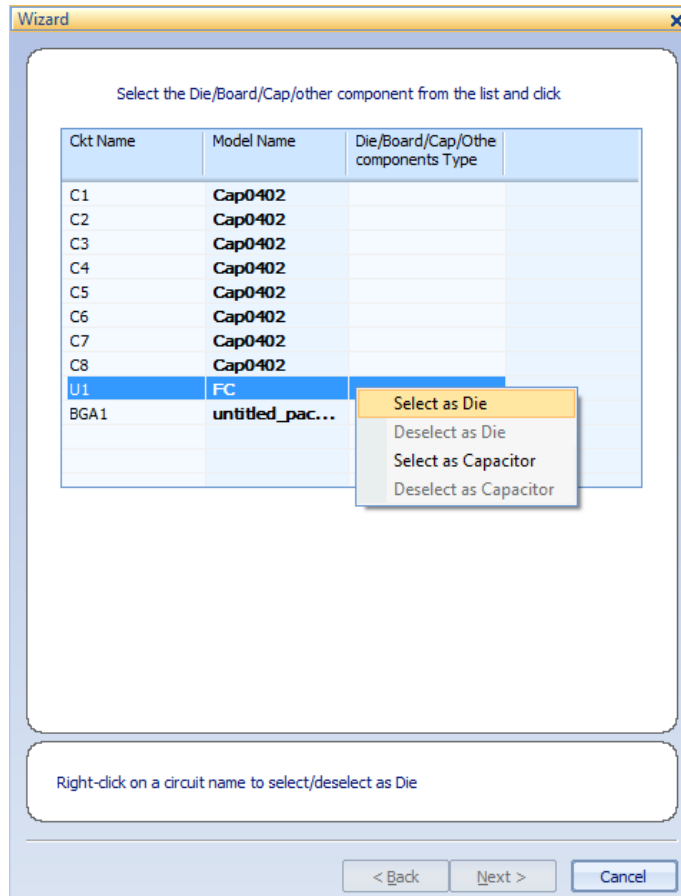
The following example shows the workspace with the package type: **Single Die, Single BGA, Flip-Chip**.



Setup Components

1. Click **Components** in the **Workflow** pane to set up the Components data for a Flip-Chip package.

The **Wizard** pane opens.



2. Right-click the desired component and select **Select as Die** from the pop-up menu list.
3. Click **Next**.
4. Right-click the desired component and select it as a **Board** component.
5. Click **Finish** to complete the components setup.

Setup Stackup

1. Click **Stackup** in the **Workflow** pane.
The **Layer Manager** -> **Stack Up** window opens.
2. Right-click **Signal\$Bottom** layer.
3. Insert a **Solder Ball Medium Layer**.
4. Insert an empty Signal layer.

5. Insert a medium layer standing for a PCB medium layer. All layers are inserted under **Signal\$Bottom**.

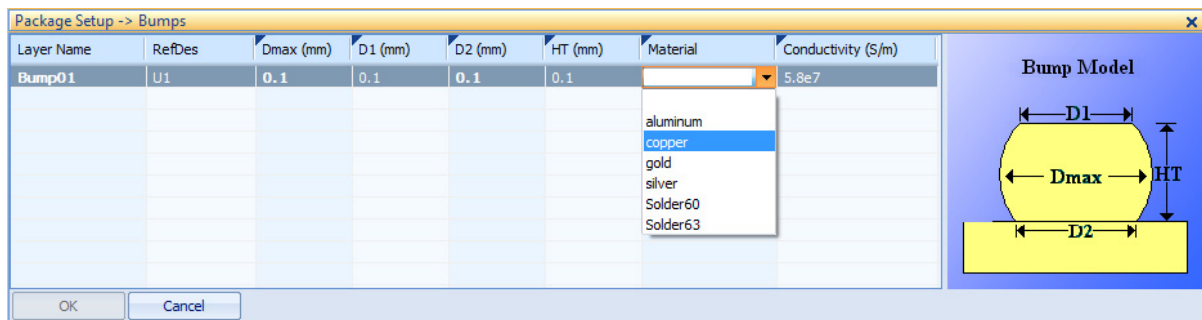
The added Signal layer is located at the end of the solder ball.

Setup Bump Medium Layer

1. Right-click on the **Signal\$Top** layer.
2. Insert a **Bump Medium Layer** above **Signal\$Top**.
3. Insert a **signal layer** above **Signal\$Top**. The added signal layer is the ending of the Bump. Both the Bump and Solder Ball Medium Layers are created.

Setup Bumps

1. Click **Bumps** in the **Workflow** pane to set up the Bump data for a Flip-Chip package. The **Package Setup -> Bumps** pane appears at the bottom of the window.



2. Input the settings for the Bumps.
Maximum Diameter: Dmax (mm)
D1 (mm)
D2 (mm)
Height: HT (mm)
Conductivity (S/m) (or click **Material** and choose material from the drop-down list, the conductivity will be automatically input.)

NOTE!

XtractIM includes a material file in library (in the default installation path: <INSTALL_DIR>\SpeedXP\Library\material\). It can be edited.

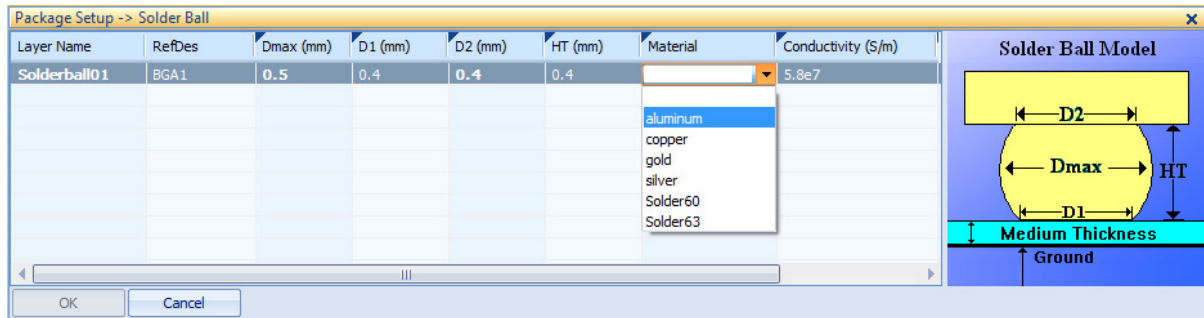
3. Click **OK** to save your entries.
4. (Optional) Click **Cancel** if you do not want to save your changes, or if you want to start over and re-enter your settings.

NOTE!

Perform the same steps to set up a wirebond package.

Setup Solder Ball

1. Click **Solder Ball** in the **Workflow** pane to setup the Solder Ball data for a Flip-Chip package.
The **Package Setup -> Solder Ball** pane appears at the bottom of the window.



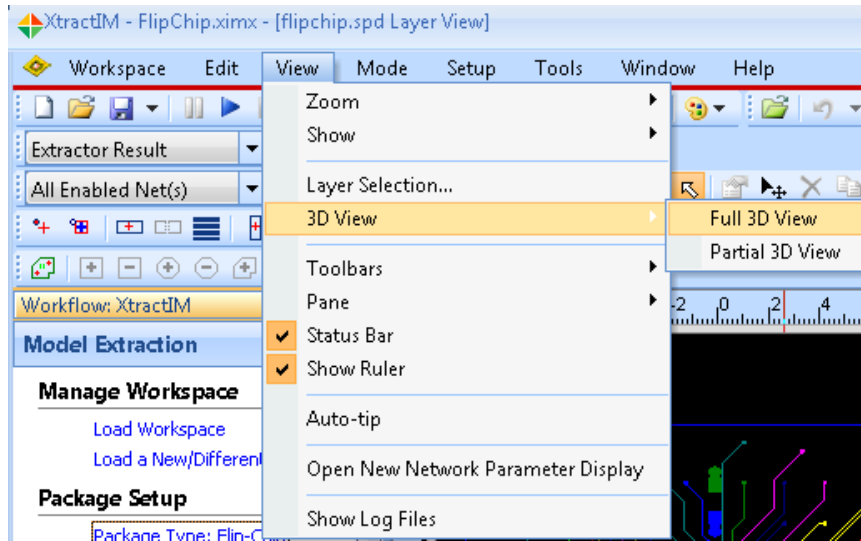
2. Input the settings for Solder Ball.
Maximum Diameter: Dmax (mm)
D1 (mm)
D2 (mm)
Height: HT (mm)
Conductivity (S/m) (or click **Material** and choose material from the drop-down list, the conductivity will be automatically input.)
3. Click **OK** to save your entries.
4. (Optional) Click **Cancel** if you do not want to save your changes, or if you want to start over and re-enter your settings.

Viewing 3D Layout

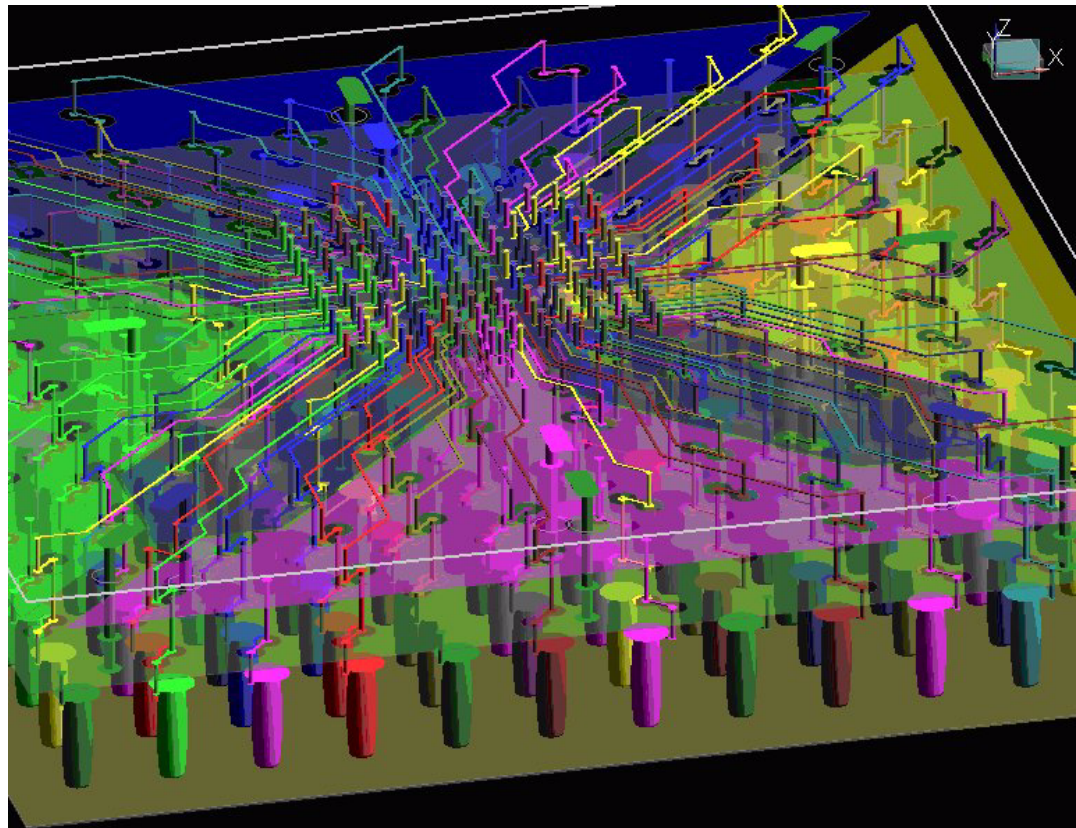
Full 3D View

Select

View > 3D View > Full 3D View

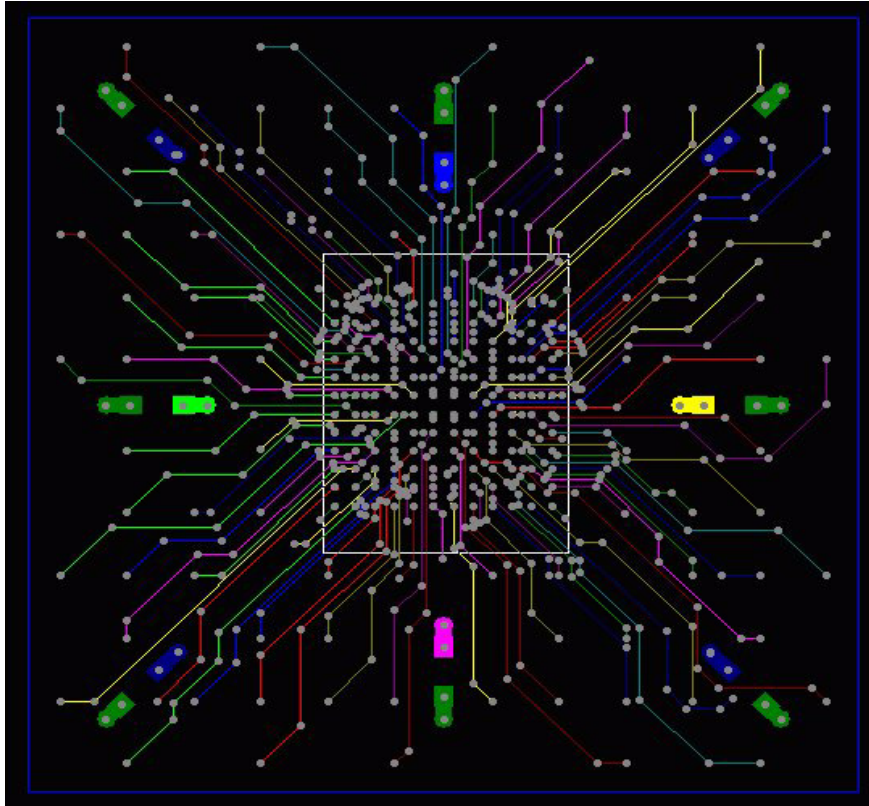


The 3D view of the package is displayed showing the bumps and solder balls.

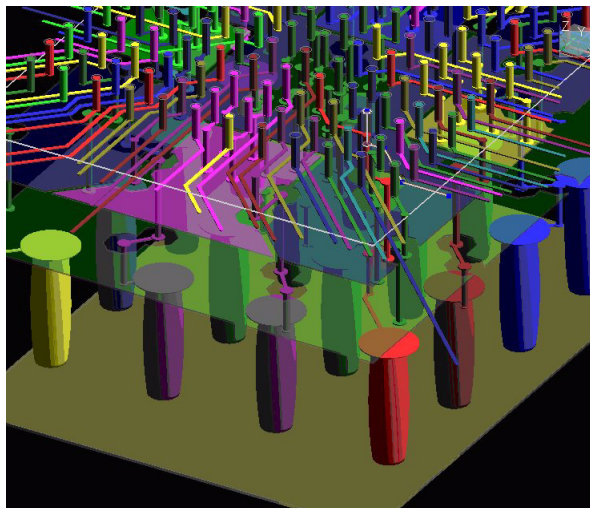


Partial 3D View

1. Select
View > 3D View > Partial 3D View
2. Use the mouse to select a region (shown as a box outline in the following image).

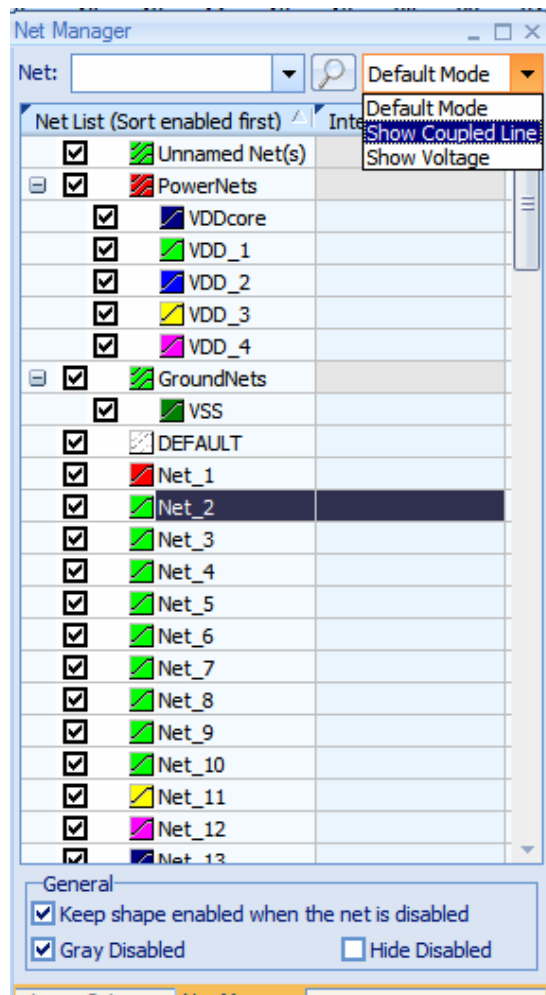


The 3D view of the selected region is shown in the display.



Setup Nets

1. Click **Nets** in the **Workflow** pane to open **Net Manager**.
2. Choose any desired nets for **RLC** (Resistance, Inductance and Capacitance) extraction.
You can move the Signal Net into and out of Power Nets and Ground Nets if you wish.
3. Choose only the desired Ground Net as the reference net.
At least one Ground Net must be selected to act as a **Reference ground Net**.
4. Set the Trace coupling threshold to a proper level to generate RLC models with accurate mutual terms.
5. Switch to **Show Coupled Line**. The **Coupled Lines Edit** pane opens.
6. Set the **Trace Coupling Threshold** to a proper level.



NOTE!

The Coupled Lines tab controls only the coupling threshold between Traces.

Via coupling and wirebond coupling are always considered.

Rise Time and %Coupling

When Traces are identified as **coupled lines**, the crosstalk between these lines is calculated during the simulation. Based on electrical threshold parameters, Traces belonging to several nets are automatically identified and analyzed as coupled transmission line sections.

- Two Traces are said to be coupled if their reverse crosstalk exceeds the **%Coupling**
- Coupled lines can be selected after the relevant Traces have been placed. Coupled lines are treated as multi-conductor transmission lines
- An **isolated Trace** is modeled by the single transmission line algorithm

For a given **Rise Time**, the accumulated coupled section lengths between Trace nets should be long enough for forward crosstalk to exceed the %Coupling.

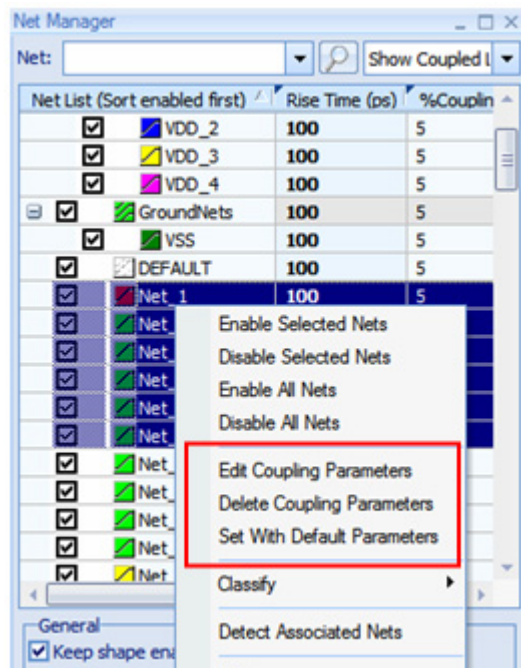
- **Rise Time Value** — Must be greater than 0. Default value is 200 ps
- **%Coupling Value** — Must be $0 < \text{value} \leq 100$. Default value is 5%

NOTE!

If the coupling parameters - %Coupling and Rise Time - are left blank, the trace-to-trace coupling is not calculated during simulation.

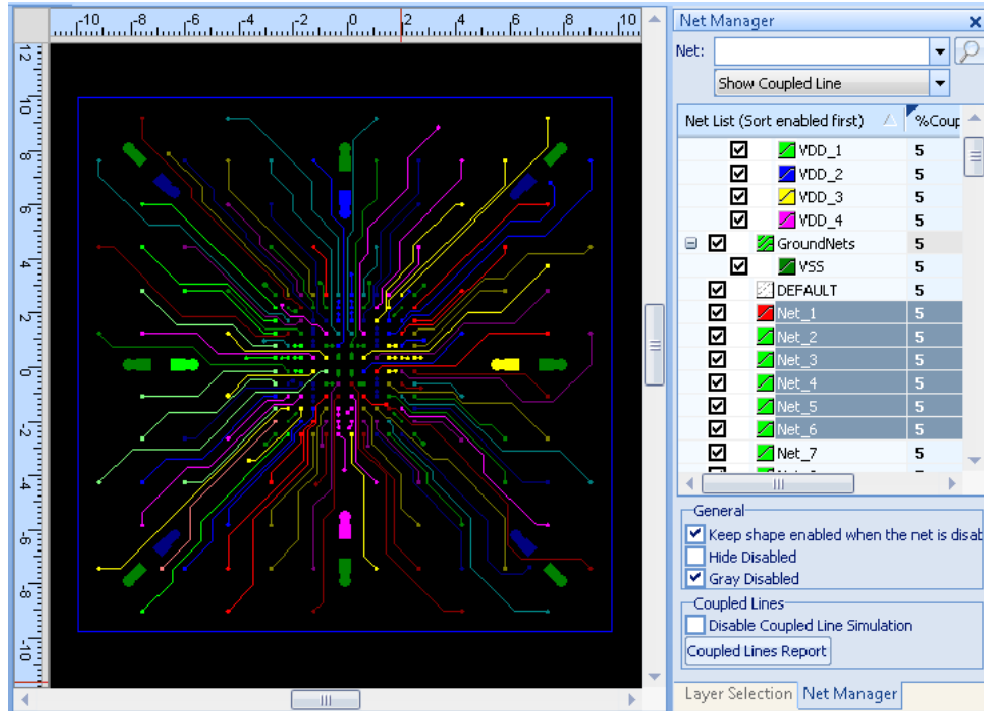
Setup Rise Time and %Coupling

1. Click on **Coupled Line** tab to set up *Setup Extraction Frequency* to identify a coupled trace.
2. Select the nets you wish to edit.
3. Right-click to open the pop-menu.
4. Select:
Set With Default Parameters



5. Select **Show Coupled Lines** in the **Net Manager**.

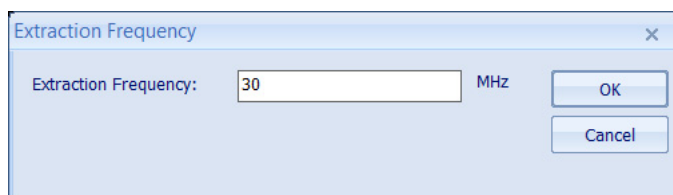
The Trace identified as coupled lines is displayed in the **Layout View** pane, as shown in the following screen.



Setup Extraction Frequency

- To change the Extraction Frequency, select Setup > Extraction Frequency

The **Extraction Frequency** window opens.



- Input the value of extraction frequency in the field.
The default value is 30MHz.
- Click **OK**.

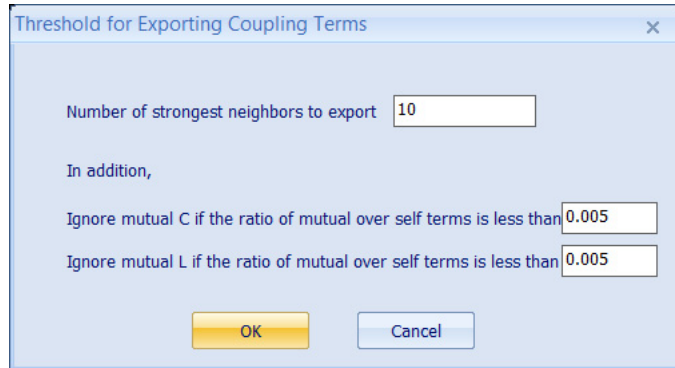
Setup Threshold for Exporting Mutual Terms

XtractIM provides an option to reduce the size of the output circuit during the export stage. Besides, XtractIM captures all the coupling during the extraction stage.

- Select

Setup > Threshold for Exporting Coupling Terms

The **Threshold for Exporting Coupling Terms** window opens.



2. Input the number of strongest coupling neighbors to be kept in the circuit model.
The default number of strongest coupling neighbors is 10; which means outputting the 10 strongest neighbors (including self).
3. Ignore mutual capacitance or inductance if the ratio of mutual terms over self term is less than a percentage.
The default percentage threshold for ignoring mutual capacitance and inductance is 0.005.

Exporting Mutual Terms Example

If the mutual capacitance or inductance is less than the 0.5% of the minimum of the two self-capacitances and inductances,

then

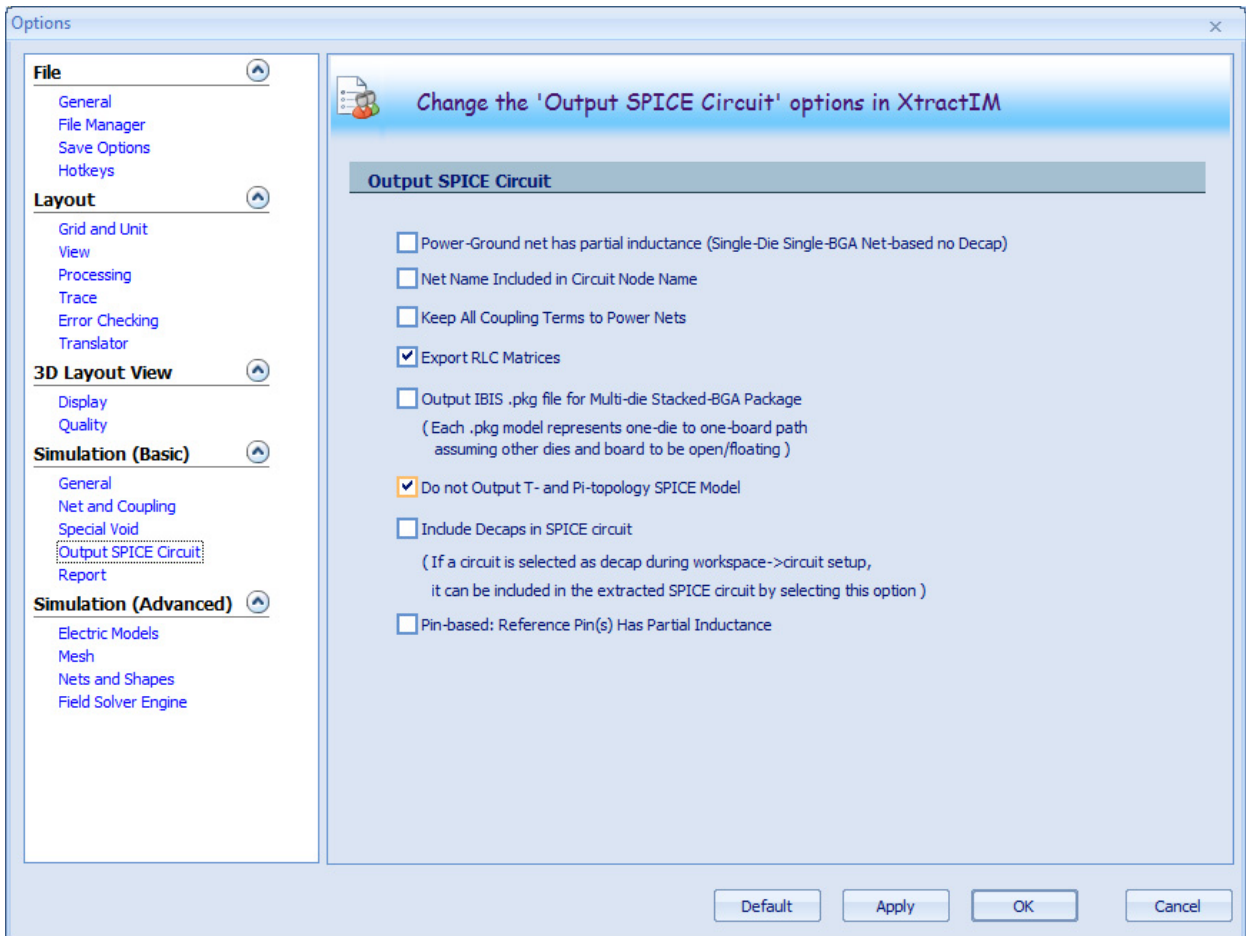
XtractIM does not output the mutual capacitance or inductance

NOTE!	<p>Threshold for Exporting Coupling Terms is used to:</p> <ul style="list-style-type: none"> - Control the size of the SPICE circuit file. - Ignore mutual capacitance or inductance less than a specified net-to-net coupling threshold.
--------------	---

Output RLC Matrix in .csv Format

1. To output RLC matrix in .csv format, select
Tools > Options > Edit Options...

The **Options** window opens.







2. Click **Output SPICE Circuit** under **Simulation (Basic)**.
3. Select the **Export LC Matrices** option.
4. (Optional) Select the **Do not Output T- and Pi-topology SPICE Model** option if you do not want these two SPICE models.
5. Click **OK**.

LESSON TWO: SAVE WORK AREAS

Tool Bar

There are four icons related with work areas saving.

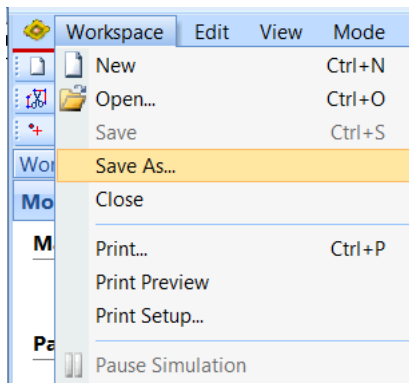


ICON	DESCRIPTION
	Open Workspace File
	Save all
	Save Workspace File Save Layout File
	Attach a layout file

NOTE! Saving the workspace automatically saves the .spd file.
Saving the layout file does not automatically save the workspace.

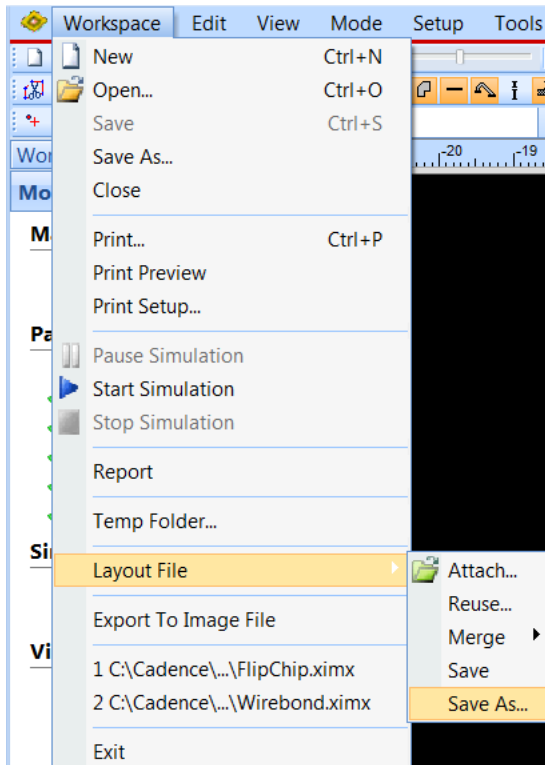
Workspace File

To save the workspace under a different name, select
Workspace > Save As...




Layout File

To save the layout file under a different name, select
Workspace > Layout File > Save As...



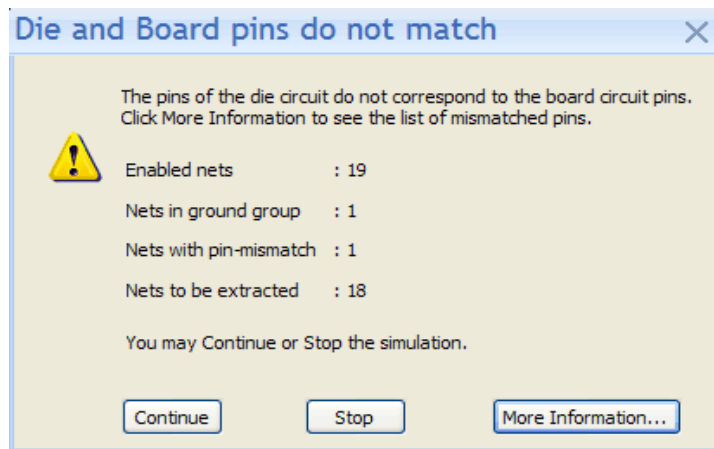
LESSON THREE: RUN THE SIMULATION

Start Simulation

1. Click the **Start Simulation** icon  on toolbar to start the extraction (simulation).

XtractIM only extracts RLCG for a net which has at least one pin at the Die side and at least one pin at the board side.

At the beginning of the simulation, if some nets have Die-Board mis-match, a pop-up window appears.

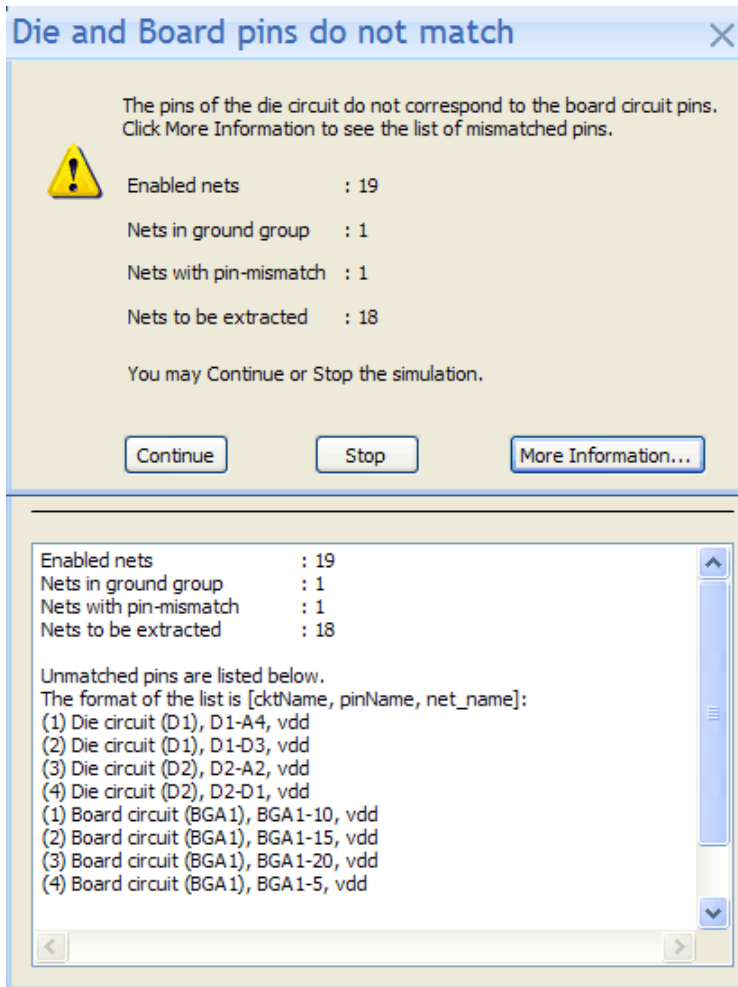


2. Select the next action.
 - **Continue** — Continue the simulation
 - **More Information** — Examine what nets are mis-matched
 - **Stop** — Cancel the simulation

Investigate Mis-matched Nets

1. The **More Information** window lists all the mis-matched nets.
2. Investigate the mis-matched nets to see whether there is a special design or a defective design.
3. Decide whether or not to proceed with the simulation.
4. Choose **Continue**, **Stop** or **More Information**.

If 30 seconds pass and the user has not made a choice; then, by default, the simulation continues.



NOTE! A file named Xtracted_PinNode_Info.log is saved on hard disk. This file records the total extracted node number of each circuit and, if available, the mis-matched information.

LESSON FOUR: OBSERVE AND SAVE SIMULATION RESULTS

XtractIM performs calculations for each net. The calculations include:

- Conductance
- Mutual capacitance with other net
- Mutual loop inductance
- Resistance
- Self capacitance
- Self loop inductance

The inductance and capacitance are matrices. In the Inductance Matrix, the Diagonal Element is the Self Inductance of each net. The off-diagonal elements are mutual Inductance.

There are two concepts of capacitance matrix:

- Maxwell capacitance matrix
- SPICE capacitance matrix
- **Maxwell Capacitance Matrix** — Each diagonal element is the loading capacitance; for example, capacitance-to-ground when other nets are grounded. This represents the worst-case capacitive loading. Off-diagonal elements are mutual capacitance with negative values
- **SPICE Capacitance Matrix** — Each diagonal element is capacitance-to-ground. Off-diagonal elements are mutual capacitance with positive values

In the examples, review the relationship between Maxwell capacitance and SPICE capacitance matrix.

Inductance and Capacitance Matrix Example

A simple group of four nets has the following inductance and capacitance matrix.

$$\begin{bmatrix} L_{11} & L_{12} & L_{13} & L_{14} \\ L_{21} & L_{22} & L_{23} & L_{24} \\ L_{31} & L_{32} & L_{33} & L_{34} \\ L_{41} & L_{42} & L_{43} & L_{44} \end{bmatrix} \quad \begin{bmatrix} C_{11} & C_{12} & C_{13} & C_{14} \\ C_{21} & C_{22} & C_{23} & C_{24} \\ C_{31} & C_{32} & C_{33} & C_{34} \\ C_{41} & C_{42} & C_{43} & C_{44} \end{bmatrix}$$

Capacitance Example

$$C_{ij}(\text{SPICE}) = -C_{ij}(\text{Maxwell})$$

$$C_{ii}(\text{Maxwell}) = \sum_j C_{ij}(\text{SPICE})$$

$$C_{ii}(\text{SPICE}) = \sum_j C_{ij}(\text{Maxwell})$$

Summary of the Extracted Results

1. Click **Summary** in the **Workflow** pane.
2. View the data for R, L and C.
 - Extraction Frequency
 - Full RLC Matrix
 - Maximum / minimum R, L, C
 - Nets Extracted
 - Package Name
3. Reorder the list, if desired.

The screenshot displays the XtractIM software interface. The main window is titled 'Extractor Result' and shows the following parameters:

- [Version] 12.1.b1.02041
- [Date] 06/05/2013
- [Package Name] C:\Cadence\SPB_16.6\ASI\Update1\SpeedXP\Samples\Xtract
- [Description] C:\Cadence\SPB_16.6\ASI\Update1\SpeedXP\Samples\Xtract
- [Nets Extracted] 105
- [Frequency of Extraction] 30MHz
- [Max R (mOhm)] 312.934
- [Min R (mOhm)] 4.54504
- [Max self-inductance L (nH)] 8.76833

Below the parameters is a table with columns: Net, Net, R(mOhm), L(nH), and C(pF). The table lists various nets and their corresponding R, L, and C values.

Net	Net	R(mOhm)	L(nH)	C(pF)
VDD_1	VDD_1	12.9943	1.02645	18.0999
VDD_2	VDD_2	0	0	0
VDD_3	VDD_3	0	0	0
VDD_4	VDD_4	0	0	0
VDD_4	VDDcore	0	0	0
VDDcore	Net_1	0	0	0
Net_1	Net_2	0	0	0
Net_2	Net_3	0	0.184293	0.406076
Net_2	Net_4	0	0.393493	0.438503
Net_3	Net_5	0	0.393493	0.438503

Below the table is an 'Output' window showing the following text:

```
* Processing patch02 -- Patch$VDD
* Processing patch02 -- Patch$VSS
* Processing Patch$VDD -- Patch$VSS
* Processing Patch$VSS -- Patch01
Connecting Circuits To Patches
Handling Floating Circuits
Modeling Pads
Solving Package and Circuits ...
Simulation is in progress.
```

At the bottom of the window, there is a 'Miscellaneous' section with 'Mesh - Errors' and 'VariablesCheck' options.

Save SPICE/IBIS Model Files

Upon completing the simulation, both model files are saved in the same directory as the **.spd** file.

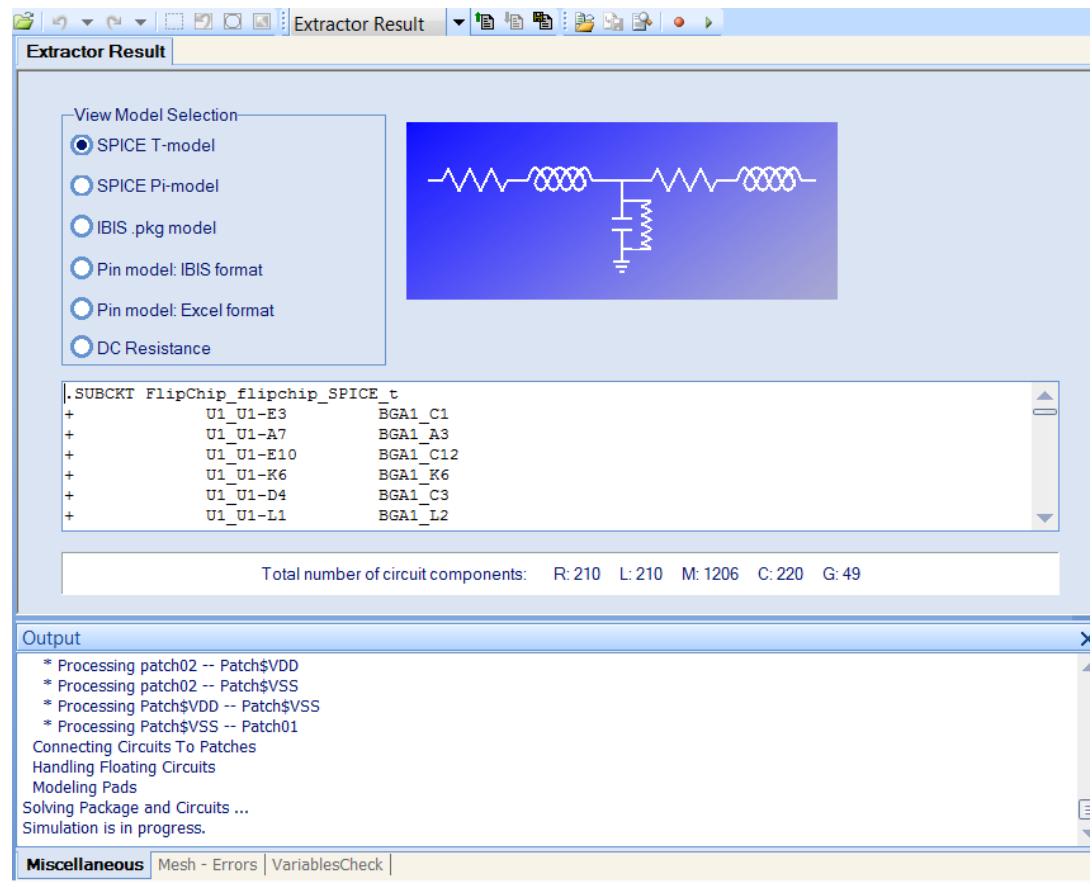
Save SPICE Model Files

The total number of elements in the circuit is displayed at the bottom of the window.

R, L, M, C and G where M is the mutual inductance

The SPICE Model is saved as a SPICE sub-circuit with the extension **.ckt**.

The SPICE model is a T-circuit.

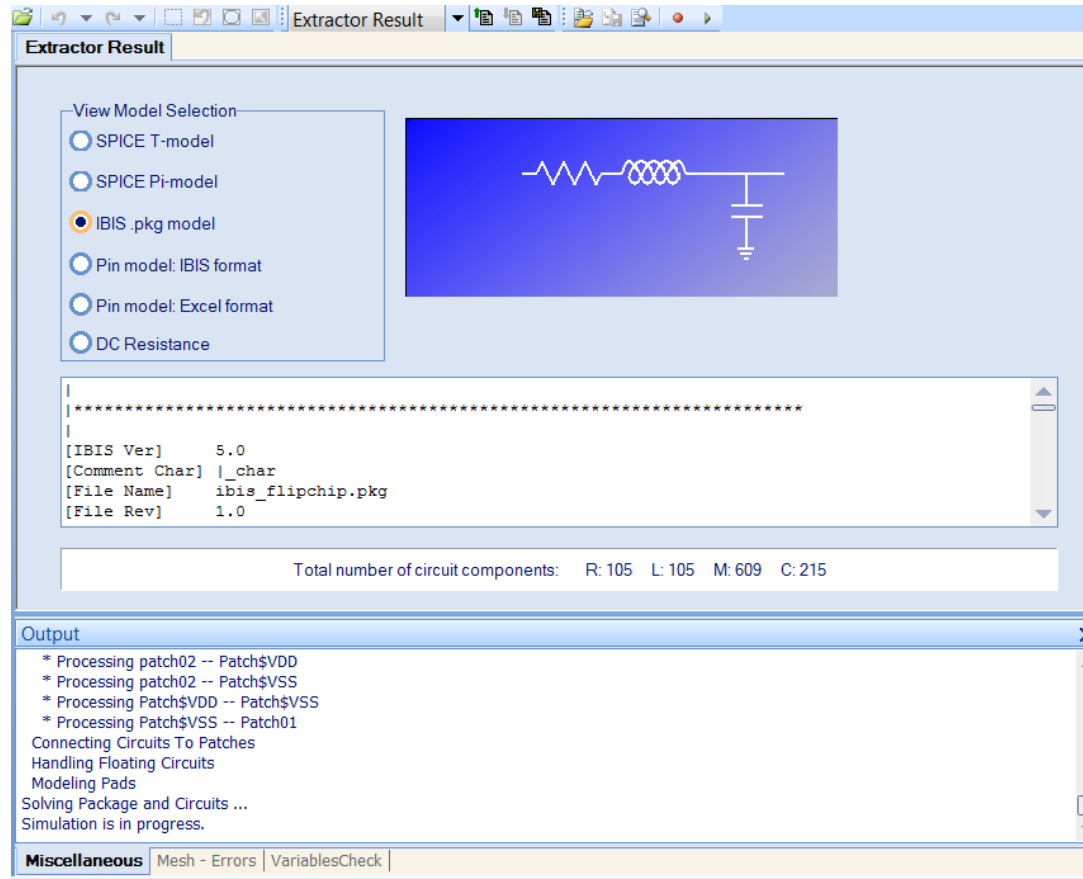


Save IBIS Model Files

The **IBIS Model** is saved as an IBIS package model. The saved model has the extension **.pkg**.

An **.ibs** format file is saved. The saved file includes each single net's R, L, C.

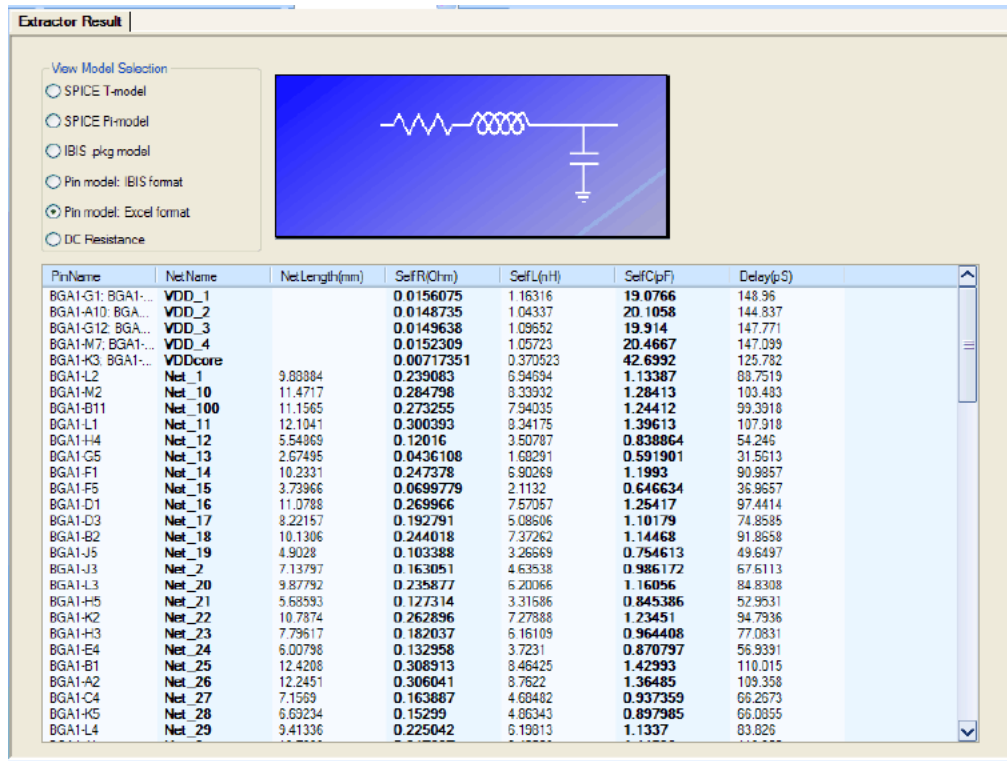
All power nets and ground nets are lumped together.



Load Pin Model in Excel Format

1. Click **Pin Model: Excel format** in the SPICE / IBIS Model window.
2. A .csv file is loaded. The .csv file includes information for each signal net.
 - Net Length
 - Net Name
 - Pin Name
 - Self-R
 - Self-L
 - Self-C
 - Time Delay

Self-C is the Maxwell Capacitance. The information for power nets does not include net length.



NOTE! Net-length is reported only for single nets. If a single net has multi-pins in either die side or BGA side, its' net -length will NOT be reported.

View DC Resistance

1. Click **DC Resistance** in the SPICE / IBIS Model window.
2. View the **.csv** file. DC Resistance is given for each of the power, ground and signal nets. A **.csv** file is saved on the hard disk.

The screenshot shows the 'Extractor Result' window with the following components:

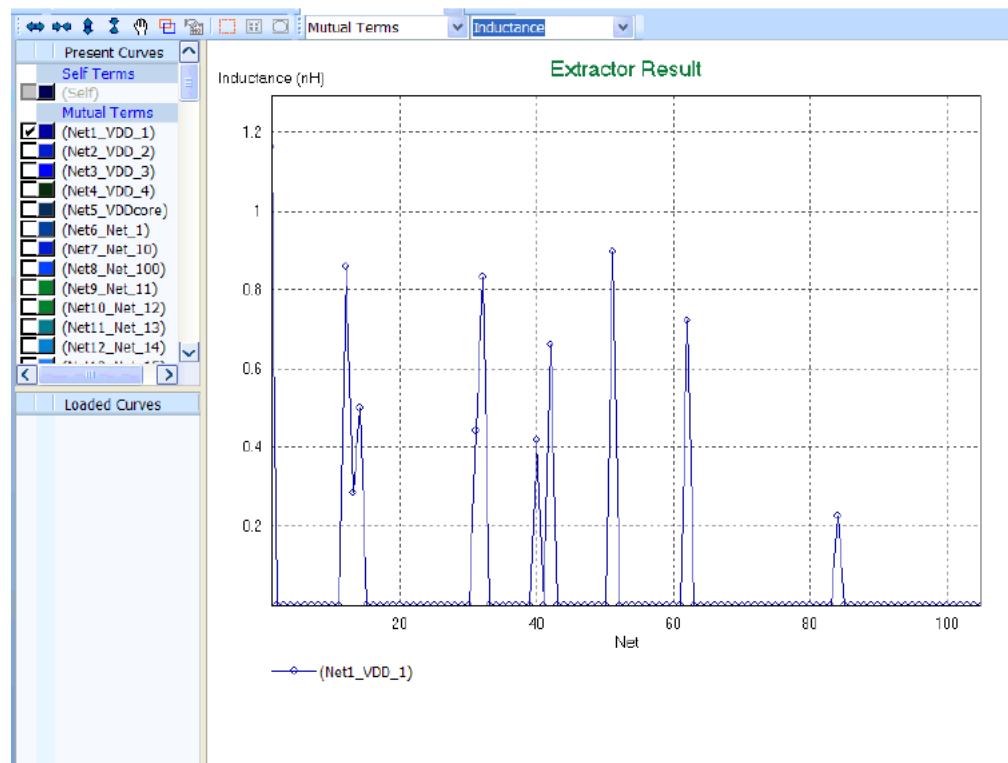
- View Model Selection:**
 - SPICE T-model
 - SPICE Pi-model
 - IBIS .pkg model
 - Pin model: IBIS format
 - Pin model: Excel format
 - DC Resistance
- Diagram:** A schematic diagram on a blue background showing a resistor and an inductor in series, connected to a ground symbol.
- Table:** A table with two columns: 'NetName' and 'DC R(Ohm)'. It lists 29 net names and their corresponding DC resistance values.

NetName	DC R(Ohm)
VDD_1	0.00766212
VDD_2	0.00728748
VDD_3	0.00734888
VDD_4	0.00731403
VDDcore	0.00389387
Net_1	0.196745
Net_10	0.233246
Net_100	0.22528
Net_11	0.247784
Net_12	0.0970853
Net_13	0.0322723
Net_14	0.204774
Net_15	0.0549716
Net_16	0.224214
Net_17	0.158531
Net_18	0.200191
Net_19	0.0822371
Net_2	0.13362
Net_20	0.196608
Net_21	0.103159
Net_22	0.217516
Net_23	0.148752
Net_24	0.107665
Net_25	0.255066
Net_26	0.251026
Net_27	0.134056
Net_28	0.123376
Net_29	0.185928

View RLC Per Net

1. View **Resistance** for each net.
2. View **Self-inductance** for each net.
3. View **Self-capacitance** for each net.
4. View **Mutual Terms**.
5. View **Mutual Inductance**.
6. View **SPICE Mutual Capacitance**.

Usually conductance is very low, so there is no view for conductance.



Save R / L / C Full Matrix

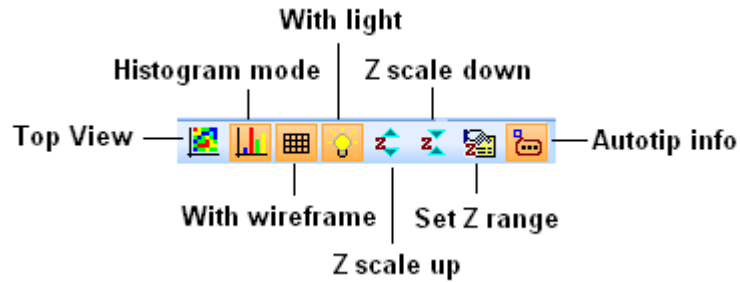
1. Click on **R/L/C** full matrix.
2. The matrix is saved on hard disk in .csv format.

	A	B	C	D	E	F	G	H
1	Net i	Net j	R _{ij} (mOhm)	L _{ij} (nH)	C _{ij} (pF)			
2	VDD_1	VDD_1	16.6984	1.14717	17.8014			
3	VDD_1	Net_5		0.882293	0.398692			
4	VDD_1	Net_14		0.845834	0.51895			
5	VDD_1	Net_32		0.830443	0.397358			
6	VDD_1	Net_6		0.706866	0.410717			
7	VDD_1	Net_41		0.660616	0.204631			
8	VDD_1	Net_16		0.501037	0.509205			
9	VDD_1	Net_31		0.447115	0.060698			
10	VDD_1	Net_4		0.41579	0.32842			
11	VDD_1	Net_23		0.28861	0.126366			
12	VDD_1	Net_15		0.280537	0.0241			
13	VDD_2	VDD_2	15.9463	1.02801	18.649			
14	VDD_2	Net_35		0.754558	0.606863			
15	VDD_2	Net_50		0.728148	0.398461			
16	VDD_2	Net_55		0.721226	0.494188			
17	VDD_2	Net_54		0.702859	0.4037			
18	VDD_2	Net_45		0.698387	0.457406			
19	VDD_2	Net_62		0.692691	0.533048			
20	VDD_2	Net_49		0.566389	0.1798			
21	VDD_2	Net_65		0.563293	0.178132			
22	VDD_2	Net_43		0.459691	0.290527			
23	VDD_2	Net_63		0.402483	0.374004			
24	VDD_2	Net_72		0.274983	0.329165			
25	VDD_3	VDD_3	15.9821	1.07951	18.4838			

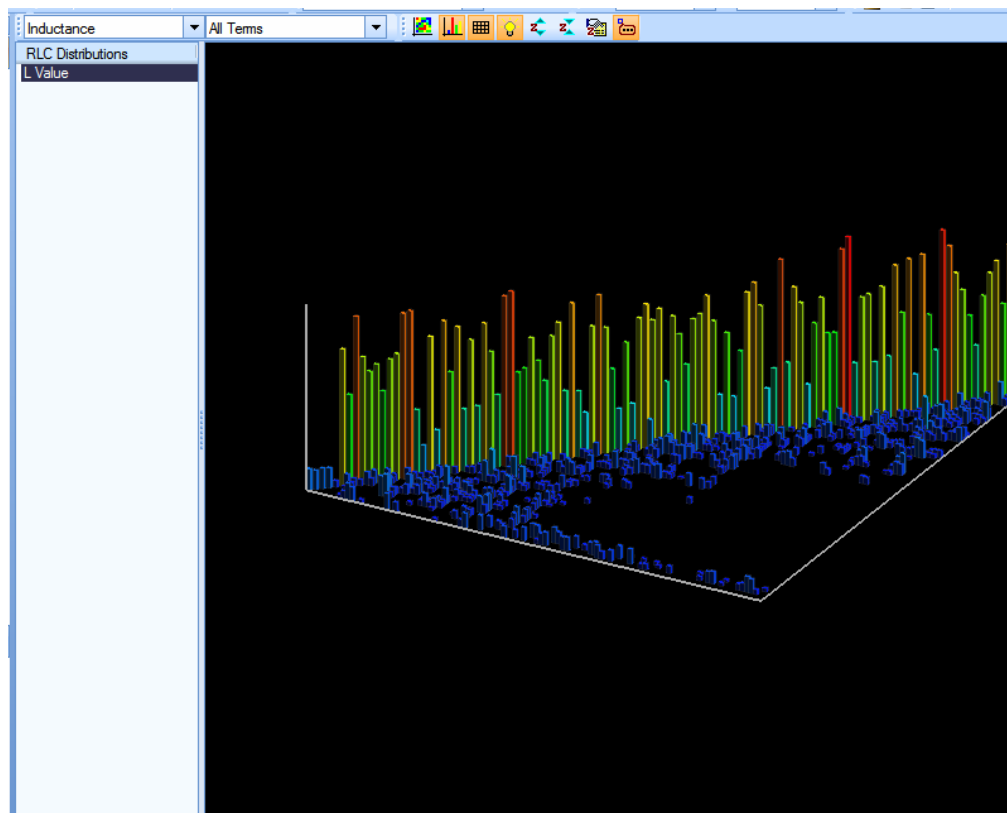
View RLC Distributions

1. Click **RLC Distributions** in the Workflow pane.
2. View the full matrix value of R, L and C.

RLC Distributions offers eight kinds of views.



3. View the **RLC distributions**.



View Segment RLC

1. Click **Segment RLC** in the **Workflow** pane.

For each Signal Net, XtractIM outputs the RLC segment of each Metal layer.

PinName	SignalNetName	Signal\$M1(O...	Signal\$VDD(...	Signal\$VSS(...	Signal\$M4(O...
L2	Net_1	0.180109	0.0111254	0.00946193	0.0119557
J3	Net_2	0.11236	0.010766	0.00949058	0.0119557
J1	Net_3	0.255368	0.010766	0.00949058	0.0119557
H2	Net_4	0.148074	0.010766	0.00949058	0.0119557
G2	Net_5	0.133487	0.0107647	0.00948935	0.0119541
E2	Net_6	0.144806	0.010766	0.00949058	0.0119557
E3	Net_7	0.100455	0.0106971	0.0094918	0.0119574
D2	Net_8	0.151882	0.0107647	0.00948935	0.0119541
C2	Net_9	0.163308	0.0107647	0.00946071	0.0119541
M2	Net_10	0.220419	0.0107647	0.00948935	0.0119541
L1	Net_11	0.236482	0.0107673	0.0094918	0.0119574
H4	Net_12	0.073506	0.010766	0.00949058	0.0119557
G5	Net_13	0.00569206	0.00895375	0.00759813	0.0124565
F1	Net_14	0.18993	0.010766	0.00949058	0.0119557
F5	Net_15	0.0247396	0.0134646	0.00851012	0.0119541
D1	Net_16	0.2101	0.010766	0.00949058	0.0119557
D3	Net_17	0.140426	0.010766	0.00949058	0.0119557
B2	Net_18	0.176829	0.0178275	0.00946193	0.0119557
J5	Net_19	0.0565564	0.0107647	0.00948935	0.0119541
L3	Net_20	0.180453	0.0107673	0.00946315	0.0119574
H5	Net_21	0.0728056	0.00613949	0.0050913	0.0269901
K2	Net_22	0.204092	0.0107647	0.00946071	0.0119541
H3	Net_23	0.128777	0.0107673	0.00946315	0.0119574
E4	Net_24	0.0855075	0.0106953	0.00949058	0.0119557
B1	Net_25	0.244964	0.0107673	0.0094918	0.0119574
A2	Net_26	0.240459	0.0107647	0.00948935	0.0119541
C4	Net_27	0.113034	0.0107647	0.00948935	0.0119541
K5	Net_28	0.1011	0.0107647	0.00948935	0.0119541

Resistance(Ohm) | Inductance(nH) | Capacitance(pF)

2. View the Segment RLC values.

Note the three tabs across the bottom of the screen. These bars are for Resistance, Inductance and Capacitance

- Click on the **Resistance** tab. The Resistance values are displayed.
- Click on the **Inductance** tab. The Inductance values are displayed.
- Click on the **Capacitance** tab. The Capacitance values are displayed.

Segment RLC Report

Segment RLC are reported for Signal Nets with single-pin at each of the Die- and Board circuit.

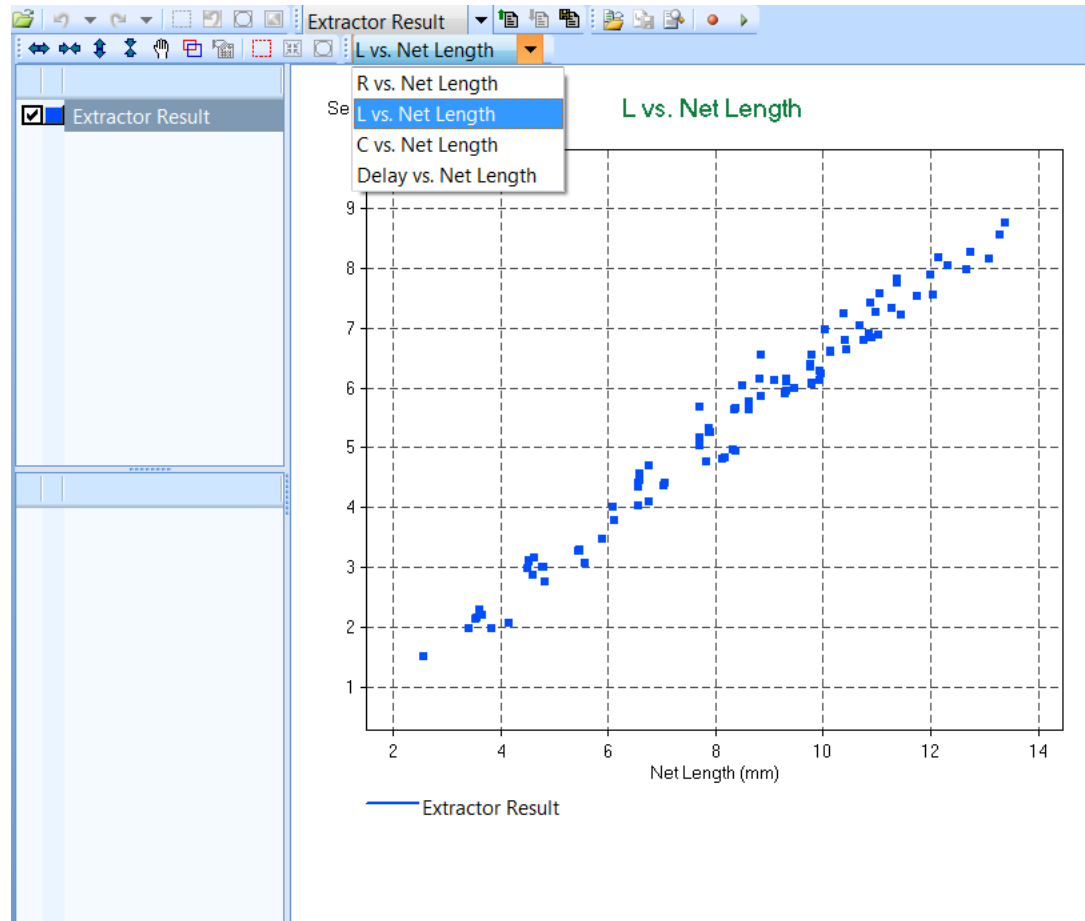
Via resistance and inductance are reported at the Via starting layer (the upper layer).

Components	Segment R	Segment L	Segment C
Wirebond	Yes	Yes	Yes
Trace	Yes	Yes	Yes
Via	Yes	Yes	Yes
Pad	-	-	Yes
Leadframe	Yes	Yes	Yes

View RLC vs. Net Length

1. Click **RLC vs. Net Length** in the **Workflow** pane.

The **Inductance plot** is displayed in the result window.

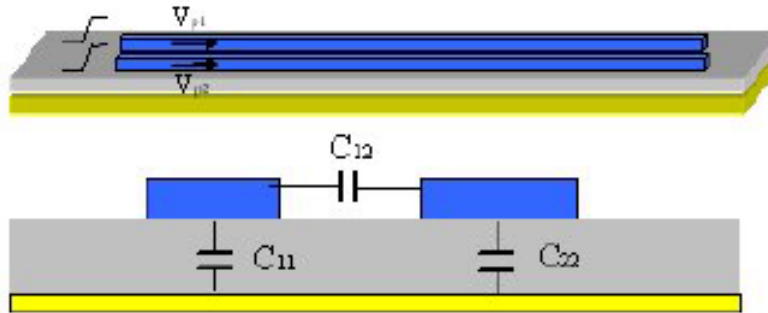


- To view the **Inductance plot**, select L vs. Net Length from the drop-down list
- To view the **Capacitance plot**, select C vs. Net Length from the drop-down list
- To view the **Delay plot**, select, select Delay vs. Net Length from the drop-down list

View Signal Nets Crosstalk

NEXT and FEXT

The mathematical definitions for NEXT and FEXT are shown in the following examples.



Aggressor: Z_{10}, L_{11}, C_{11}

Victim: Z_{20}, L_{22}, C_{22}

$$K = \frac{V_p}{4} \left(C_{12} Z_{20} + \frac{L_{12}}{Z_{10}} \right)$$

Where, $\frac{2}{V_p} = \frac{1}{V_{p1}} + \frac{1}{V_{p2}}$

$$V_{p1} = \frac{1}{\sqrt{L_{11} C_{11}}} \quad V_{p2} = \frac{1}{\sqrt{L_{22} C_{22}}}$$

$$Z_{10} = \sqrt{\frac{L_{11}}{C_{11}}} \quad Z_{20} = \sqrt{\frac{L_{22}}{C_{22}}}$$

Definitions

K	The near-end coupling coefficient from aggressor net on victim net.
C_{11} / C_{22}	The self capacitance per unit length of signal net to its reference plane.
L_{11} / L_{22}	The self-inductance per unit length of signal net.
C_{12}	The mutual capacitance per unit length between aggressor and victim net.
L_{12}	The mutual inductance per unit length between aggressor and victim net.
V_{p1} / V_{p2}	The signal velocity propagate on signal net.
Z_{10} / Z_{20}	The characteristic impedance of signal Traces.

$$FEXT = \frac{\sqrt{L_{ii} C_{ii}}}{2T_r} \left(\frac{C_{ij}}{C_{ii}} - \frac{L_{ij}}{L_{ii}} \right)$$

RLC of differential Pair and crosstalk with others

Assume two nets are different pair which has L_1 / L_2 and L_{12} as self-inductance and mutual induc-

tance, and C11/C22 and C12 as loading capacitance and mutual capacitance

L_1, C_{11}, R_1	$Diff_R = R_1 + R_2$
	$Diff_L = L_1 + L_2 - 2L_{12}$
	$Diff_C = (C_{10} \cdot C_{20}) / (C_{10} + C_{20}) + C_{12}$
L_2, C_{22}, R_2	<i>where, $C_{10} = C_{11} - C_{12}, C_{20} = C_{22} - C_{21}$</i>

Mutual Inductance and Capacitance

- Differential Pair vs. Single-ended

diff {	m	$L_{diff-k} : L_{mn-k} = L_{mk} - L_{nk} $
	n	
Single →	k	$C_{diff-k} : C_{mn-k} = C_{mk} + C_{nk}$

- Differential Pair vs. Differential Pair

diff {	m	$L_{diff-diff} : L_{mn-kl} = (L_{mk} - L_{nk}) - (L_{ml} - L_{nl}) $
	n	
diff {	k	$C_{diff-diff} : C_{mn-kl} = (C_{mk} + C_{nk}) + (C_{ml} + C_{nl})$
	l	

Crosstalk: NEXT and FEXT

- Differential Pair vs Single-ended

diff {	m	$NEXT : K_{mn-k}^{near} = K_{m-k}^{near} - K_{n-k}^{near} $
	n	
Single →	k	$FEXT : K_{mn-k}^{far} = (K_{m-k}^{far} - K_{n-k}^{far})$

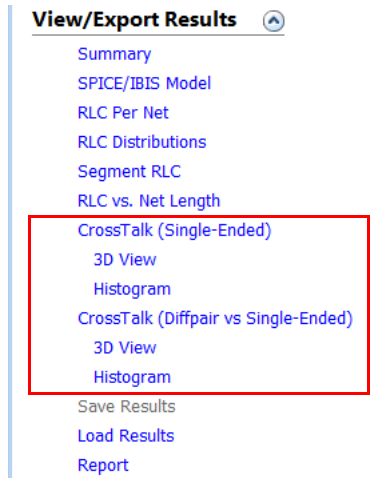
- Differential Pair vs. Differential Pair

diff {	m	$NEXT : K_{mn-kl}^{near} = (K_{m-k}^{near} - K_{n-k}^{near}) - (K_{m-l}^{near} - K_{n-l}^{near}) $
	n	
diff {	k	$FEXT : K_{mn-k}^{far} = (K_{m-k}^{far} - K_{n-k}^{far}) - (K_{m-l}^{far} - K_{n-l}^{far})$
	l	

View Crosstalk Results

Two kinds of Crosstalk results are provided:

- Single-Ended
- Diffpair vs Single-Ended



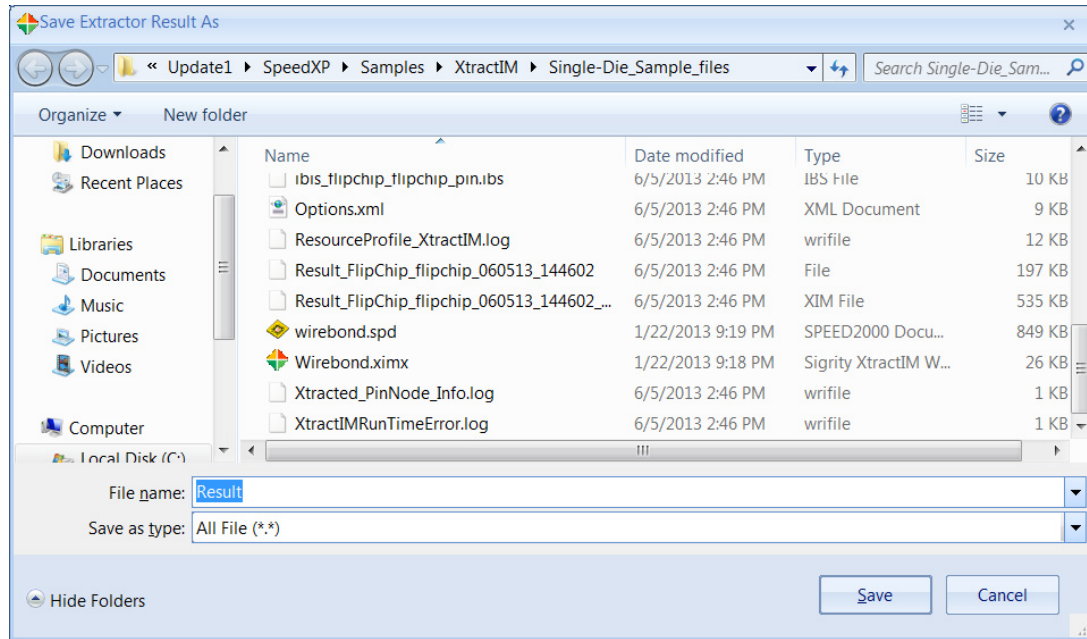
- To view single-ended near-end and far-end crosstalk (NEXT and FEXT) click **CrossTalk (Single-Ended)** in the **Workflow** pane
- To view diffpair near-end and far-end crosstalk (NEXT and FEXT) click **CrossTalk (Diffpair vs Single-Ended)** in the **Workflow** pane

A file is created in the project folder. The file name is:

*signal_Xtalk.csv

By default, the far-end crosstalk is defined with rise time = 100ps.

Net i	Net j	Rij (mOhm)	Lij (nH)	Cij (pF)	NEXT (%)	Total NEXT (...)	FEXT (%)	Tr (pS)
Net_1	Net_1	220.586	6.5703	1.011		26.91		
Net_1	Net_11	0	1.0701	0.072	5.33		-3.94	100
Net_1	Net_10	0	0.9105	0.000	3.14		-5.57	100
Net_1	Net_2	0	0.6407	0.010	3.43		-4.14	100
Net_1	Net_20	0	0.6277	0.000	2.48		-4.05	100
Net_1	Net_22	0	0.5013	0.000	1.85		-3.13	100
Net_1	Net_29	0	0.4415	0.000	1.80		-2.87	100
Net_1	Net_40	0	0.4049	0.000	1.58		-2.48	100
Net_1	Net_30	0	0.3650	0.000	1.73		-2.60	100
Net_1	Net_3	0	0.3007	0.000	1.05		-1.93	100
Net_1	Net_12	0	0.2742	0.000	1.56		-2.03	100
Net_1	Net_19	0	0.2512	0.000	1.45		-1.82	100
Net_1	Net_21	0	0.2459	0.000	1.52		-2.01	100
Net_2	Net_2	143.402	4.3835	0.864		29.23		
Net_2	Net_11	0	0.9447	0.119	6.30		-1.31	100
Net_2	Net_1	0	0.6407	0.010	3.03		-3.57	100
Net_2	Net_40	0	0.5993	0.002	2.74		-3.59	100
Net_2	Net_22	0	0.4411	0.000	1.84		-2.76	100
Net_2	Net_12	0	0.4346	0.007	3.14		-3.00	100
Net_2	Net_3	0	0.3957	0.000	1.55		-2.54	100
Net_2	Net_20	0	0.3120	0.000	1.40		-2.01	100
Net_2	Net_30	0	0.3112	0.000	1.70		-2.22	100
Net_2	Net_10	0	0.3019	0.000	1.17		-1.85	100
Net_2	Net_29	0	0.2934	0.000	1.37		-1.91	100
Net_2	Net_23	0	0.2850	0.000	1.32		-1.72	100
Net_2	Net_21	0	0.2638	0.000	1.92		-2.15	100
Net_2	Net_19	0	0.2553	0.000	1.76		-1.85	100
Net_3	Net_3	296.611	8.0109	1.325		12.47		
Net_3	Net_40	0	0.8060	0.000	2.77		-4.94	100
Net_3	Net_2	0	0.3957	0.000	1.69		-2.78	100
Net_3	Net_22	0	0.3864	0.000	1.26		-2.41	100



2. Input a file name.
3. Click **Save**.

The results are saved in a binary file. The file is named:

`result_spd_file_name.xim`

4. (Optional) Click **Cancel** if you do not want to save the results in the file name you input in earlier steps.

Simulation Output Files

The **result** and **result*.xim** files save all the output data including Summary, SPICE circuit and the two package model files. The SPICE file and two IBIS files are automatically saved by the tool.

The result file is created automatically when the simulation is finished. The output files can be viewed on the on hard disk.

- **One Crosstalk file in Excel Format** — Signal_Xtalk.csv for signal net crosstalk
- **One IBIS Package Model File** — *.pkg file. Both L and C include coupling elements
- **One Pin Model in Excel Format** — *.csv file includes each signal net length, self-R, self-L, self-C, and time delay. No coupling elements are included
- **One Pin Model in IBIS Format** — *.ibs file including each signal net self-R, self-L, and self-C. No coupling element is included
- **One Summary Content in Excel Format** — *.csv file includes RLC Full Matrix
- **Three Segment RLC in Excel Format** — Segment RLC of each metal layer with *.csv files
- **Two SPICE Circuit Files** — Pi-model is named *.ckt and the T-model is named *_t.ckt

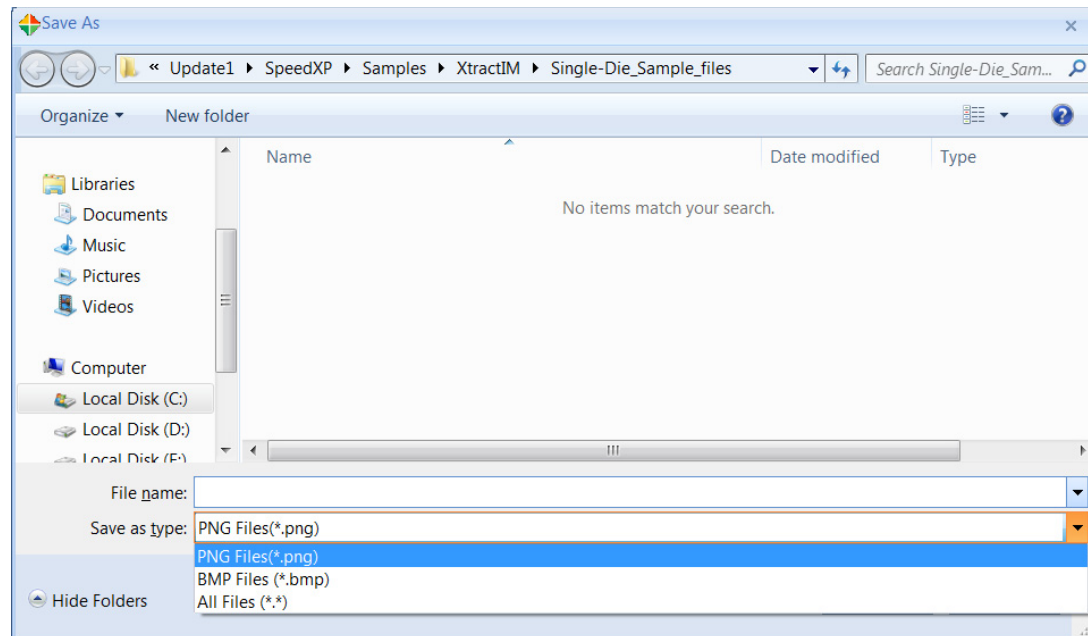
NOTE!

In model (*.ckt, *.pkg, and *PinModel.csv) extraction, XtractIM uses all ground nets as reference for both power and signal nets.

The *.ibs model is for signal nets only. In *.ibs model extraction, by IBIS definition, XtractIM uses all ground and power nets as ideal reference to get R, L, and C for each signal net.

Output Result Displays with Images (PNG or BMP Format)

1. Select
Workspace > Export to Image File
The **Save As** window opens.

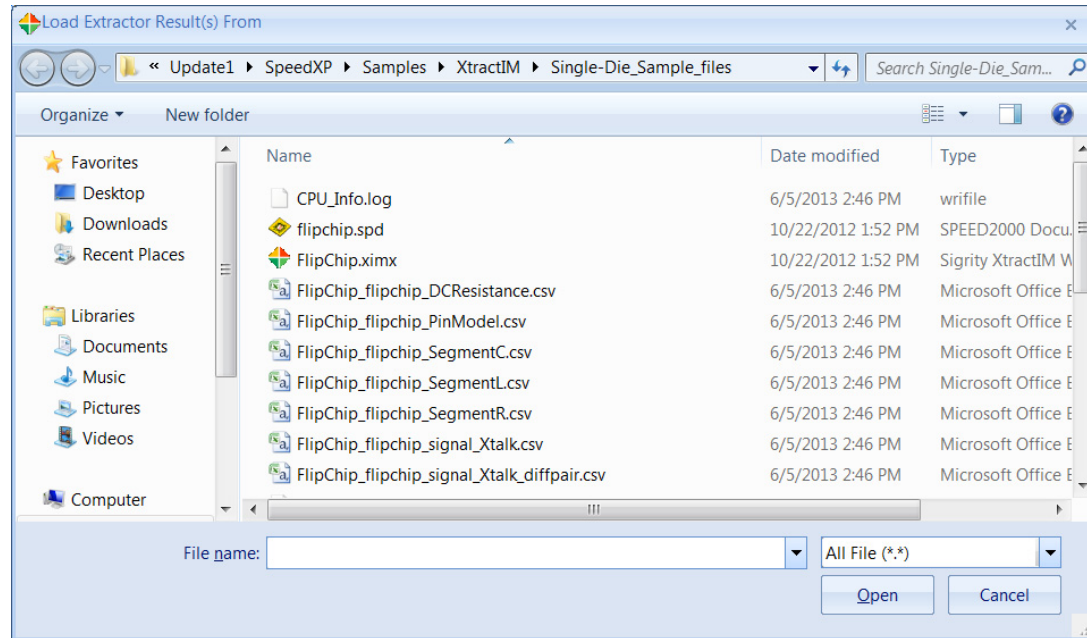


2. In the new window select the file type (.png or .bmp).
3. Click **Save**. The image file is saved.

Load in Saved Results

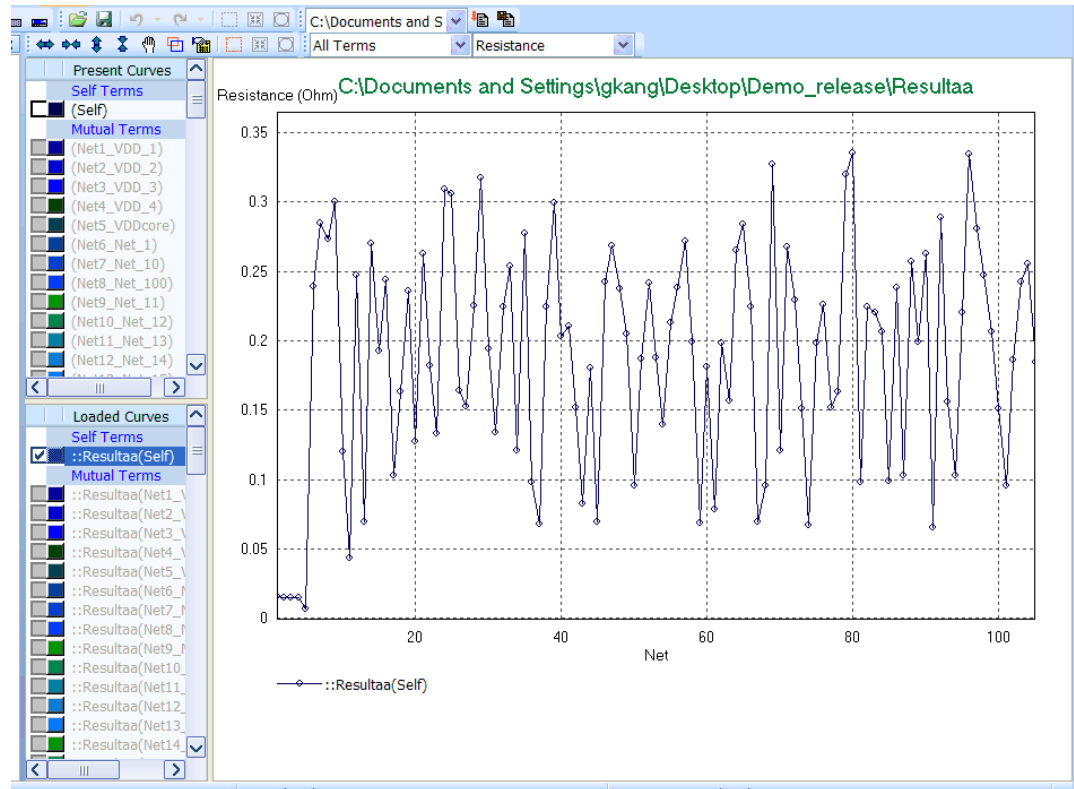
1. To load the saved results, click **Load Results** in the **Workflow** pane.

The **Load Extractor Result(s) From** window opens.



2. Browse to select the desired result file.
3. Click **Open**.
The result file is loaded.
4. View present results or the loaded results.
 - **Loaded Curves** — Shows the loaded results
 - **Present Curves** — Present extracted results
5. To unload a loaded result:
Unload Extractor Result

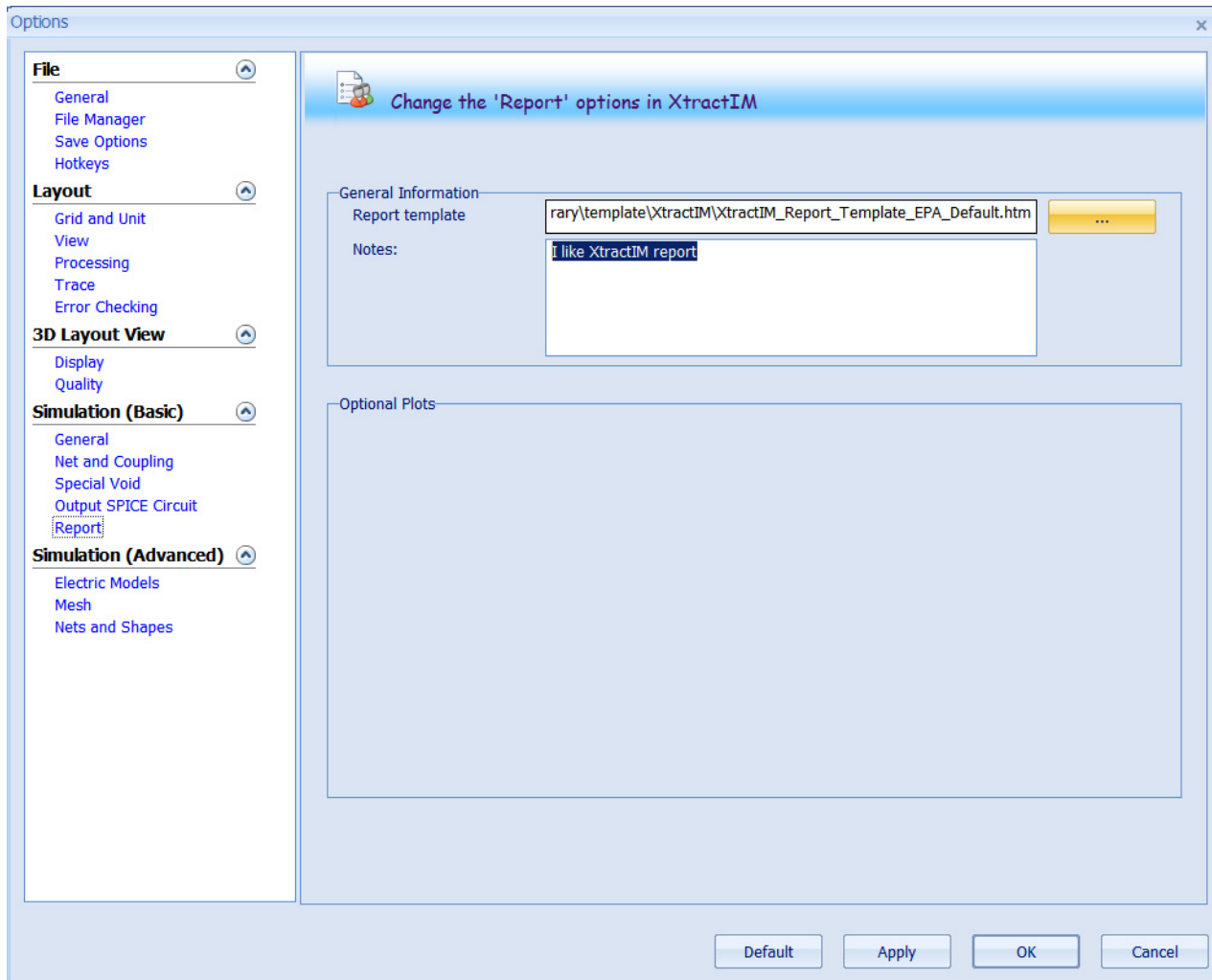
Resistance Results



Simulation Report with .htm / .html Format

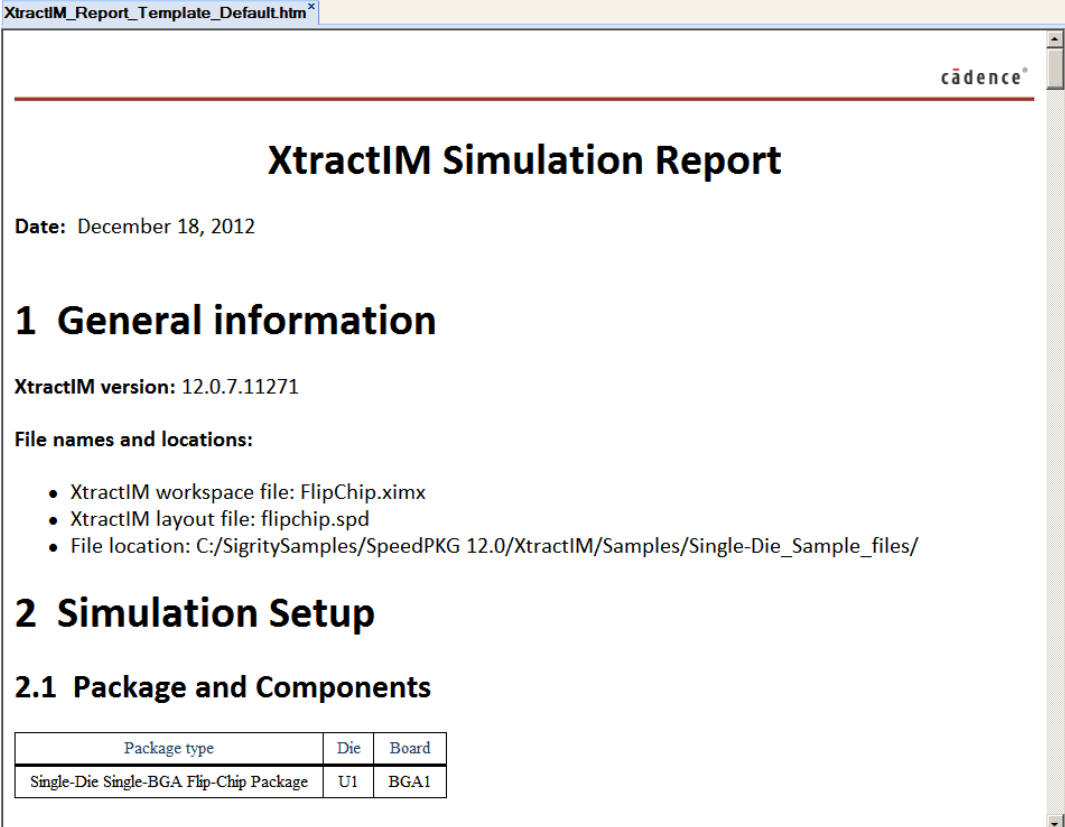
1. Click **Report** in the **Workflow** pane.

The **Options** window appears.



2. Browse to select the Report Template from
<INSTALL_DIR>\SpeedXP\Library\template\XtractIM\
3. Input notes, if desired.
4. Click **OK**.

The report file is created.



XtractIM_Report_Template_Default.htm

cadence®

XtractIM Simulation Report

Date: December 18, 2012

1 General information

XtractIM version: 12.0.7.11271

File names and locations:

- XtractIM workspace file: FlipChip.ximx
- XtractIM layout file: flipchip.spd
- File location: C:/SigritySamples/SpeedPKG 12.0/XtractIM/Samples/Single-Die_Sample_files/

2 Simulation Setup

2.1 Package and Components

Package type	Die	Board
Single-Die Single-BGA Flip-Chip Package	U1	BGA1

LESSON FIVE: BATCH MODE SIMULATION

- To run a simulation in Batch Mode, select:
Start > Run
- Change to the directory where the XtractIM.exe file is located.
- Upon completing the simulation, all output files are automatically saved in the same directory as the *.spd file.
 - *.ckt files
 - *.ibs files
 - *.pkg files
 - .csv files

Batch Mode Example

If you want to use the project (.spd file) defaulted in the workspace file (.xml file), enter
XtractIM -b "Full_path_toMy_xml_File *xml filename*"

If you want to use a different project file other than the one in the .xml file, enter

XtractIM -b "Full_path_toMy_xml_File\xml filename" "Full_path_toMy_xml_File *new_spd-file-name*"

LESSON SIX: PARTIAL INDUCTANCE REPORT FOR POWER/GROUND NETS

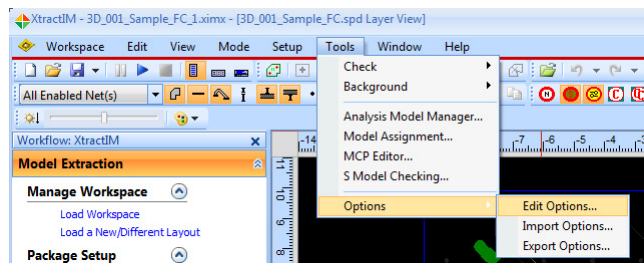
Introduction

Net-based partial inductance of power and ground nets is an optional output result for single-die single-BGA packages. It is used to evaluate the relative power and ground network design quality, while loop inductance of power and ground net pair provides meaningful electrical performance.

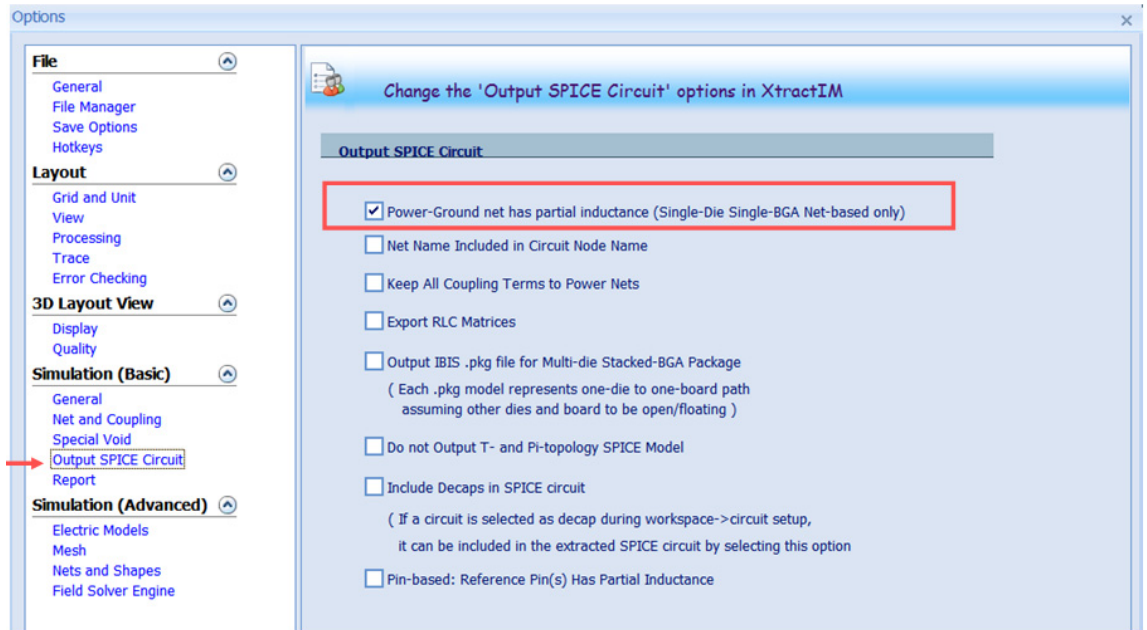
In the **SPICE/IBIS Model** section of **View/Export Results**, three partial inductance reports are available.

- Partial RLC for Power and ground nets reported with .csv format
- T-topology SPICE model with Power-ground nets having partial inductance
- Pi-topology SPICE model with Power-ground nets having partial inductance

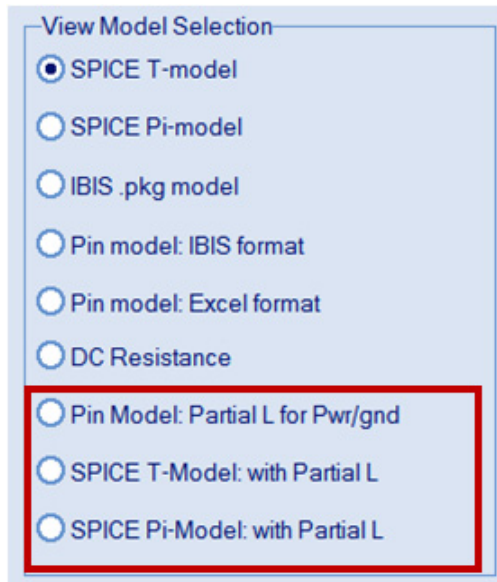
- Choose Tools > Options > Edit Options....



- Click **Output SPICE Circuit** in the **Options** window.
- Check **Power-Ground net has partial inductance (single-Die Single-BGA Net-based only)**.



In the **Model Selection** section, partial inductance reports for power and ground nets are also available.



LESSON SEVEN: 3D-EM OPTIONAL FIELD SOLVER IN XTRACTIM

Introduction

Cadence 3D-EM is an optional field solver for XtractIM. It's targeted to solve simpler packages such as lead frame package and two-layer BGA package with higher accuracy. The workflow is totally consistent with the existing hybrid solver bases.

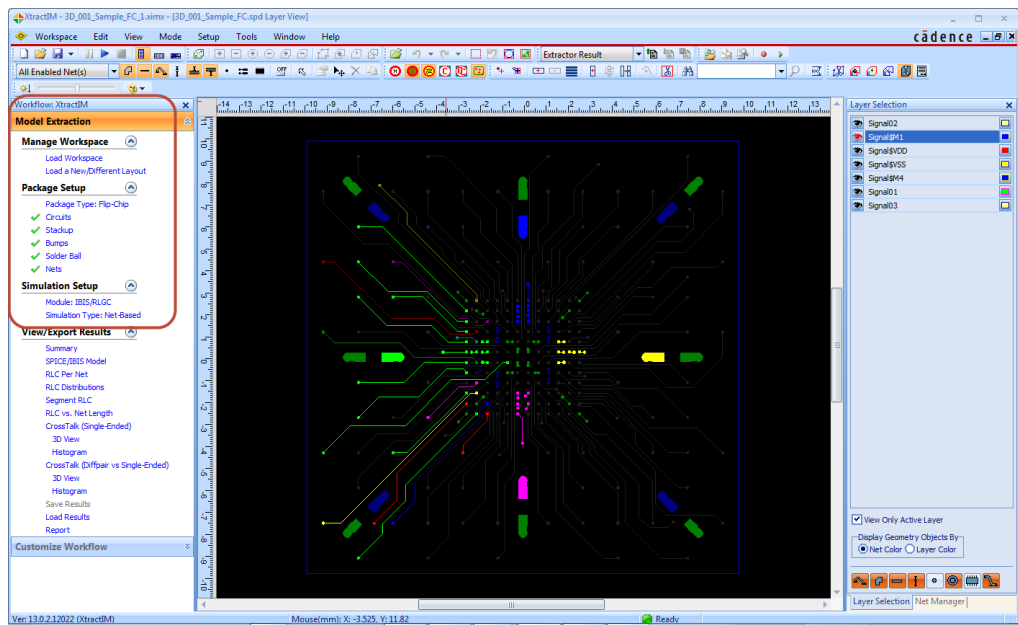
The integration of 3D-EM and XtractIM is only applied for single-die single-BGA and single-die lead-

frame for Net-based RLGC/IBIS model at single-frequency.

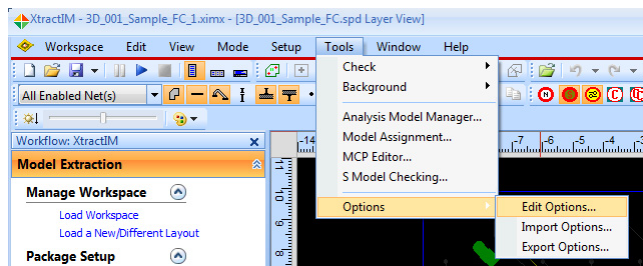
For better performance, it is recommended that you select no more than 20 nets with at most four layers.

Enabling 3D-EM Field Solver

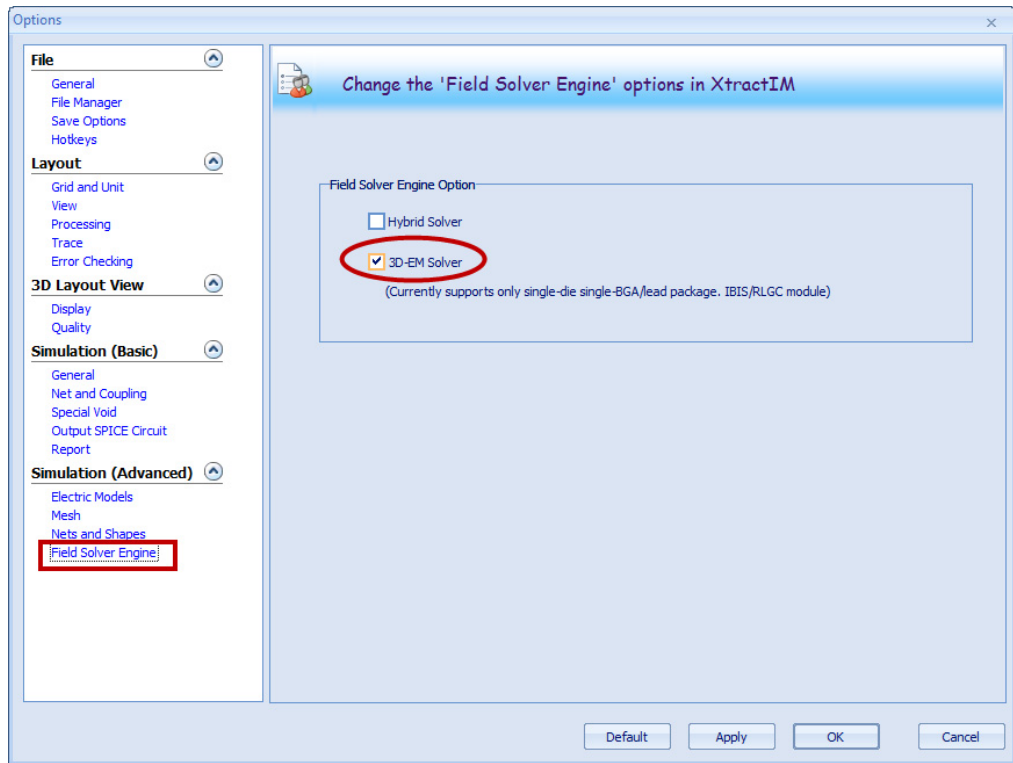
1. Make sure all the workflow setup is completed with green check-mark.



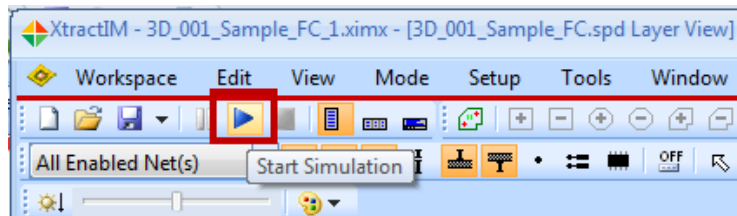
2. Choose Tools > Options > Edit Options....



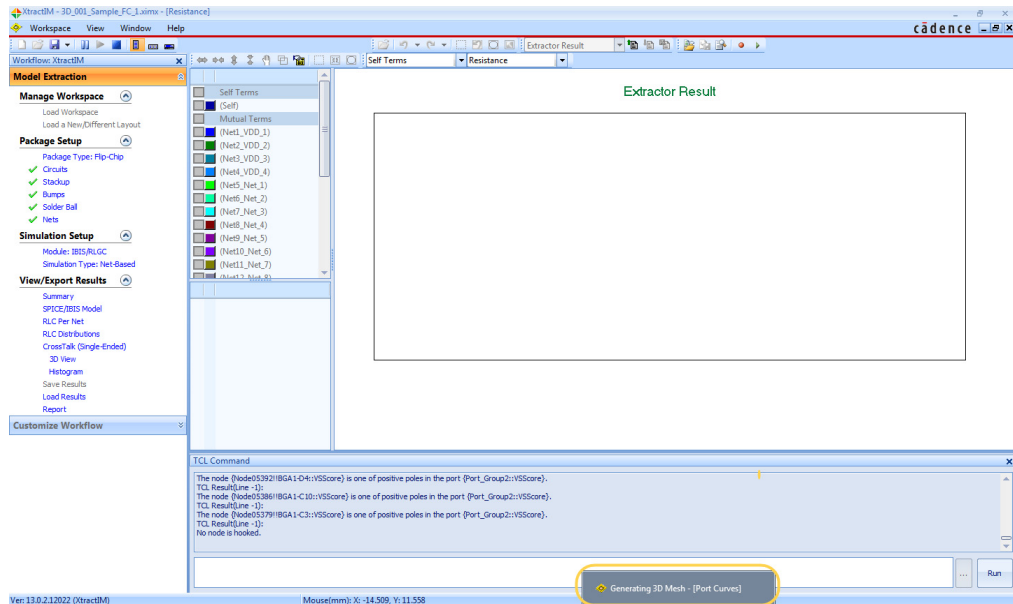
3. Click **Field Solver Engine** under **Simulation (Advanced)** in the **Options** window.
4. Check **3D-EM Solver** in **Field Solver Engine Option**.



- 5. Click **OK**.
- 6. Click the **Start Simulation** button to run simulation.



3D-EM is automatically launched as solver, and RLC result is obtained.



A temp3DFEM.spd file is generated for 3D-EM simulation. This SPD file has all settings required for 3D-EM, including:

- Port defined
- Frequency settings
- Solver options
- Geometry settings

You can use this SPD file for advanced 3D-EM simulation.

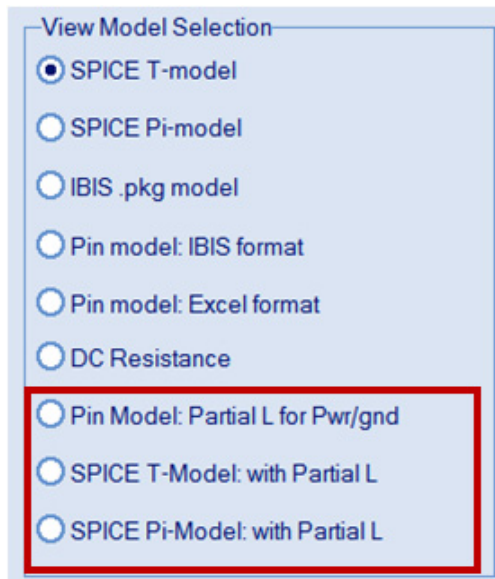
Results Display

- With 3D-EM field solver enabled, the following result is available.

View/Export Results

- Summary
- SPICE/IBIS Model
- RLC Per Net
- RLC Distributions
- Segment RLC
- RLC vs. Net Length
- CrossTalk (Single-Ended)
 - 3D View
 - Histogram
- CrossTalk (Diffpair vs Single-Ended)
 - 3D View
 - Histogram
- Save Results
- Load Results
- Report

- In the SPICE/IBIS Model, partial inductance reports for power and ground nets are also available.



RLGC Module: Net-based Simulation of Multi-die Stacked-BGA Packages

This chapter takes you through the steps to use the XtractIM tool in the simulation of the multi-die stacked BGA Package.

PREPARE FOR SIMULATION

Collect this information before you begin the simulation.

- Make sure your files have been translated into SPD format.
- Have the Stackup information ready.
- Have the Bump and Solderball diameters, length, heights and conductivity ready.

LESSON ONE: SIMULATION SETUP

Simulation Overview

1. Load an existing file (.xml file) or open a layout file (.spd file).
2. Select a package type: Wirebond or Flip-Chip, single BGA or stacked BGA.
3. Setup the circuits: **Die-circuit** or **Board circuit**.
4. Setup the **Stackup**. Set parameters for the Bump / Solderball medium layer.
5. Set the **Bump** data if you choose a Flip-Chip package.
6. Set the **Solder Ball** data. Select the nets for extraction.
7. Setup extraction frequency and capacitance / inductance output control.
8. Save the workspace.
9. Save Layout files.
10. Run the simulation.

Setup Package Simulation

Simulation setup is similar to the setup procedures described in *IBIS/RLGC Module: Net-based Simulation of Single-die Single-BGA Packages*. The only difference is in three steps.

- Select a Package Type
- Setup Circuits
- Setup Stackup

Setup Package Type

1. Click on the appropriate radio button from these options:

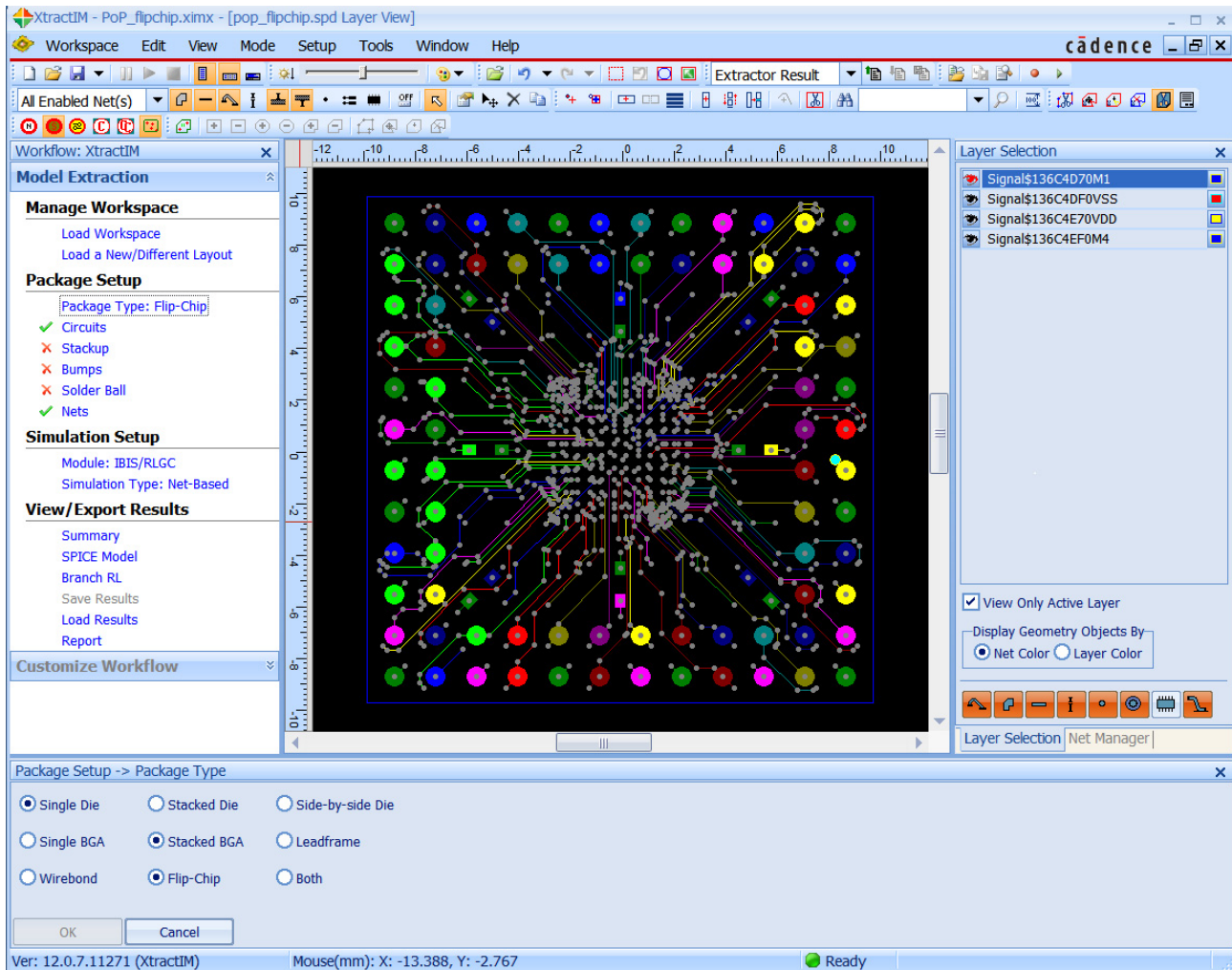
- Flip-Chip
- Side-by-side Die
- Single BGA
- Single Die
- Stacked BGA
- Stacked Die
- Wirebond

or select both Wirebond and Flip-Chip for various packages.

The default package type is **Single Die, Single BGA, Wirebond**.

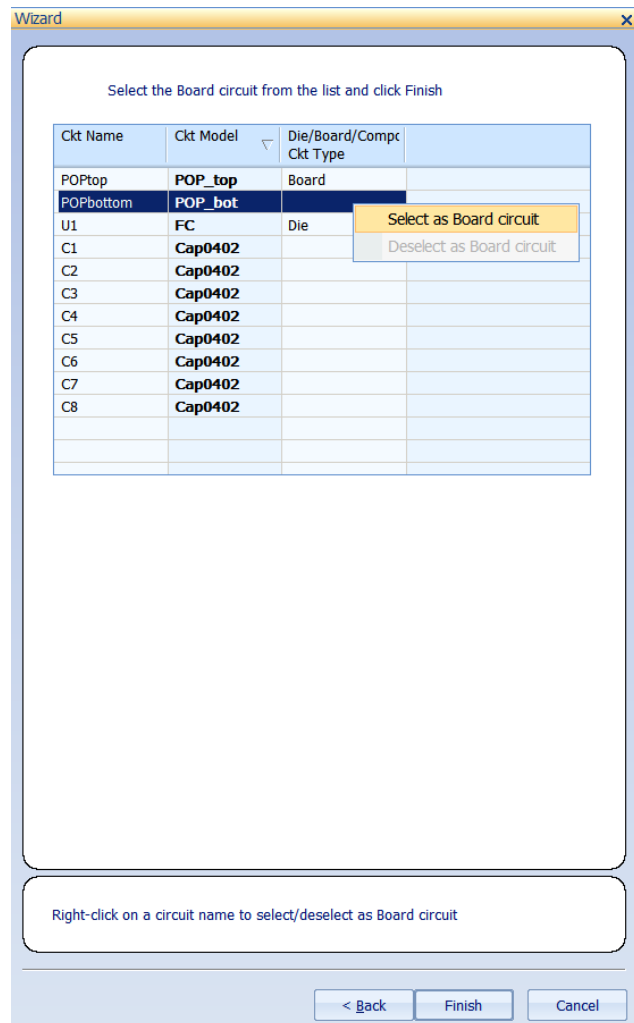
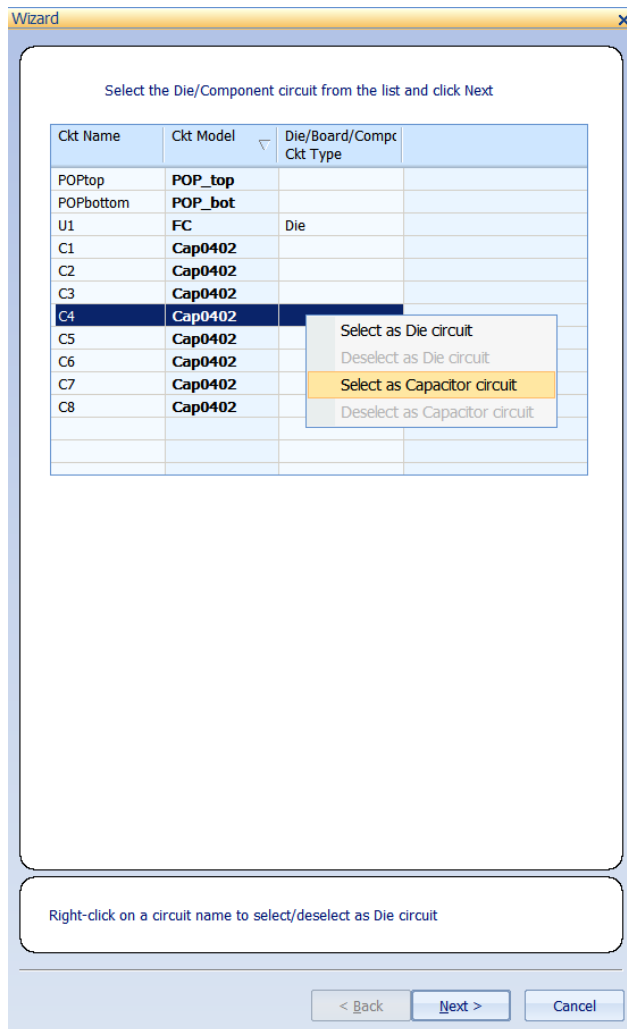
2. Click **OK** to save your selection.

3. Click **Cancel** if you wish to start over and re-enter your settings.



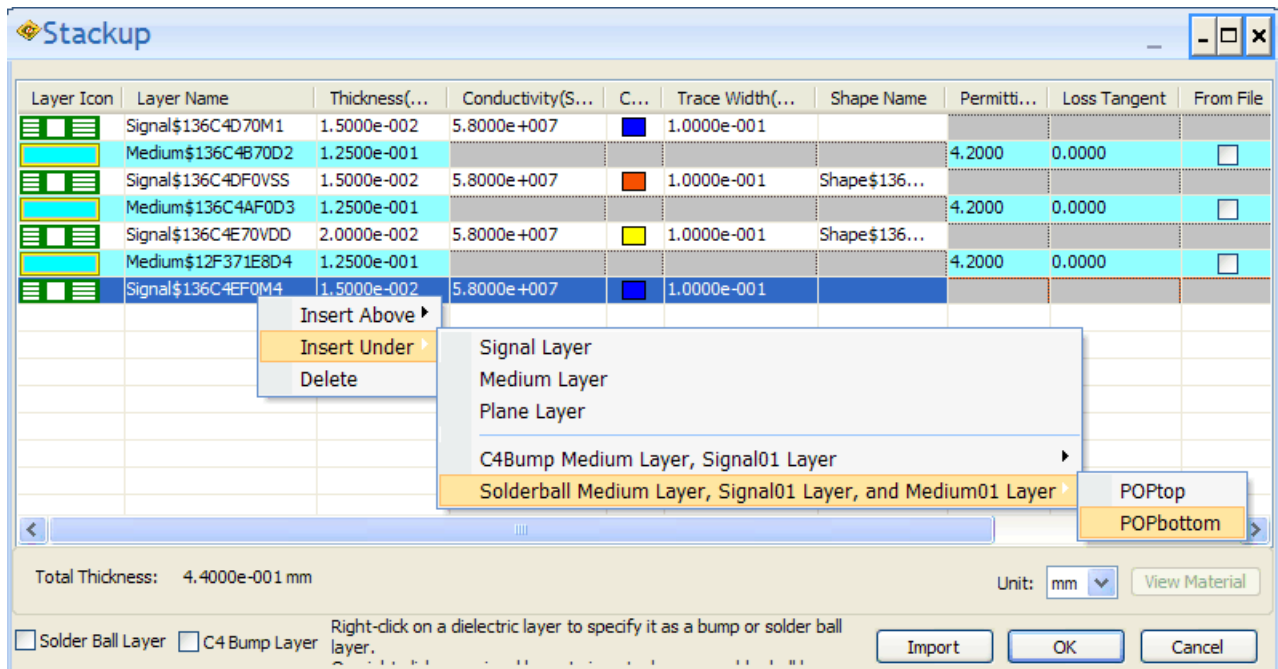
Setup Circuits

1. Click on **Circuits** in the Workflow pane to setup the Circuits data for a Flip-Chip package. A new pane opens.
2. Right-click on the desired circuit.
3. Select it as **Die** circuit (you can also select it as **Capacitor** circuit).
4. Click **Next**.
5. Right-click on another desired circuit.
6. Select it as a **Board** circuit.
7. To set up the second as a Board circuit, choose:
Select as Board circuit
8. Click **Finish** to finish the setup.
9. Select the multi-die circuit if the package has multi-dies.



Setup Stackup

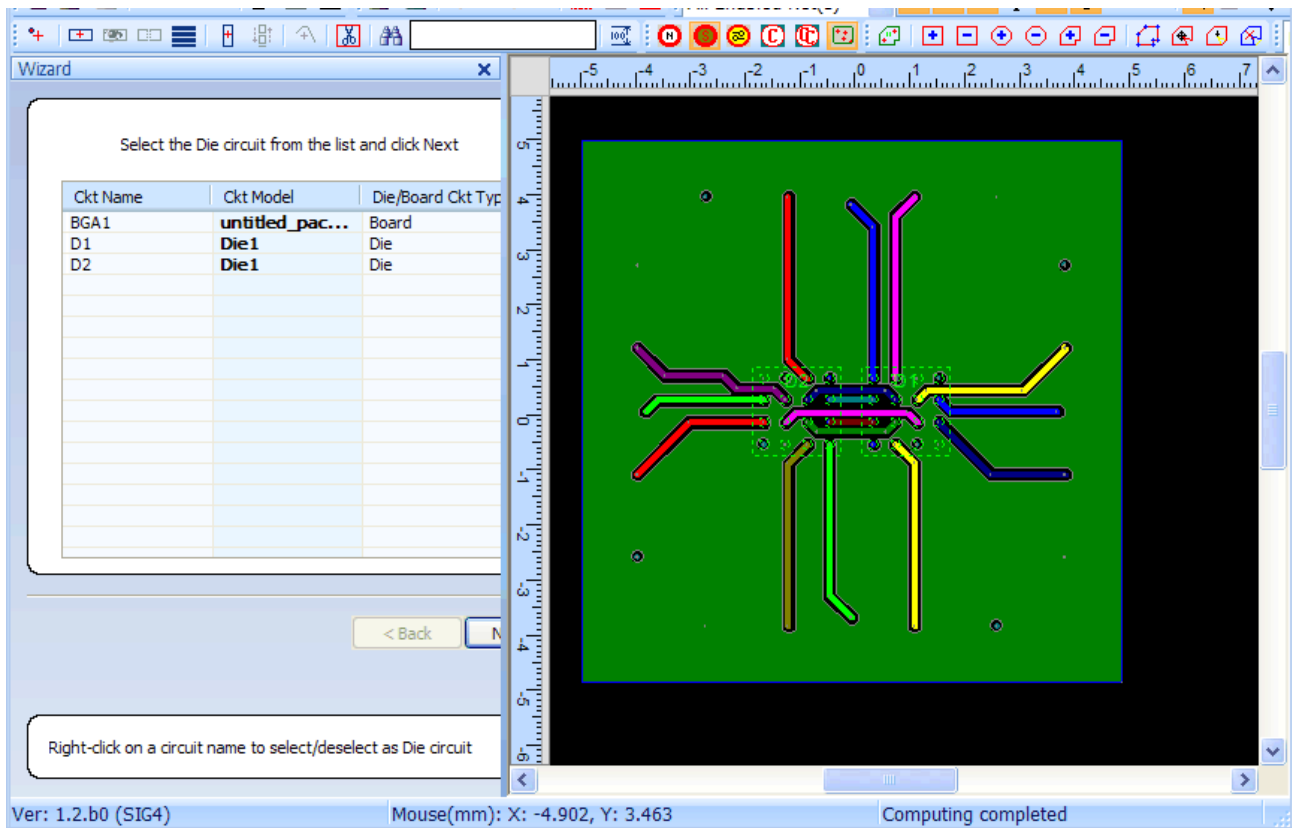
1. Click on **Stackup**. The Stackup window opens.
2. In the **Layer Name** column click on:
Signal\$Bottom layer (Signal\$136C4EF0M4)
A pop-up window opens.
3. Select
Insert Under
A second pop-up window opens and displays layer options.
4. Click:
Solderball Medium Layer, Signal01 Layer, and Medium01 Layer
A menu opens.
5. To insert all layers under the Signal\$Bottom layer (Signal\$136C4EF0M4)
POPbottom



Setup Bump and Solder Ball Medium Layers

The newly-added signal layer is found at the end of the solderball.

1. Right-click on the **Signal\$Top** layer.
2. Insert a **Bump Medium Layer** and a **signal layer** above Signal\$Top. The added signal layer is the end of the Bump.
3. Return to the **Stackup**.
4. View the Bump and Solder Ball Medium Layers as they are created.
5. Edit the medium parameters for Bumps, if desired.
6. Edit the solderball, if desired.
7. Edit the PCB medium layers, if desired.



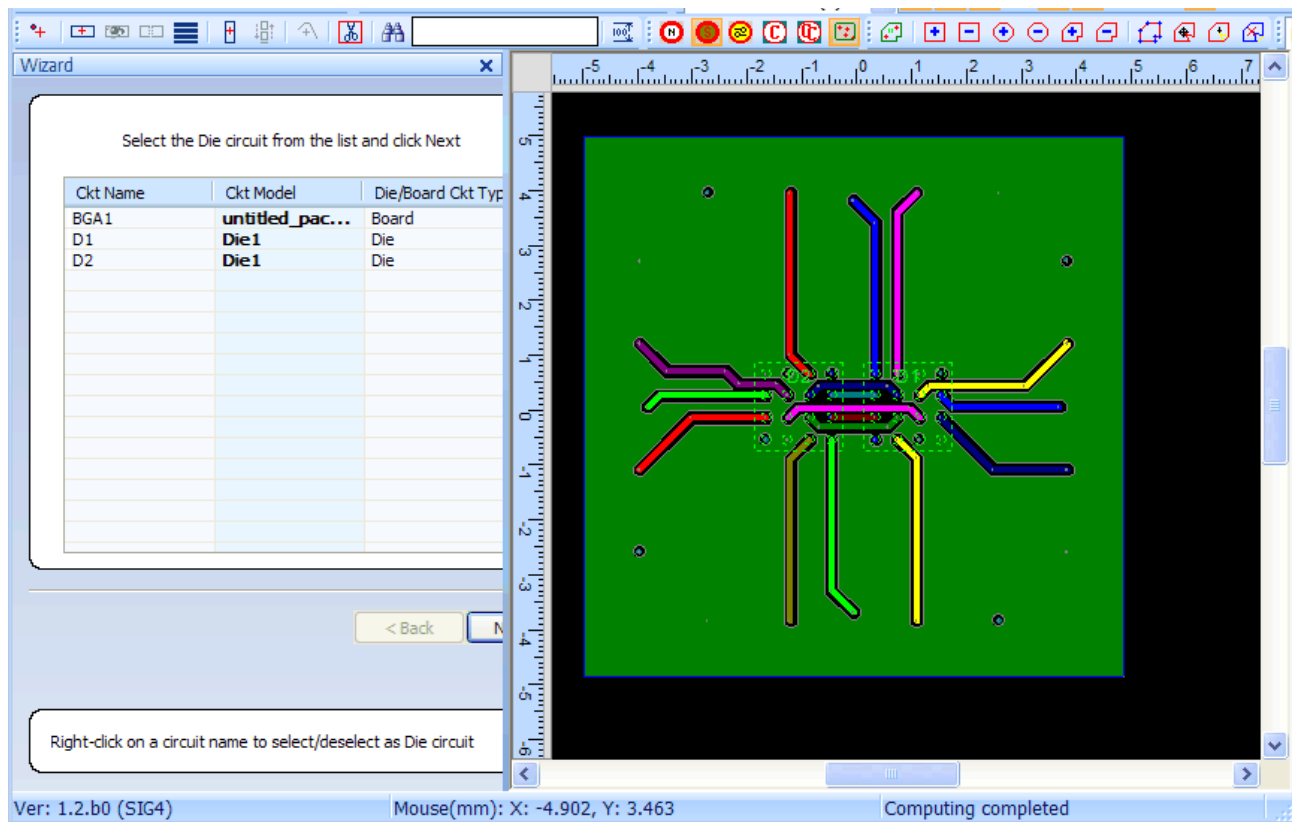
Setup Bumps to a Side-by-Side Die Package

If the side-by-side Die Flip-Chip package has the same Bump height in all die circuits, it is treated as a **distributed die package**.

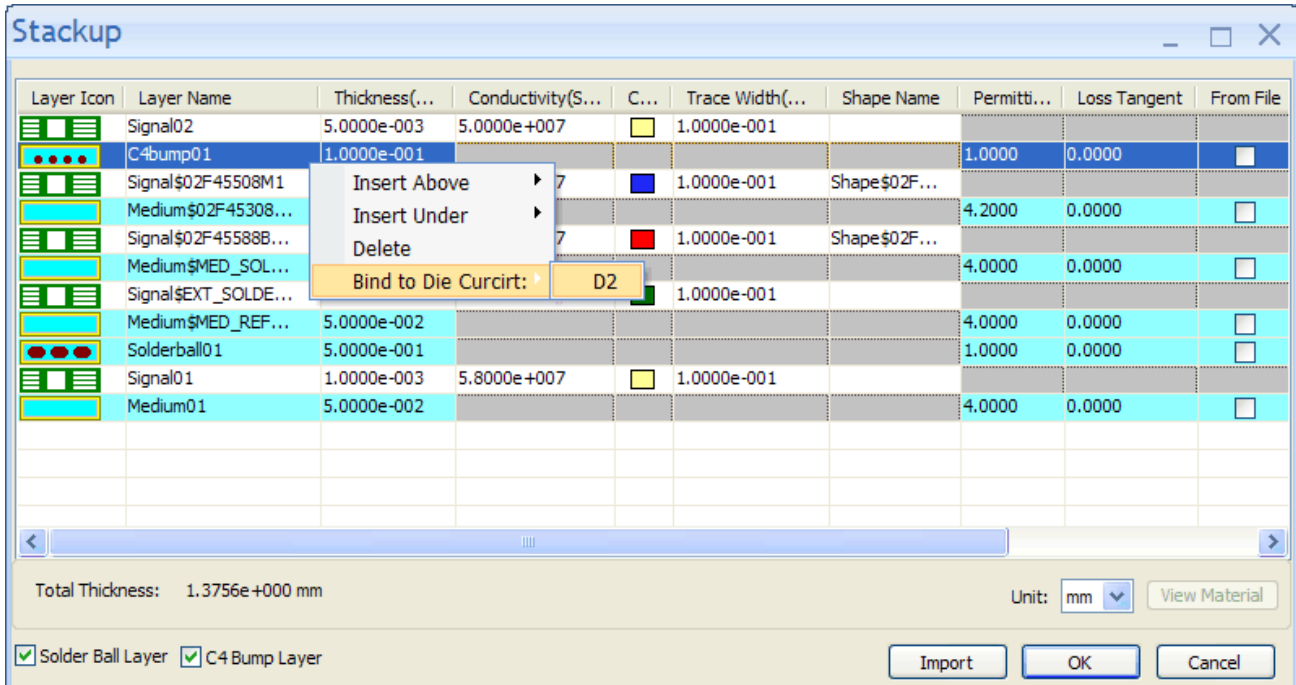
If the heights are different, it is treated as a stacked die package.

1. Add one Bump layer.
2. Open the **Stackup** for the distributed Bump die package.

You can bind them together to add the same Bump medium layer for each die circuit.



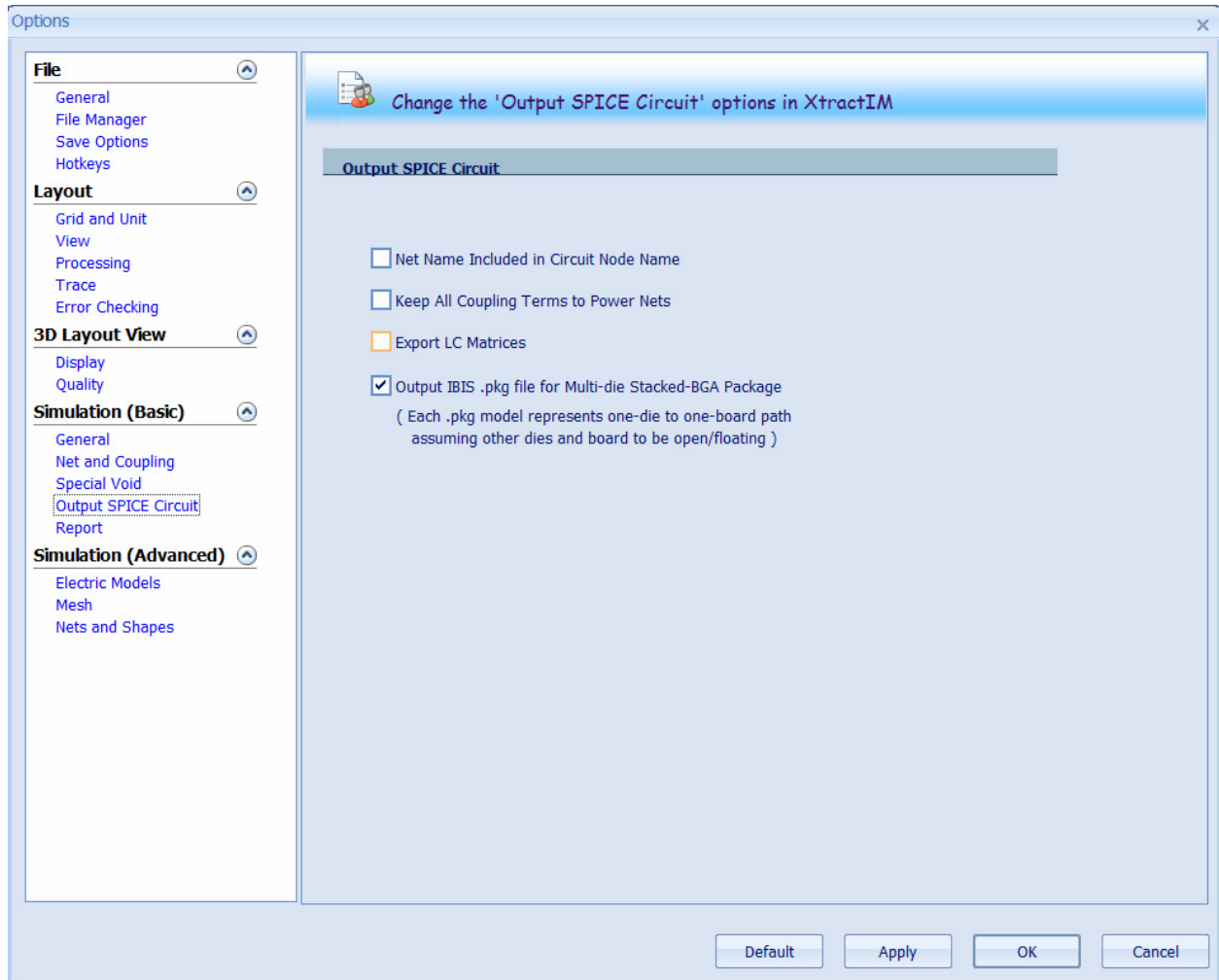
3. After adding the Bump for D1, select:
 Bind to Die Circuit: D2
 Both D2 and D1 have the same layer thickness.



Output IBIS .pkg Model for Each Die-to-Board Path

1. To output IBIS .pkg model for each die-to-board path, select Tools > Options > Edit options...

The **Options** window open.



2. Click **Output SPICE Circuit** under **Simulation (Basic)**.
3. Select the **Output IBIS .pkg file for Multi-die Stacked-BGA Package** checkbox.
4. Click **OK**.

LESSON TWO: SAVE WORK AREAS

Layout File

1. Click on the workspace.
2. Click on the **Open Layout File** icon (**green**) to open the project file.
3. Click on the **Save Layout File** icon (**green**) to save the project file.
4. Use **Save as** to save the layout file under a different name.


NOTE!

Saving the workspace does not automatically save the .spd file.
Saving the .spd file does not automatically save the workspace.

Workspace

1. Click on the workspace. The workspace opens. Note the workspace toolbar.
2. Click on the **Save Workspace** icon (**yellow**) in the toolbar.
3. To save the workspace under a different name, select:
Save as

LESSON THREE: RUN THE SIMULATION

Click on the **Play** button  at the top of the window to start the extraction (simulation).

XtractIM only extracts RLCG for the net which has at least one pin at the Die side and at least one pin at the board side.

At the beginning of the simulation, if some nets have Die-Board mis-match, a pop-up window opens. You are asked to select the next action.

- **Continue** — Continue the simulation
- **More Information** — Examine what nets are mis-matched
- **Stop** — Cancel the simulation

Investigate Mis-matched Nets

1. The **More Information** window lists all the mis-matched nets.
2. Investigate the mis-matched nets to see whether it is a special design or a defective design.
3. Decide whether or not to proceed with the simulation.
4. Choose **Continue**, **Stop** or **More Information**.

If 30 seconds pass and the user has not made a choice; by default, the simulation continues.

LESSON FOUR : OBSERVE AND SAVE SIMULATION RESULTS

XtractIM performs calculations for each net. The calculations include:

- Conductance
- Mutual capacitance with other nets
- Mutual loop inductance
- Resistance
- Self capacitance
- Self loop inductance

Display SPICE Model Results

The illustration in the right corner shows the detail of the Circuit topology for a 2-die BGA package.

The screenshot shows the XtractIM software interface. The main window is titled 'Extractor Result'. On the left, there is a sidebar with various options: 'Manage Workspace', 'Package Setup', 'Simulation Setup', and 'View/Export Results'. The 'View/Export Results' section is expanded, showing options like 'Summary', 'SPICE Model', 'Branch RL', 'Save Results', and 'Load Results'. The main area of the window displays a 'View Model Selection' panel with four radio buttons: 'SPICE T-model' (selected), 'DC_R of Each Path', 'RLC of Each Path', and 'Coupling of Each Path'. To the right of this panel is a circuit diagram showing two dies (D1 and D2) connected to a BGA package (BGA1). Below the diagram is a list of net connections:

```

SUBCKT XIM_MultiDie_Sample3_WB2distributed_2diesidebyside_wbwb_newn1_NetBaseSPICE
+
+   D1_10      BGA1_10
+   D2_10
+   D2_4       BGA1_4
+   D2_3       BGA1_3
+   D1_13      BGA1_13
+   D1_14      BGA1_14
+   D1_4       D2_12
+   D1_3       D2_13
+   D1_2       D2_14
+   D2_2       BGA1_2
+   D1_7       BGA1_7
+   D2_7
+   D1_19      BGA1_19
+   D2_19
+   D1_8       BGA1_8
+   D2_8
+   D1_18      BGA1_18
+   D2_18
+   D1_9       BGA1_9
+   D2_9

```

The status bar at the bottom of the window shows 'Ver: 4.0.1.04171 (SIG4)', 'Mouse(um): X: -8692.371, Y: 5569.138', and 'Ready Computing completed'.

View DC Resistance

1. To view the DC Resistance of Power, Ground and Signal Nets of each circuit-to-circuit path, click:

DC_R of Each path

2. In the drop-down pane make a selection for a circuit-to-circuit path. In the following example the selection is:

D1 > D2

Extractor Result

View Model Selection

SPICE T-model

DC_R of Each Path

RLC of Each Path

Coupling of Each Path

D1 -> D2

NetName	DC_R(Ohm)
vdd	0.0128746
Net_12	0.0286816
Net_13	0.0286816
Net_14	0.0286816
Net_3	0.0821354
Net_4	0.0835846
Net_5	0.0781685
Net_6	0.0781685
Net_7	0.082948
Net_8	0.0824216
gnd	0.00852792

m): X: -8692.371, Y: 5569.138

Ready Computing completed

Display RLC of Each Path

1. To view the **Net Length**, **Self R**, **Self L**, **Self C**, or **Delay** of a Signal Net., click on RLC of Each Path
2. Use the drop-down pane to select a circuit-to-circuit path.

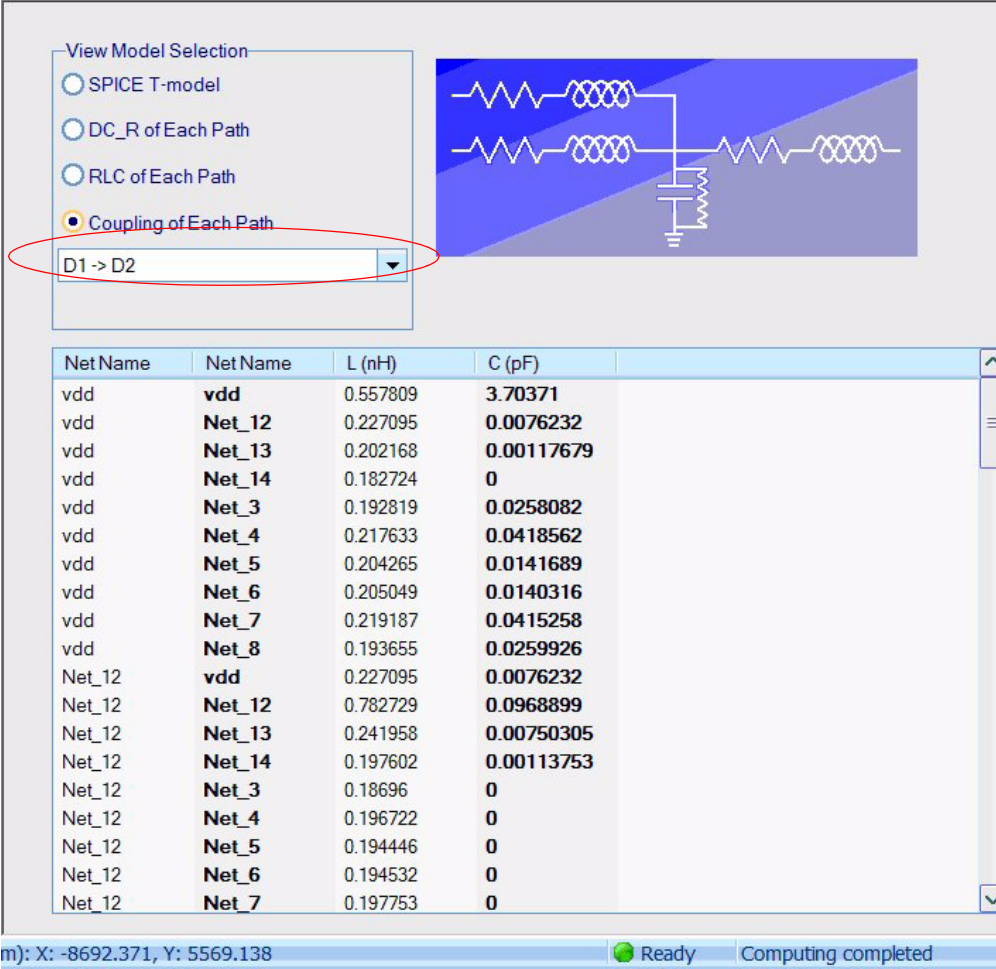
The screenshot shows the 'Extractor Result' window. On the left, under 'View Model Selection', the 'RLC of Each Path' radio button is selected. Below it, a dropdown menu is set to 'D1 -> D2'. To the right is a circuit diagram with a blue background. Below the settings is a table with the following data:

SignalNetNa...	NetLength(m...	SelfR(Ohm)	SelfL(nH)	SelfC(pF)	Delay(pS)
vdd		0.0259458	0.557809	3.70371	45.4529
Net_12	0.865615	0.0389037	0.782729	0.0968899	8.70853
Net_13	0.865615	0.0388801	0.774898	0.097438	8.68934
Net_14	0.865615	0.0390491	0.750168	0.0969146	8.52656
Net_3	7.32683	0.136337	5.14279	1.0151	72.2526
Net_4	7.62281	0.139003	5.43555	1.02052	74.4787
Net_5	6.72973	0.135472	5.03568	1.09907	74.3948
Net_6	6.72973	0.136465	5.21655	1.10419	75.8949
Net_7	7.4928	0.138143	5.37479	1.04397	74.9076
Net_8	7.38528	0.13889	5.51948	1.0466	76.0047

At the bottom of the window, the status bar shows 'm): X: -8692.371, Y: 5569.138', a green 'Ready' indicator, and 'Computing completed'.

Display Coupling of Each Path

1. To view **Mutual Inductance** among nets along the path, click:
Coupling of Each Path
2. Use the drop-down pane to select the circuit-to-circuit path.



View Model Selection

SPICE T-model
 DC_R of Each Path
 RLC of Each Path
 Coupling of Each Path

D1 -> D2

Net Name	Net Name	L (nH)	C (pF)
vdd	vdd	0.557809	3.70371
vdd	Net_12	0.227095	0.0076232
vdd	Net_13	0.202168	0.00117679
vdd	Net_14	0.182724	0
vdd	Net_3	0.192819	0.0258082
vdd	Net_4	0.217633	0.0418562
vdd	Net_5	0.204265	0.0141689
vdd	Net_6	0.205049	0.0140316
vdd	Net_7	0.219187	0.0415258
vdd	Net_8	0.193655	0.0259926
Net_12	vdd	0.227095	0.0076232
Net_12	Net_12	0.782729	0.0968899
Net_12	Net_13	0.241958	0.00750305
Net_12	Net_14	0.197602	0.00113753
Net_12	Net_3	0.18696	0
Net_12	Net_4	0.196722	0
Net_12	Net_5	0.194446	0
Net_12	Net_6	0.194532	0
Net_12	Net_7	0.197753	0

m): X: -8692.371, Y: 5569.138 Ready Computing completed

Summary of the Extracted Results

1. Click on **Summary** to open a brief summary of the extracted R, L, and C in the SPICE circuit.
2. View the maximum and minimum values, and other information in the **Brief Summary** window.

Extractor Result	
[Version]	4.0.1.04171
[Date]	04/16/2010
[Package Name]	C:\Users\gkang\Desktop\Samples\Multi-die_Sample_
[Description]	C:\Users\gkang\Desktop\Samples\Multi-die_Sample_
[Nets Extracted]	16
[Frequency of Extraction]	30MHz
[Max R (mOhm)]	62.2883
[Min R (mOhm)]	7.26778
[Max self-inductance L (nH)]	2.40819
[Min self-inductance L (nH)]	0.356281
[Max self-capacitance C (pF)]	3.70371
[Min self-capacitance C (pF)]	0.0968899

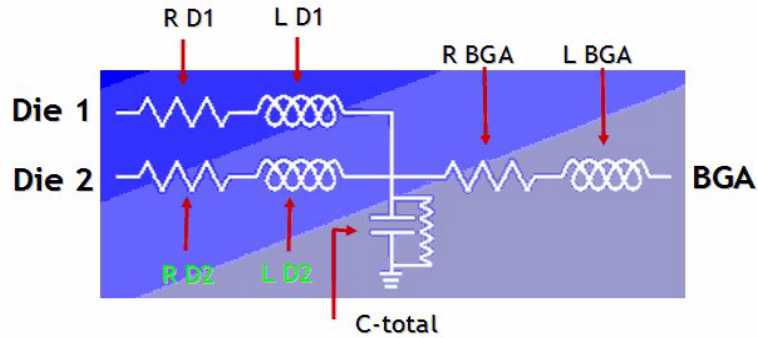
Branch RL and Total C

Click **Branch RL** to view the display the **Branch R, L**, and total **C** of each net.

If a branch is missing from a net, the cell is left empty.

Extractor Result							
Net Name	C-total (pF)	R D1(Ohm)	R D2(Ohm)	R BGA1(Ohm)	L D1(nH)	L D2(nH)	L BGA1(nH)
vdd	3.70371	0.0189957	0.0190755	0.00726778	0.502131	0.494327	0.360268
Net_0	0.586283		0.0499985	0.0144941		1.34022	0.898667
Net_1	0.519641		0.0467442	0.0123515		1.23658	0.78594
Net_10	0.507267	0.046825		0.012005	1.33644		0.779702
Net_11	0.573214	0.0502395		0.0140962	1.4453		0.889757
Net_12	0.0968899	0.0183871	0.0502395		0.3721	1.4453	
Net_13	0.097438	0.0183802	0.0183871		0.368179	0.3721	
Net_14	0.0969146	0.0184685	0.0183802		0.356281	0.368179	
Net_2	0.585876		0.0499099	0.0142809		1.32604	0.843666
Net_3	1.0151	0.0611592	0.0589	0.012166	2.2961	1.89191	0.955124
Net_4	1.02052	0.0622883	0.0594929	0.0125821	2.40819	1.96941	1.00588
Net_5	1.09907	0.0607214	0.0603477	0.0129294	2.1364	2.03507	1.023
Net_6	1.10419	0.0607857	0.0610096	0.0129482	2.12252	2.17874	1.0308
Net_7	1.04397	0.0602726	0.0612385	0.012329	2.08603	2.26651	0.99801
Net_8	1.0466	0.0602456	0.0619516	0.0123209	2.07494	2.39202	0.998978
Net_9	0.5723	0.050101		0.0138617	1.42172		0.833771

The figure below illustrates the Branch RL and Total-C for one net of a 2-die 1-BGA package. It is straightforward for multi-die stacked-BGA packages.



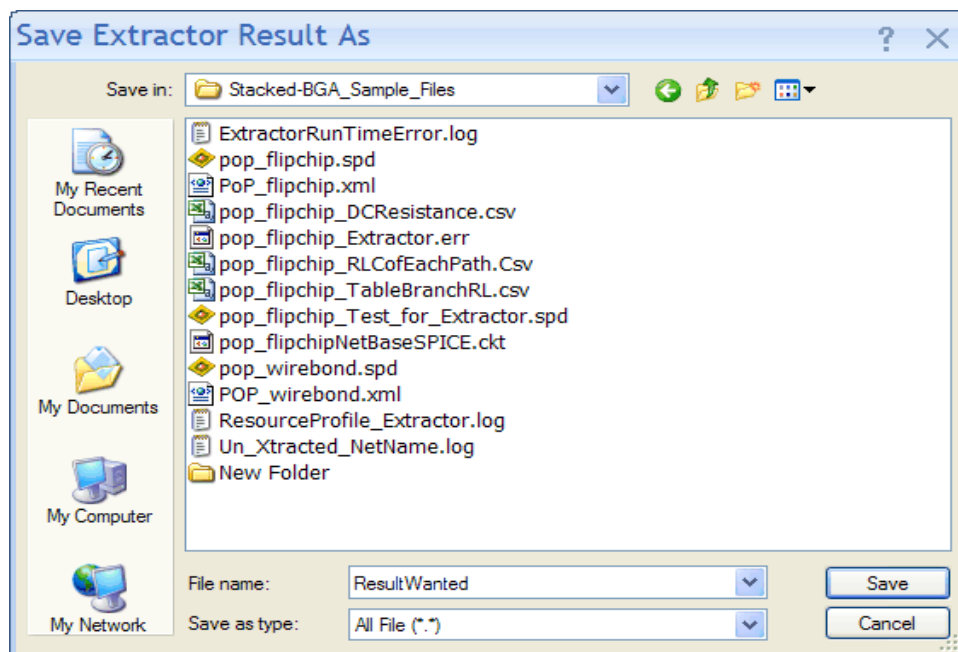
Save Results and Output Files

1. Click:
Save Results
The **Save Extractor Result** window appears.
2. Enter a name in the **File name** window.
3. Click on **Save**. The results are saved in a binary file named as result and as:
result_spd_file_name.xim
4. Click on **Cancel** if you do not want to save the results in the file name you entered.
5. Save all the output data including Summary and one SPICE model in the **result** and **result*.xim** files.

The result file is created only when the user chooses to save the output data.

You'll see these output files on hard disk.

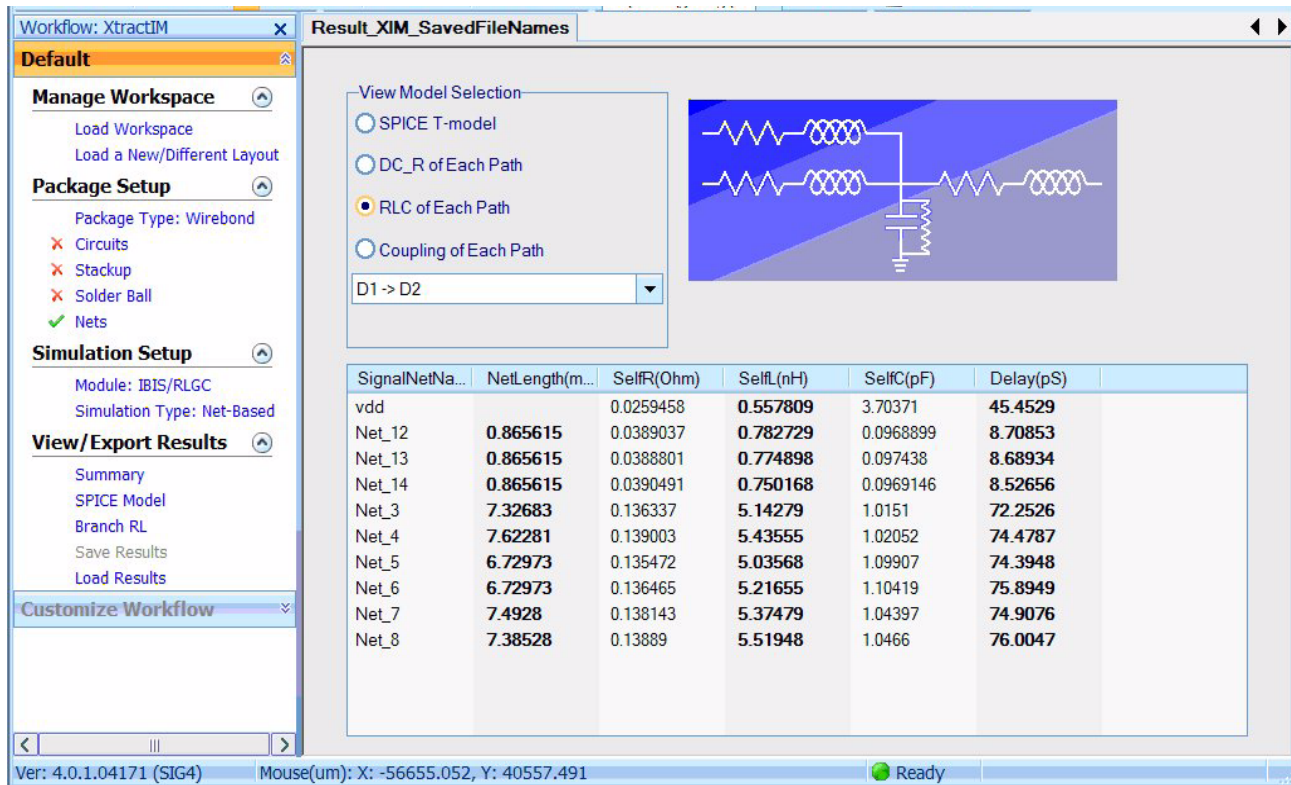
- **Branch RL File** — An .csv file including the branch R, L, and total C of each net
- **Coupling of Each Patch** — A .csv file including Mutual L and Mutual C among nets along every circuit-to-circuit path
- **DC R of Each Path File** — A .csv file including each net's DC Resistance
- **One SPICE Circuit File** — Named *.ckt
- **RLC of Each Path File** — A .csv file including each Signal net name, Length, Self R, Self L, Self C and Delay



Load in Saved Results and Files

1. To load saved results, select:
Load Results
2. View the present results or the loaded results.
3. Unload a loaded result by clicking on the **Unload Extractor Result** icon in the toolbar.
4. Use the **Load** and **Unload Result** buttons.

All output files, including .csv files, are saved in the same directory as the *.spd file.



LESSON FIVE: BATCH MODE SIMULATION

1. To run a simulation in Batch Mode select:
Start -> Run
2. Change to the directory where the XtractIM.exe file is located.

Batch Mode Example

If you want to use the project (.spd file) defaulted in the workspace file (.xml file), enter:

```
xtractIM -b "Full_path_toMy_xml_File\xml filename"
```

If you want to use a different project file other than the one in the .xml file, enter:

```
xtractIM -b "Full_path_toMy_xml_File\xml  
filename" "Full_path_toMy_xml_File\new_spd-filename"
```

Optimized Broadband Module: Net-based Simulation for Single-die Single-BGA Packages or Multi-die, Stacked-BGA Packages

This chapter takes you through the steps to use the XtractIM tool Optimized Broadband Module in the net-based simulation of a single-die BGA package. Simulation of multi-die, stacked-BGA packages is the same as single-die, single-BGA packages.

LESSON ONE: SETUP FOR THE SIMULATION

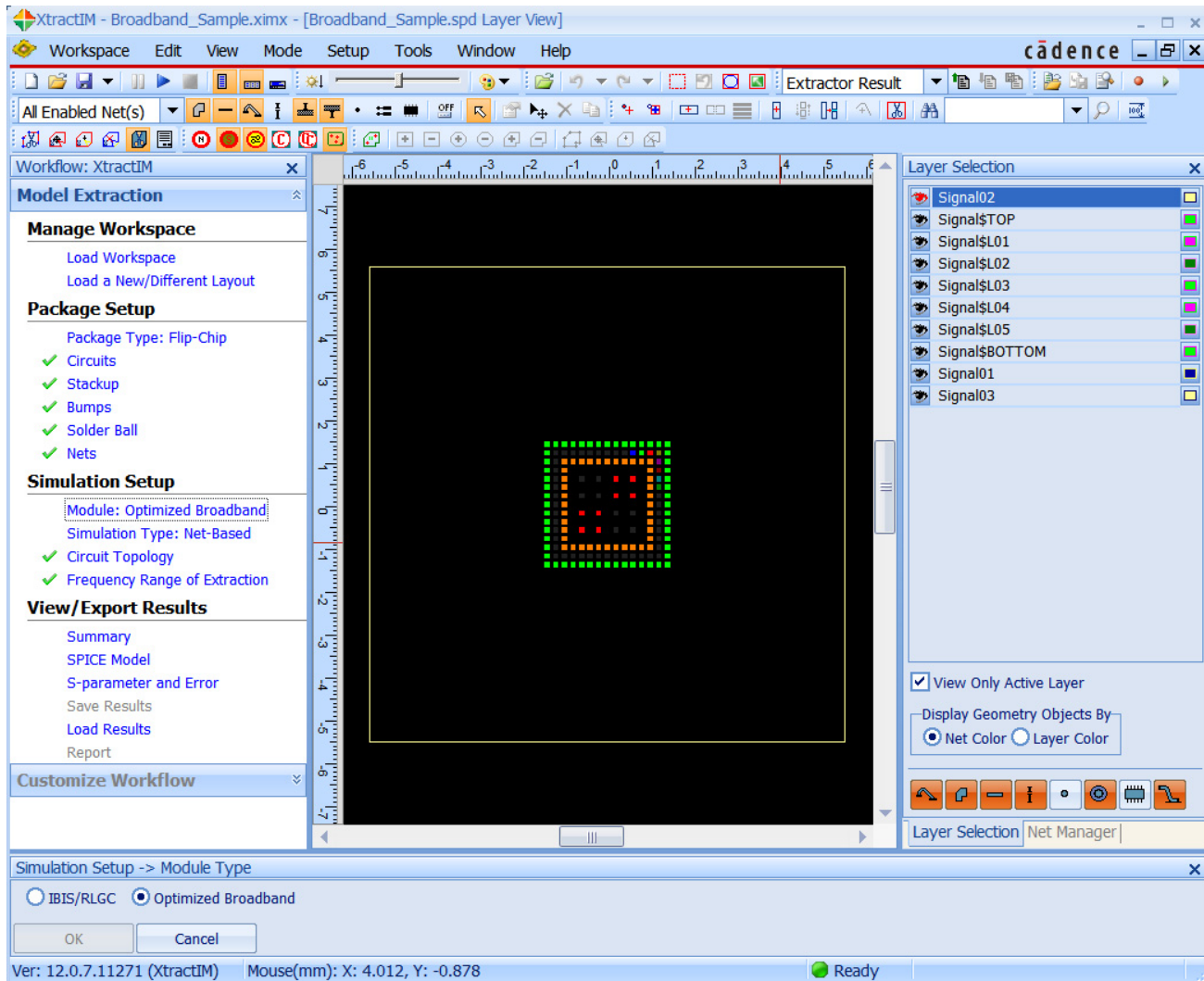
Package and Simulation Setup

1. Load an existing workspace file (.xml file).
2. Open a layout file (.spd file).
3. Select a package type: wirebond or flip-chip.
4. Setup the circuits: select or deselect Die-circuit and Board circuit.
5. Set the Stackup: set parameters for the Bump / Solderball medium layer.
6. Set the Bump data if it is a flip-chip package.
7. Set the Solder Ball data.
8. Select the **nets** for extraction.
9. Select Simulation Module: Optimized Broadband Module.
10. Select output SPICE circuit.
11. Setup the Extraction Frequency band.
12. Save the Workspace and Project file.

Steps 1-8 and Step 11 are exactly the same as *Preparing for the Simulation* in *IBIS/RLGC Module: Net-based Simulation of Single-die Single-BGA Packages*. This chapter describes steps 9-10 in detail.

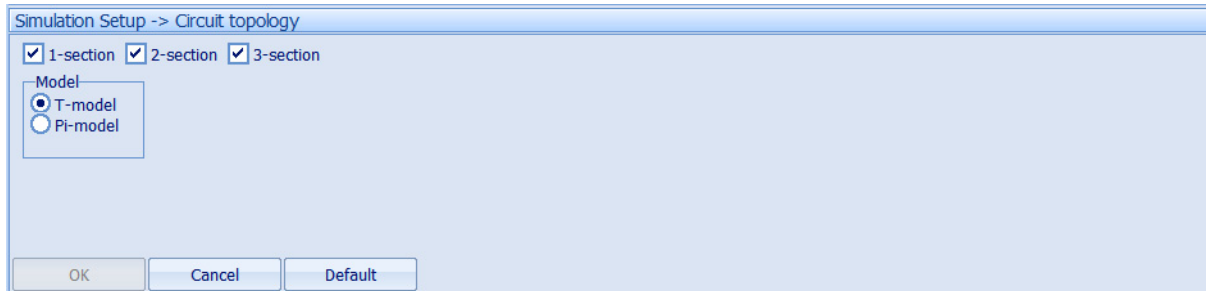
Simulation Setup

1. Select:
Simulation Setup -> Module
2. Select the **IBIS/RLGC Module**;
or select **Module: 6**.

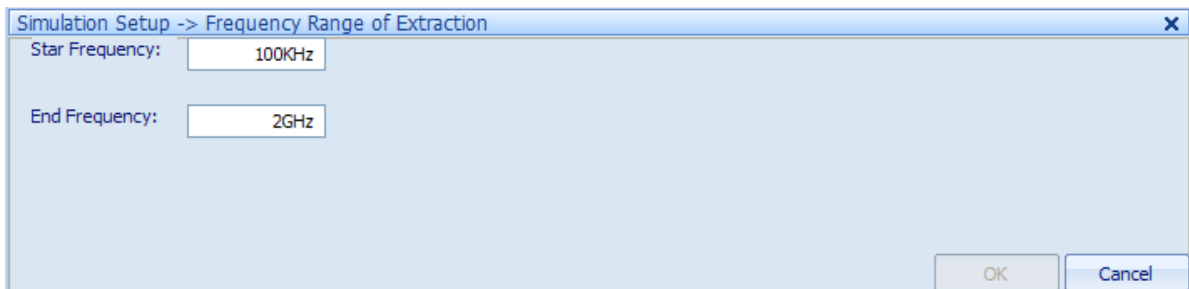


3. In the workflow window click:
Circuit Topology

4. Select the circuits to be extracted under the **Circuit Section**.
 - If you do not select a circuit, no RLGC SPICE model is extracted
 - If you select all of the circuits, all three models will be given
 - If you select a single circuit, choose **T-model** or **Pi-model**



5. In the Workflow pane click:
Frequency Range of Extraction
6. Set the **Frequency Range**.
7. Input the lower frequency and the upper frequency.



Output Original S-parameter with More Format

By default the original S-parameter is saved as a BNP file.

1. Select:
Tools > Options > Edit Options > Original S-parameter: More Format
2. Select:
Original S-parameter in Touchstone
A file with Touchstone format is also saved.
3. Select:
Original S-parameter in BNP AFS format
A file with BNP AFS format is also saved.

LESSON TWO: SAVE WORK AREAS

Layout File

1. Click on the workspace.
2. Click on the **Open Layout File** icon (**green**) to open the project file.
3. To save the layout file under a different name, select:
Save as


NOTE!

Saving the workspace automatically saves the .spd file.
Saving the .spd file does not automatically save the workspace.

Workspace

1. Click on the workspace. The workspace opens.
2. View the Workspace toolbar.
3. Click on the **Save Workspace** icon (**yellow**) in the toolbar.
4. To save the workspace under a different name, select:
Save as

LESSON THREE: RUN THE SIMULATION

1. Click on the **Play** button  at the top of the window to start the extraction (simulation).
2. The Optimized Broadband **Module** only extracts RLCG for the net which has at least one pin at the Die-side and at least one pin at the board side.

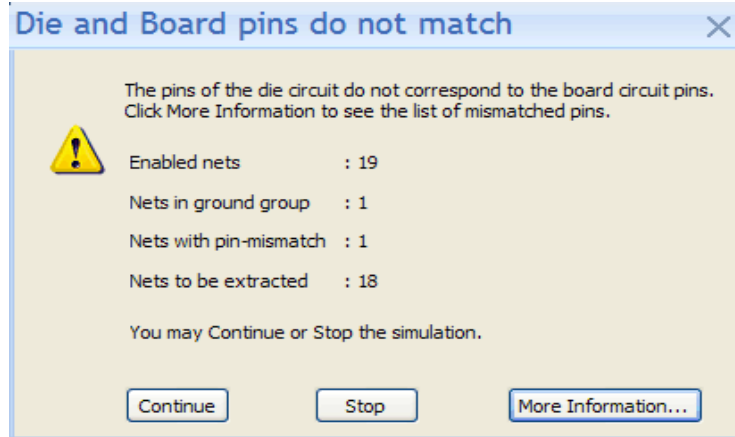
At the beginning of the simulation, if some nets have Die-Board mis-match, a pop-up window opens.

3. Select the next action.
 - **Continue** — Continue the simulation
 - **More Information** — Examine what nets are mis-matched
 - **Stop** — Cancel the simulation

Investigate Mis-matched Nets

1. The **More Information** window lists all the mis-matched nets.
2. Investigate the mis-matched nets to see whether it is a special design or a defective design.
3. Decide whether or not to proceed with the simulation.
4. Choose **Continue**, **Stop** or **More Information**.

If 30 seconds pass and the user has not made a choice; then, by default, the simulation continues.



LESSON FOUR : OBSERVE AND SAVE SIMULATION RESULTS

XtractIM performs calculations for each net. The calculations include:

- Conductance
- Mutual Capacitance with other Nets
- Mutual Loop Inductance
- Resistance
- Self Capacitance
- Self Loop Inductance

About the S - Parameter and Errors

After the simulation completes, view the S-parameter and errors in the Layer View window

- **Bottom figure (S Imaginary)** — Imaginary / phase of the S-parameter element
- **Middle figure (S Real)** — Real / amplitude of the S-parameter element
- **Top figure (Average error in S)** — Average S-parameter error for each net

View S - Parameter and Errors

1. Drag the black vertical marker to **Net i**. The S_{ii} is shown.
2. Click on net names in the middle column to view the:
Frequency-averaged S-parameter error of the circuit S-parameter vs. the Original S-Parameter
3. View the port names listed with net names plus port at Die- or Board- side.
4. View the average error for 1-, 2- and 3-section circuit topology.
5. Return to **Net i**.
6. View all sections, single section, or two sections results.
7. View averaged S-parameter errors of a non-optimized or optimized circuit.
8. View the port name in the error column to view any mutual S-parameters.

S-parameter Examples

The error definition of circuit S-parameter vs. original or simulated S-parameter is shown in these examples.

Define an error for each net

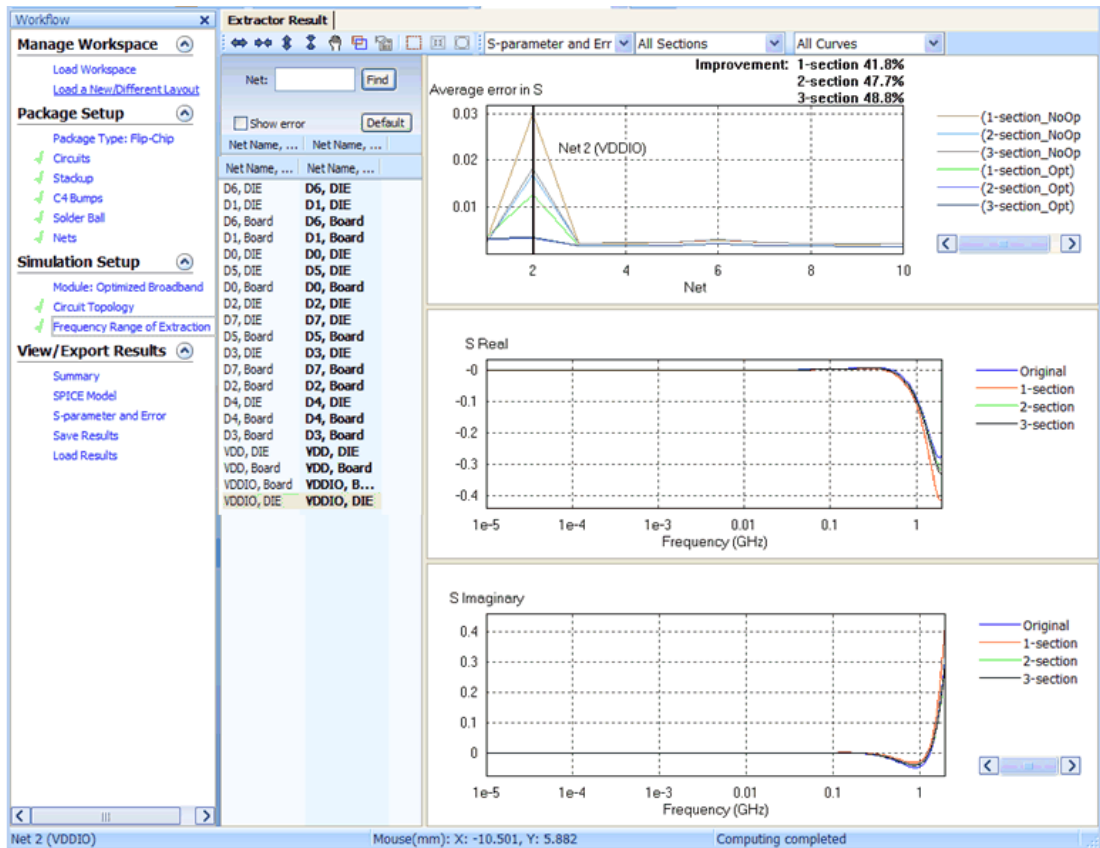
$$\text{Error}(\text{net}, \text{freq}) = \frac{1}{4} \cdot \{|S_{11_ckt} - S_{11_sim}| + |S_{22_ckt} - S_{22_sim}| + |S_{12_ckt} - S_{12_sim}| + |S_{21_ckt} - S_{21_sim}|\}$$

Net-averaged performance vs. frequency

$$\text{Error1}(\text{freq}) = \frac{1}{\text{Net_No}} \sum_{\text{Net}} \text{Error}(\text{net}, \text{freq})$$

Freq-averaged performance vs. net

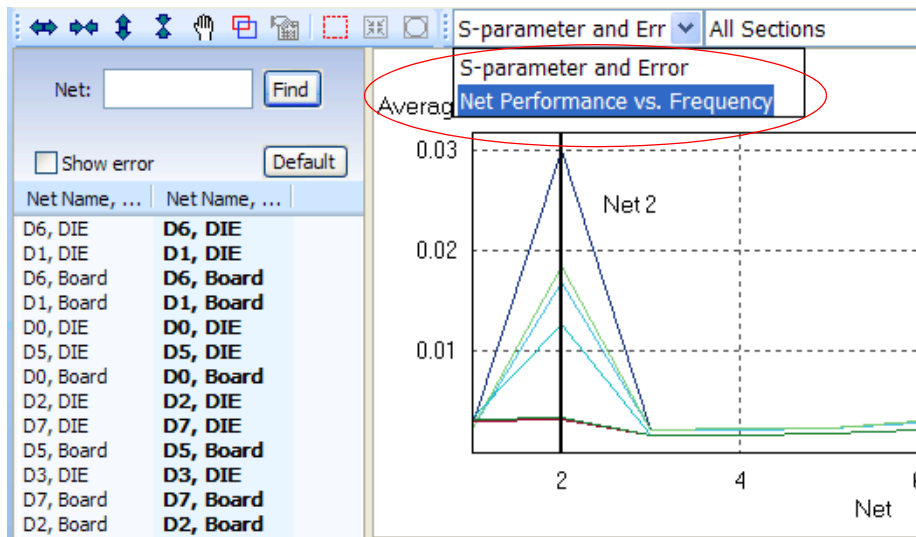
$$\text{Error2}(\text{net}) = \frac{1}{\text{Freq_No}} \sum_{\text{Freq}} \text{Error}(\text{net}, \text{freq})$$



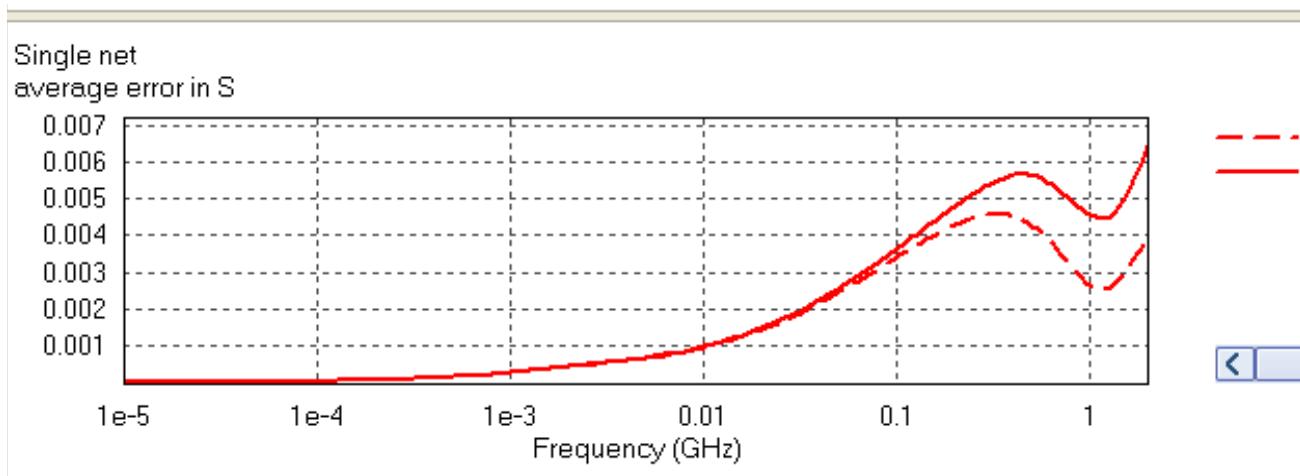
View Net Frequencies

1. Click the **S-parameter** button in the toolbar.
2. In the drop-down menu, select:
Net Performance vs. Frequency

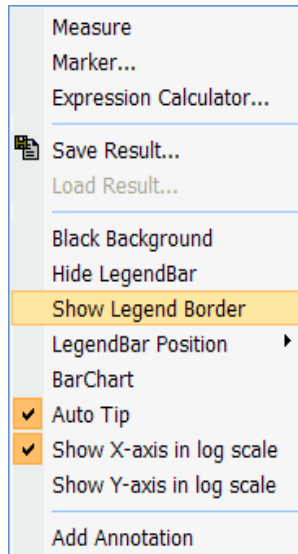
The frequency is displayed in the Layer View window.
3. Click on a net name in **Net Name** list.
4. View the Single net average error in **S chart**.



5. Click on each net name in the list.
6. View the Single net average error in S chart for every net.

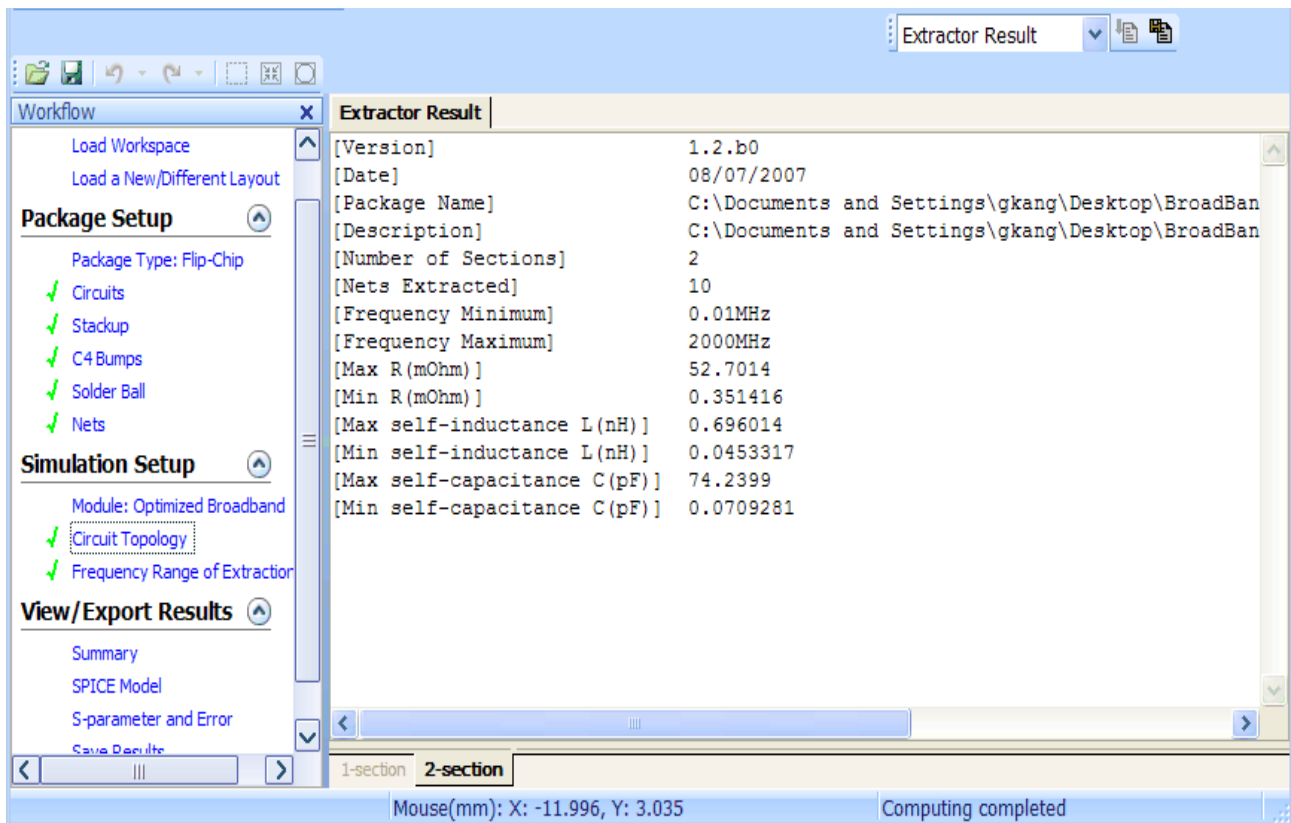


7. Click on a figure. A pop-up menu appears.
8. Click:
Show Legend Border

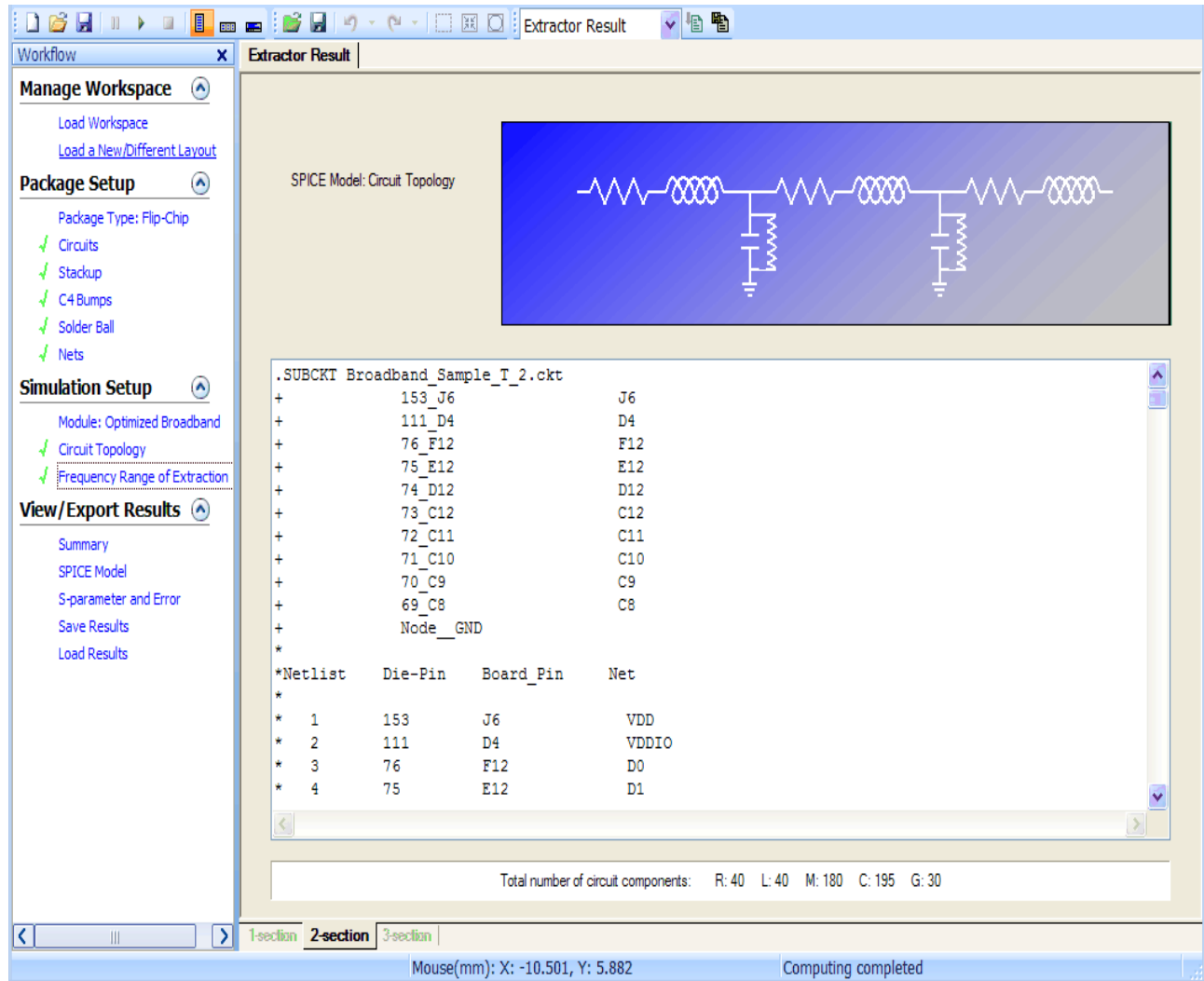


View Summaries and Models

1. Click on **Summary** to bring up the summary and tabulated data for R, L, and C.
2. View the overall results in the top right window.
3. Examine the results for:
 - Frequency Minimum
 - Frequency Maximum
 - Max R
 - Max self-capacitance C
 - Max self-inductance L
 - Min R
 - Min self-capacitance C
 - Min self-inductance L
 - Package Name
4. Click on **SPICE Model** to bring up the display of the SPICE Circuit model.



5. To see the SPICE Model circuit topology click:
- 1-section
 - 2-section
 - 3-section



Save and Load Results

1. Click **Save Result** in the workflow. The **Save Extractor Result** as window opens.
2. Enter a **name**.
3. Save the **result**.

The result file:

- Is saved in a binary file named **result** and **result_spd_file_name.xim**
- Contains all the files (all the .csv file names)
- Can be loaded into XtractIM

4. In the Workflow pane click:

Load result

The pre-saved result is loaded.

5. Open the **S-parameter view** file and check the information.
6. Open the **Summary view** file and check the information.

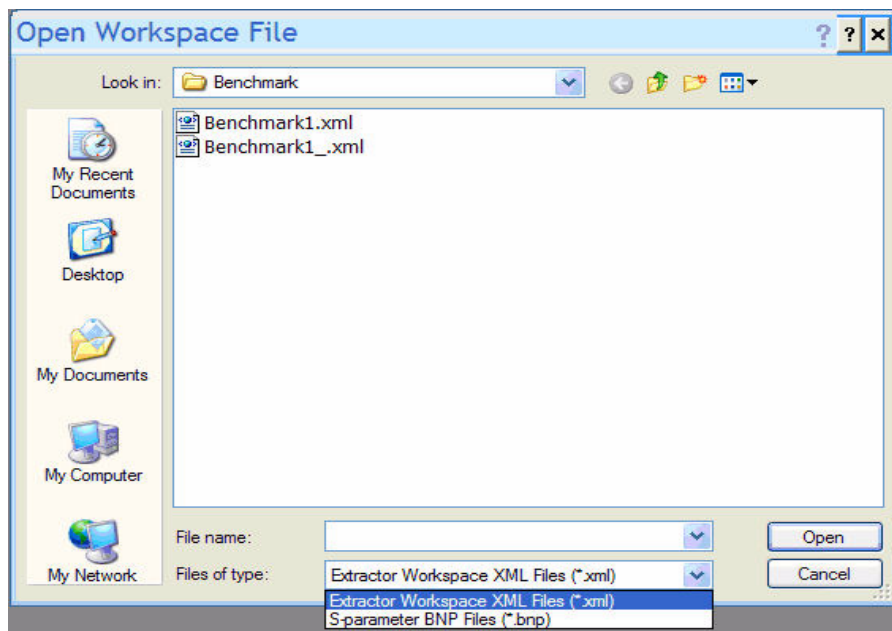
LESSON FIVE: BROADBAND EXTRACTION OF EXISTING S-PARAMETER

A typical workflow in interaction mode includes the steps described in *Load BNP Files and Setup for Simulation*.

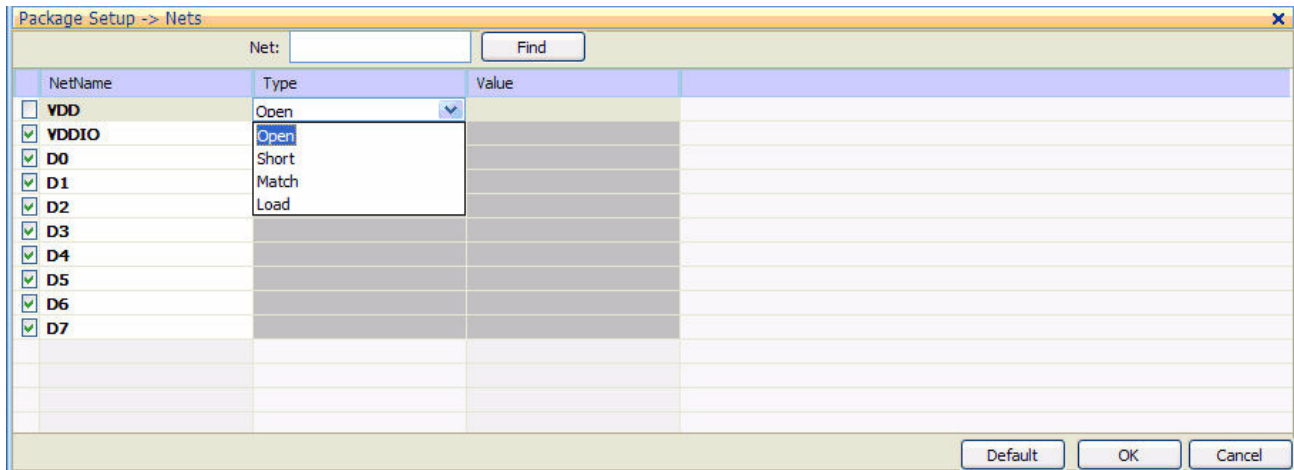
Only supported BNP files are created by XtractIM.

Load BNP Files and Setup for Simulation

1. Launch **XtractIM**.
2. Open the Workspace file.
3. Select the desired file from the pull-down menu in the **Files of type** field.



4. Select:
Extractor Workspace XML files

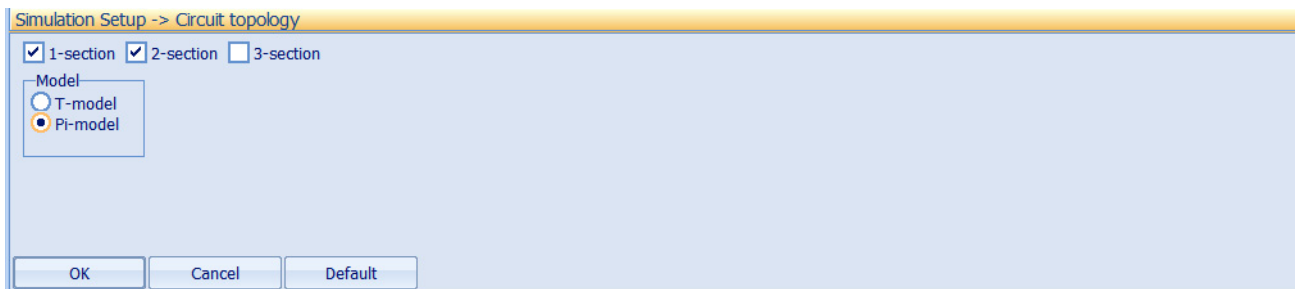


Select Circuit Topology

1. In the Workflow pane click:
Circuit Topology
 2. To open the pull-down menu click:
Circuit Section
 3. Select the circuits to be extracted: **T-model** or **Pi-model**.
- If you do not select a circuit, no RLGC SPICE model is extracted.
If you select all of the circuits, all three models are given.

Example

- Pi-model has already been selected for 1-section
- 1- Section and 2- Section models are selected.



LESSON SIX: RUN A BATCH MODE SIMULATION

1. To run a simulation in Batch Mode, select:
Start > Run
2. Change to the directory where the XtractIM.exe file is located.

Upon completing the simulation, all output files (including .ckt, .bnp, and .csv files) are saved automatically in the same directory as the *.spd file.

Batch Mode Example

If you want to use the project (.spd file) defaulted in the workspace file (.xml file), enter:

```
XtractIM -b broadband "Full_path_to_My_xml_File\xml filename"
```

If you want to use a different project file other than the one in the .xml file, enter:

```
XtractIM -b -broadband "Full_path_to_My_xml_File\xm filename"  
"Full_Full_path_to_My_xml_File\new_spd filename"
```


RLGC and Optimal Broadband Module: Pin-Based Simulation

This chapter takes you through the steps to use the XtractIM tool in a pin-based simulation of single-die single-BGA or multi-die stacked-BGA packages. The steps for single-die single-BGA RLGC module are strengthened. Those for multi-die stacked-BGA or for Optimized Broadband module are straightforward.

PREPARE FOR THE SIMULATION

Collect this information before you begin the simulation.

- Make sure your files have been translated into SPD format.
- Have the Stackup information ready.
- Have Bump and Solderball diameters, length, heights and conductivity ready.

LESSON ONE: SIMULATION SETUP

Simulation Overview

A typical workflow in interaction mode is the same as net-base extraction.

A qualified net is the one which has at least one pin in each of the die- and BGA- circuits.

No open circuit exits for these pairs of pins.

Simulation Options

Pin-based extraction has four options in RLGC circuit extraction. The Simulation Setup options are located on the right side of the Editor bar.

- **Option 1** — In DIE or BGA circuit, choose one net as reference. This would lump all pins of the chosen net together as reference in both DIE and BGA side
- **Options 2 & 3** — In DIE or BGA circuit, choose one pin node as reference
Choose **auto**. XIM automatically selects a node of the net as reference. This node is generally in the center of the circuit
Choose **manual**. Specify a node as reference.
- **Option 4** — Mesh DIE or BGA circuit. Use one cell element as reference. Any net pins in a same cell are lumped together

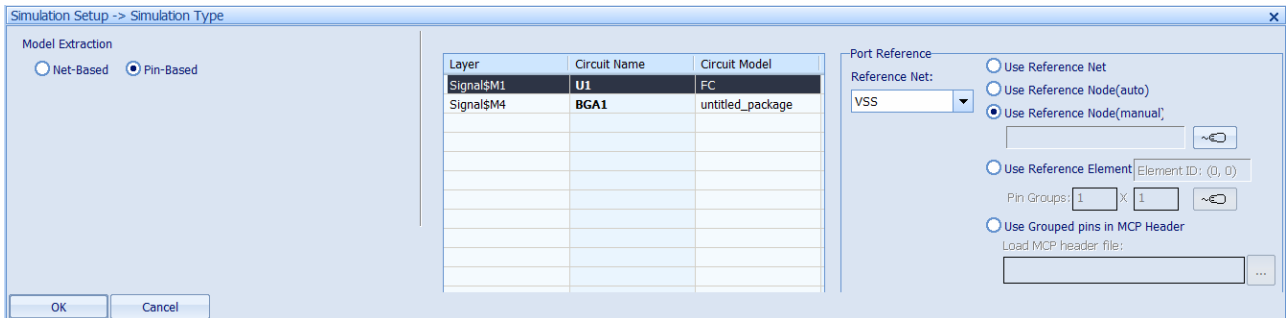
Setup Simulation Type

1. Click:
Simulation Type
2. Select:
Pin-Based
3. Click:
Reference Net

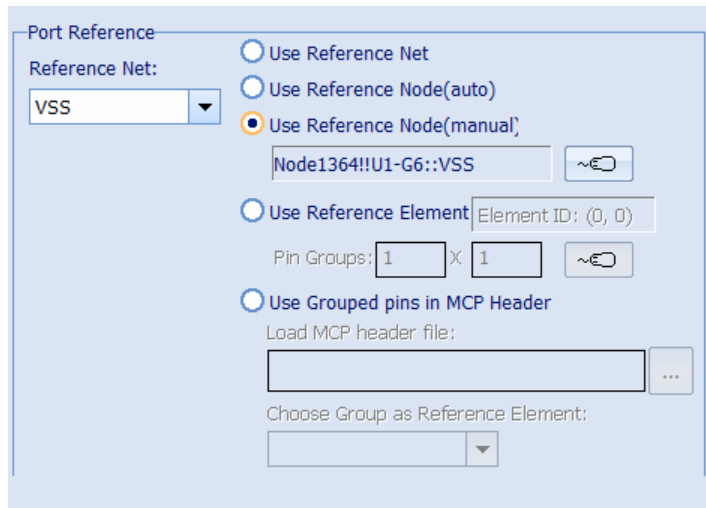
A drop-down menu opens. Qualified nets are displayed.
4. Select one net as the reference net for simulation.
5. Select a circuit from the **Circuit Name Element**.
6. Select one simulation type from the list of four.
 - Use Reference Element
 - Use Reference Net
 - Use Reference Node (auto)
 - Use Reference Node (manual)
7. If you select **Use Reference Net** or **Use Reference Node (auto)**, no further action is needed.
If you select **Use Reference Node (manual)** or **Use Reference Element**, perform the steps described in the following sections.
8. Repeat steps 5 & 6 for each circuit (DIE and BGA or DIES and BGAs for multi-die stacked BGA packages).
9. Click **OK** to save all the settings.
10. Click **Cancel** if you want to start over and enter new settings.

Select Reference Node (Manual)

1. Click:
Simulation Type
2. Select:
Pin-Based
3. Click:
Use Reference Node (manual)

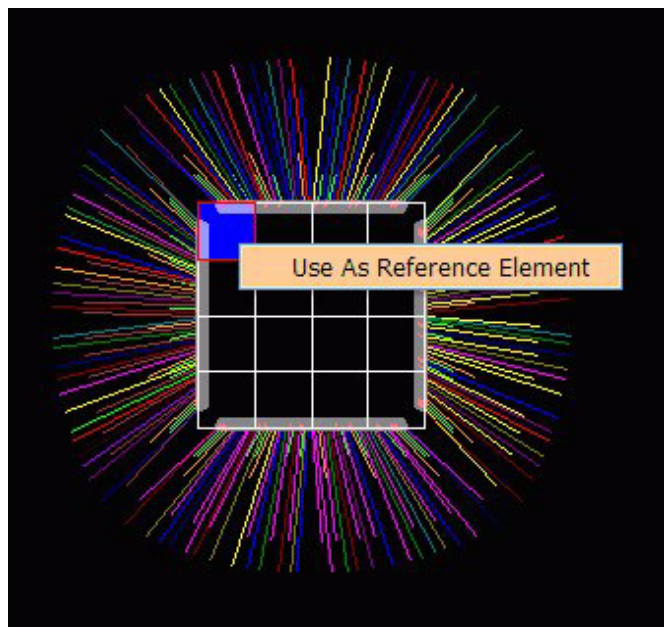


4. Click on the mouse icon.
5. In the **Layout View** window, select a **Reference Net Node**. The Node Name is displayed.



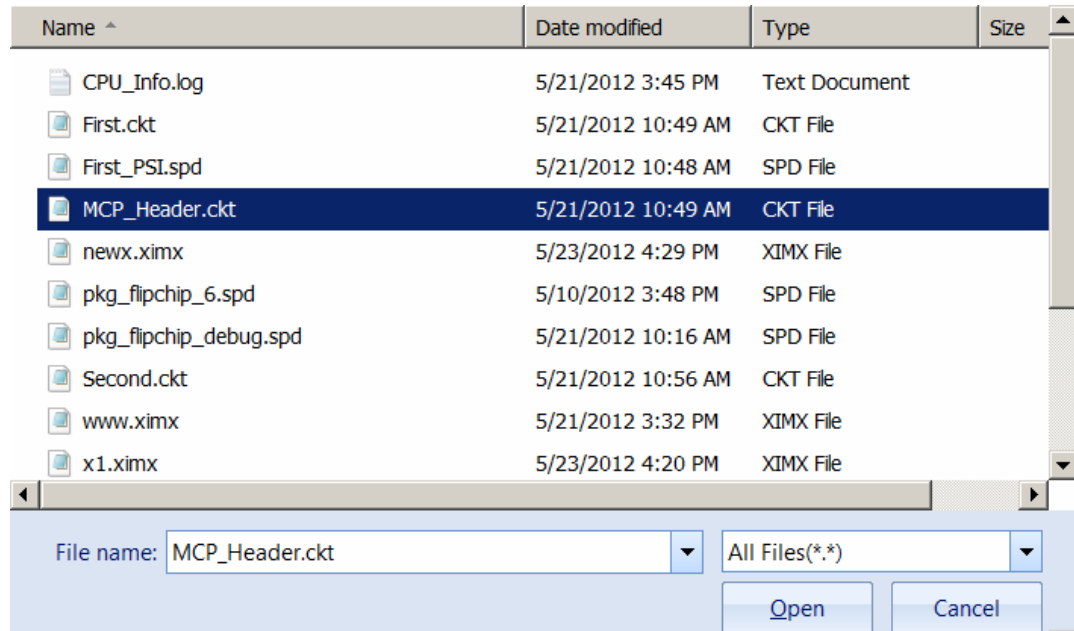
Select Reference Element

1. Select:
Use Reference Element
2. Choose:
Pin Groups
For example, 1*1, 2*4 or 5*5.
3. Click the mouse icon at the right side of Pin Groups.
4. In the Layer View window right-click to select a cell as the reference element. The selected cell becomes blue.
A message window appears
Use As Reference Element
5. Repeat these steps for other circuits (DIE or BGA)

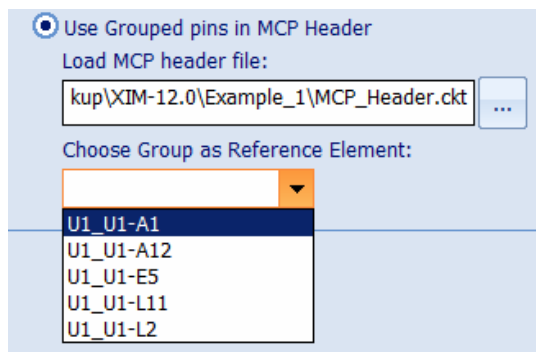


Select User Grouped Pins in MCP Header

1. To load the file with MCP Header, click  next to the **Load MCP header file** field.



2. Select the MCP Header file (which has the grouped pin information).
3. Click **Open**.
4. In the right side of the **Simulation Setup** -> **Simulation Type** pane, select a group as **Reference Element** from the drop-down list.



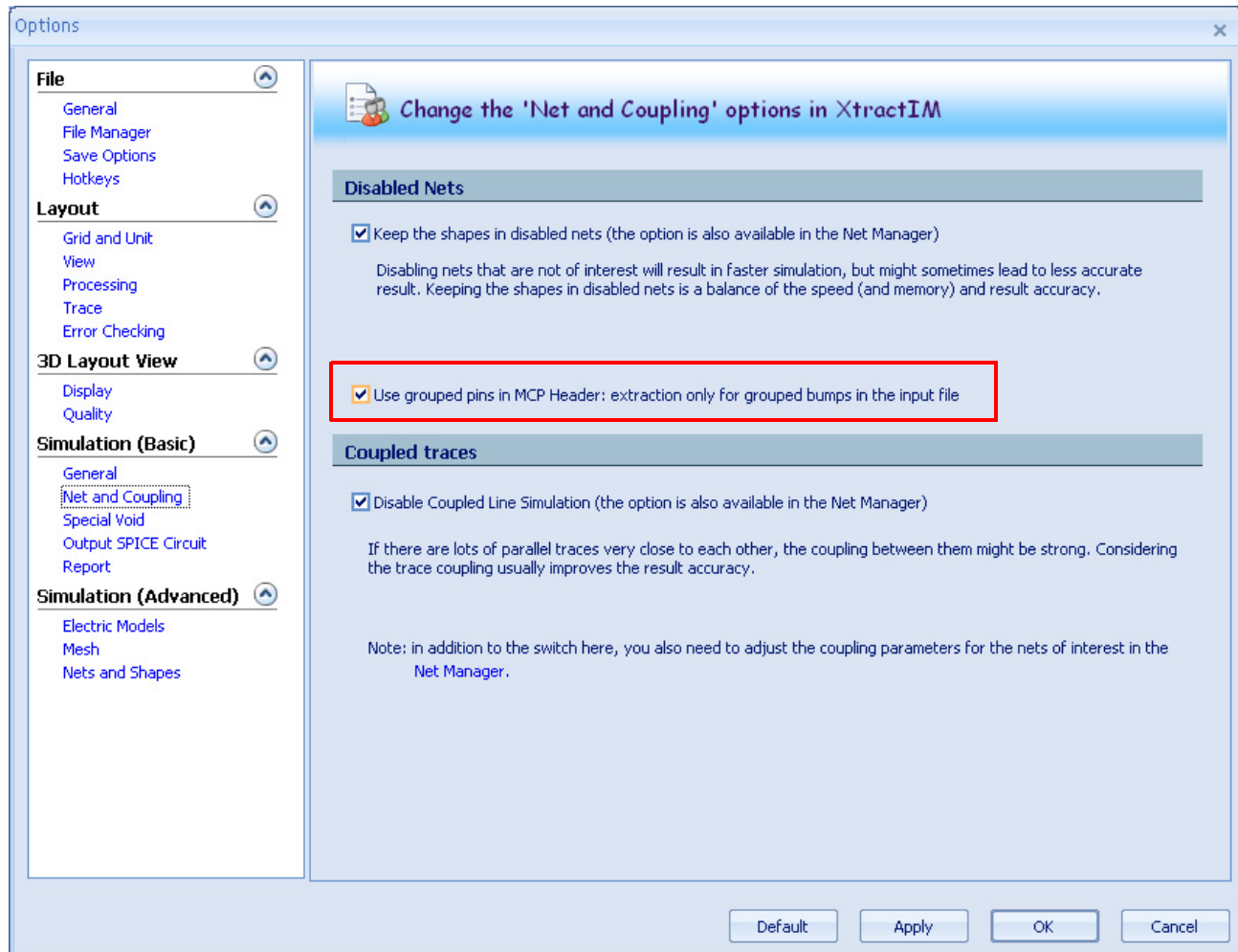
5. Click **OK**.

Reference Options

- **Use Reference Net** — Lumps all pin nodes of the Reference Net as port references
- **Use Reference Node (auto)** — Automatically selects a Pin Node of the Reference Net as the port reference; this Node is generally in the center of the circuit
- **Use Reference Node (manual)** — Uses a defined Pin Node for the Reference Net as the Port Reference; we recommend the user choose a Node in the center of the circuit
- **Use Reference Element** — Uses the lump of all the Reference Net Pins in the designed cell as the Port Reference
- **Use Grouped Pins in MCP Header** — Uses the lump of all the reference net pins in the designed group by MCP header as the Port Reference

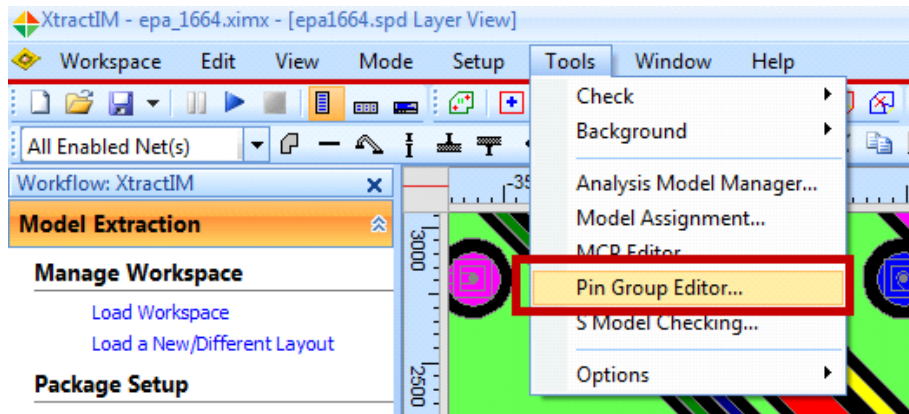
- 1) As always, extraction goes to those nets enabled in **Net Manager** only. If a net is included in the MCP Header but is disabled in **Net Manager**, it will not be extracted.
- 2) If an enabled net is not included in the MCP Header, during extraction, it will be considered as 1-cell by 1-cell lump model extraction.

If the user just wants to extract a model with bumps defined the in the MCP header (i.e. ignore those bumps not in the MCP Header), just select Tools > Options > Edit Options..., and in the **Options** window, click **Net and Couplings**, select the **Use grouped pins in MCP Header: extraction only for grouped bumps in the input file** check box, then click **OK**.



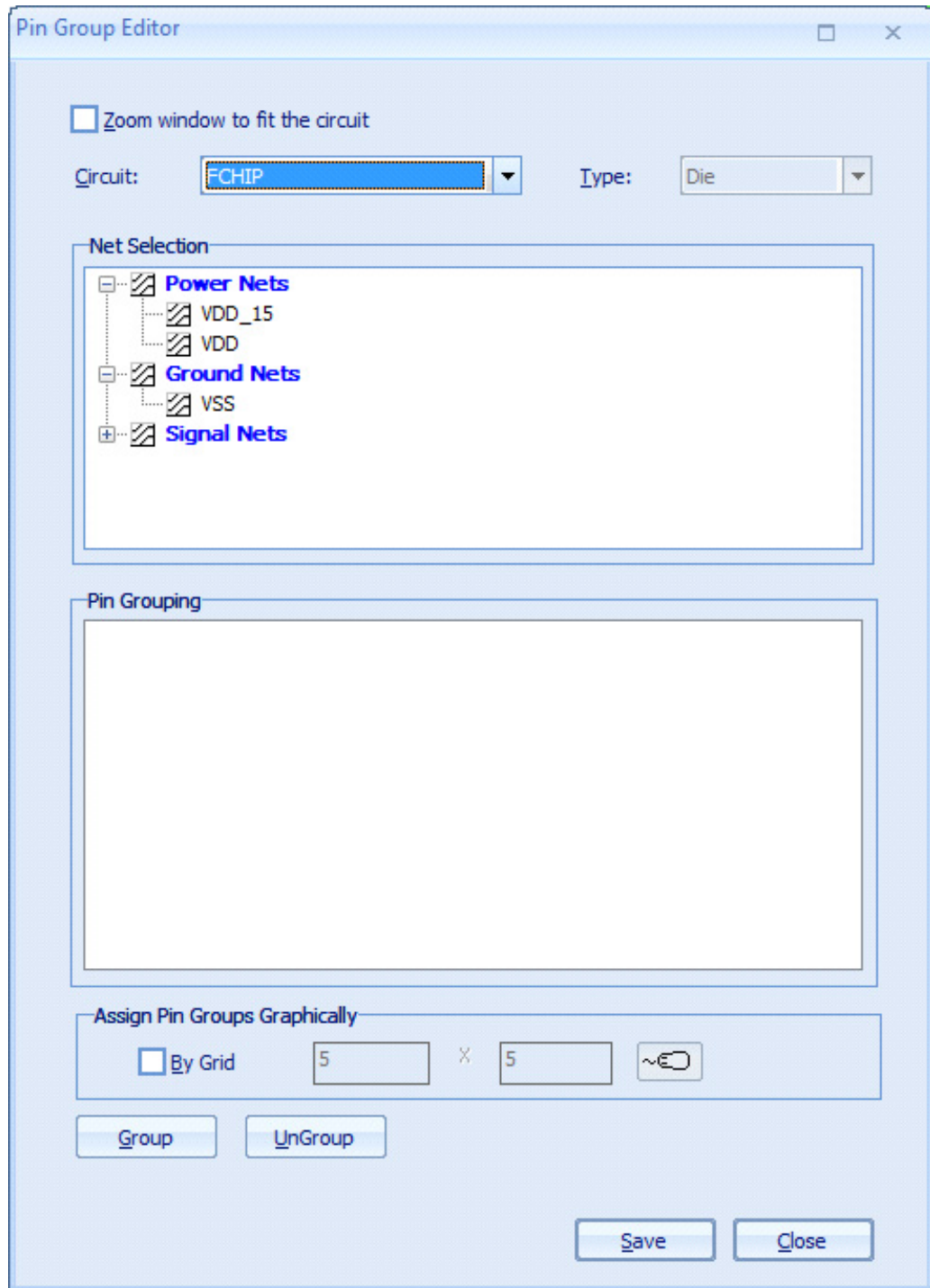
Generate MCP Header File

1. Choose Tools > Pin Group Editor...



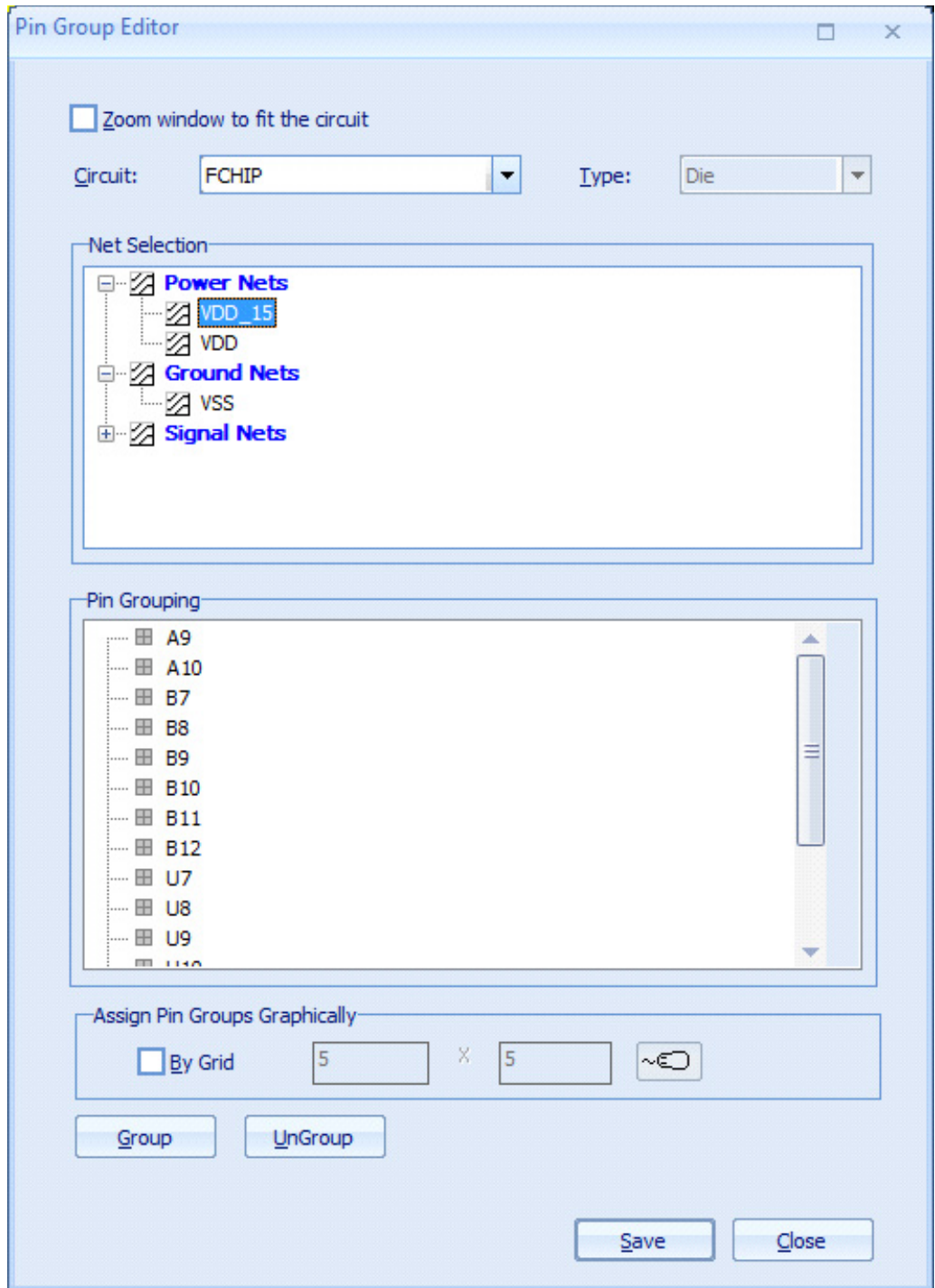
2. Choose an available circuit name from the **Circuit** pull-down list. For example, **FCHIP** in this tutorial.

All of the enabled nets related with this circuit are listed in the **Net Selection** field.

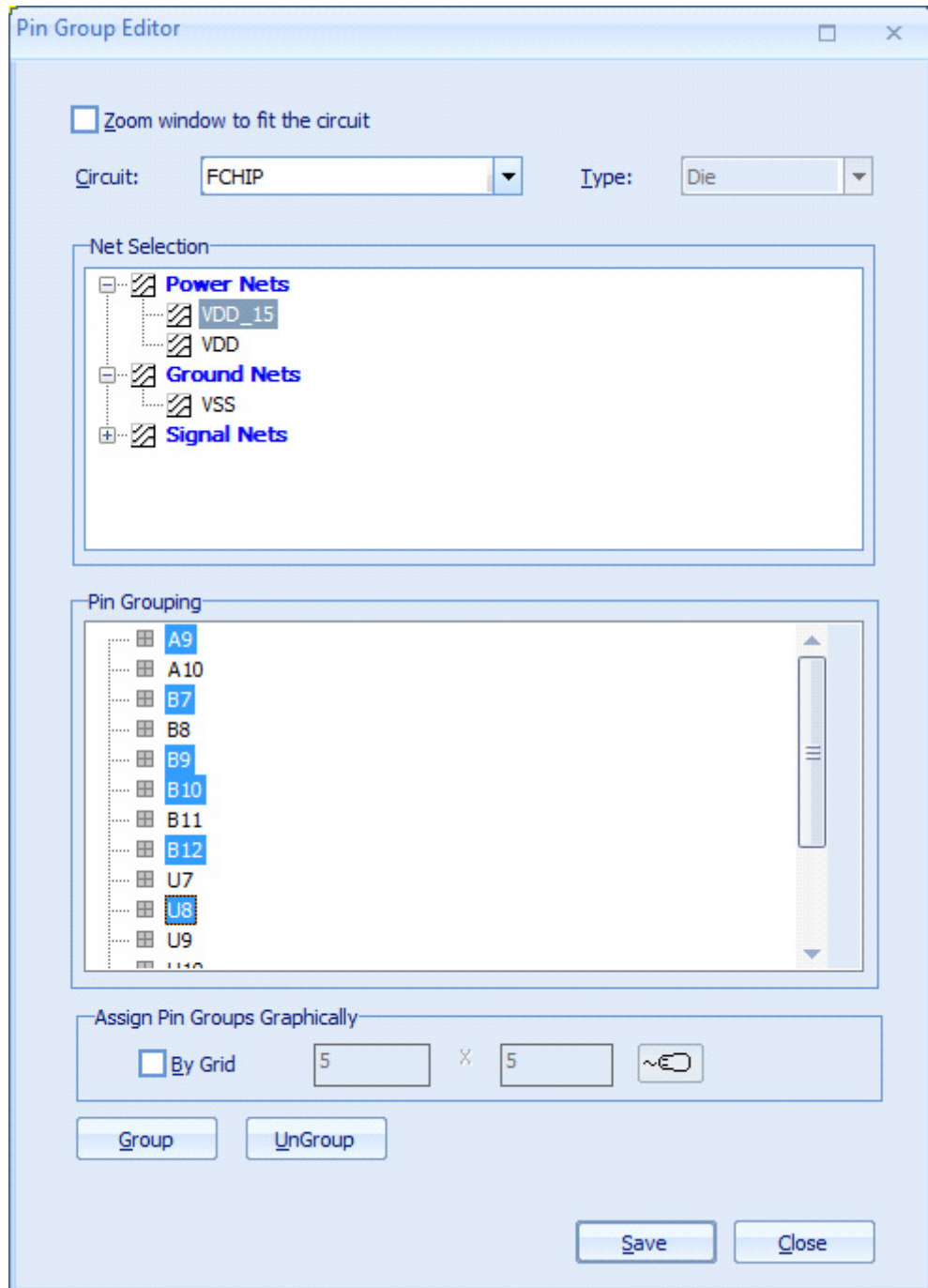


3. Choose a power or ground net to perform pin grouping. For example, **VDD_15** in this tutorial.

The corresponding pins for the selected net are listed in the **Pin Grouping** field.

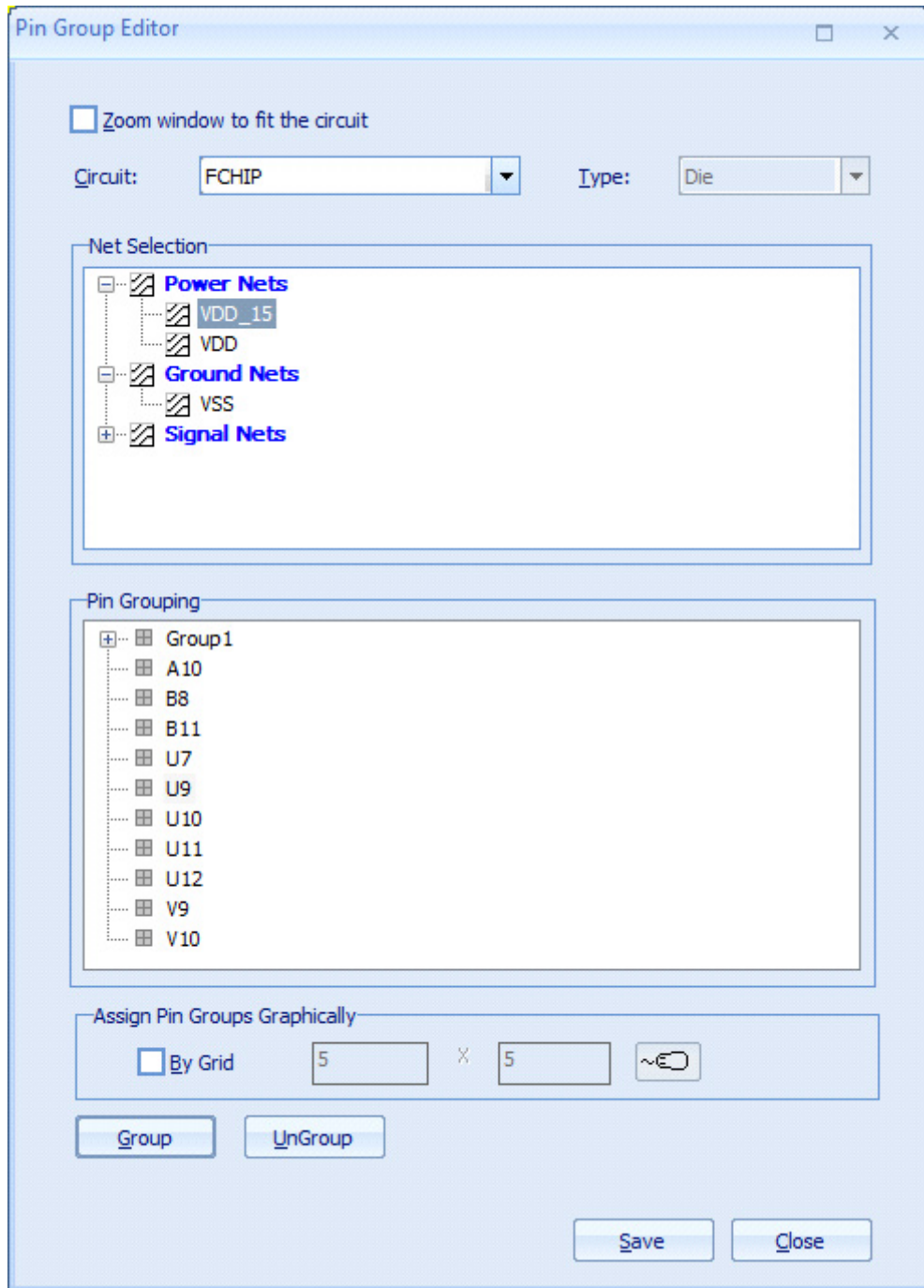


- Choose pins that you want to add in a group.

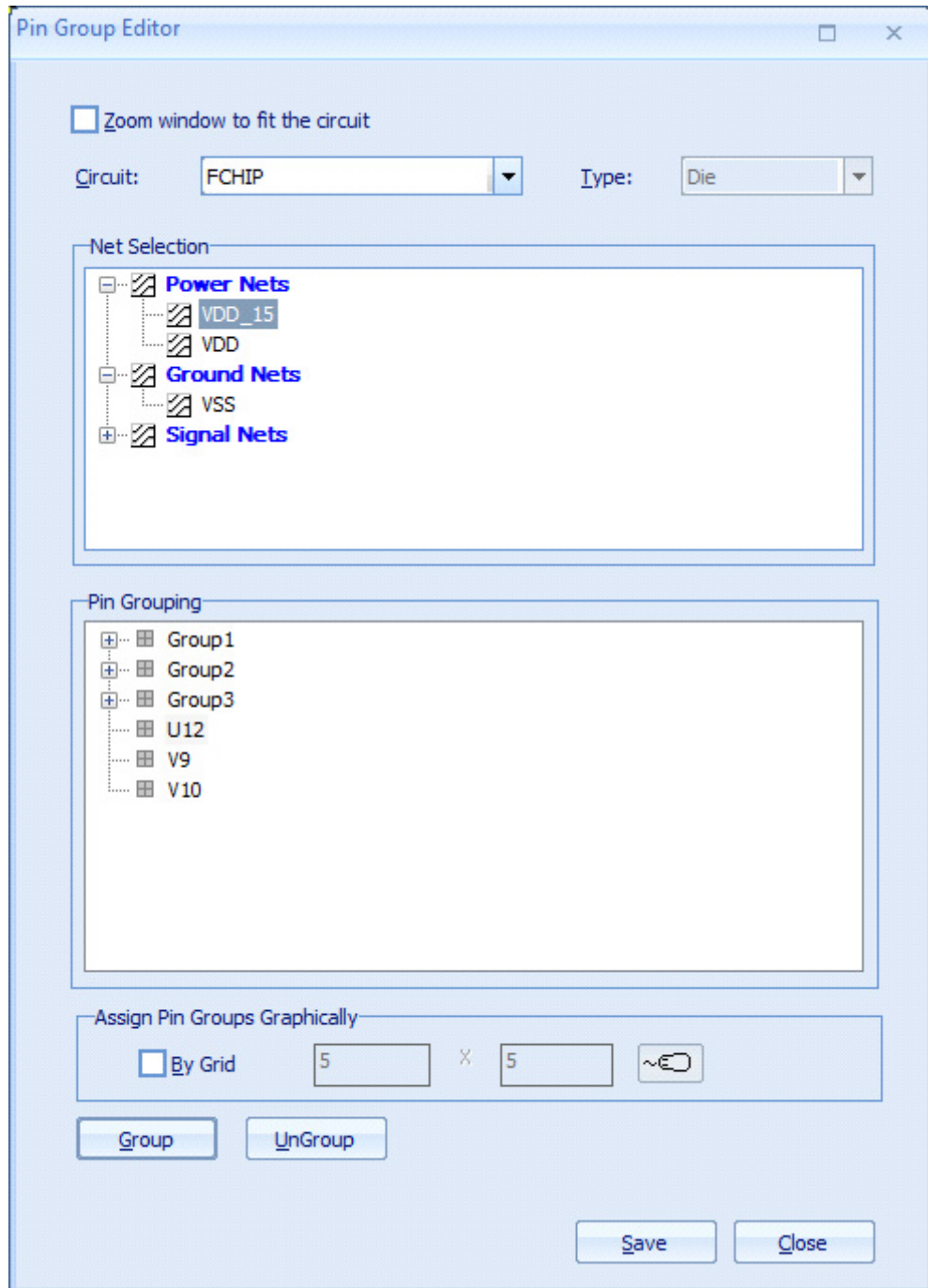


- Click the **Group** button.

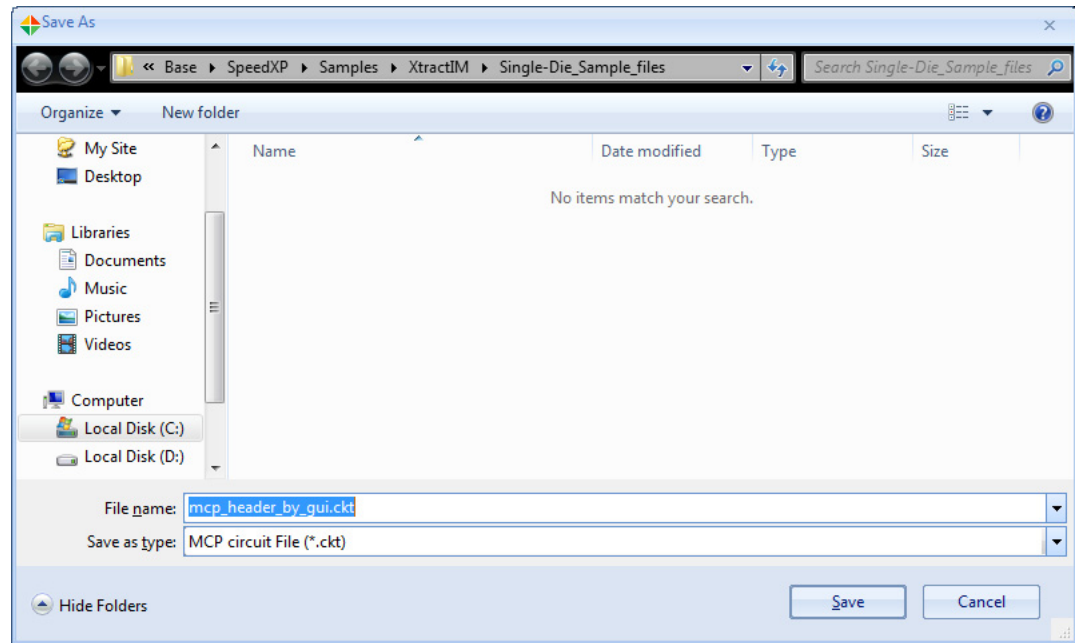
A group is generated as **Group1**.



- Repeat **Step 4** and **5** to generate multiple groups for a net.



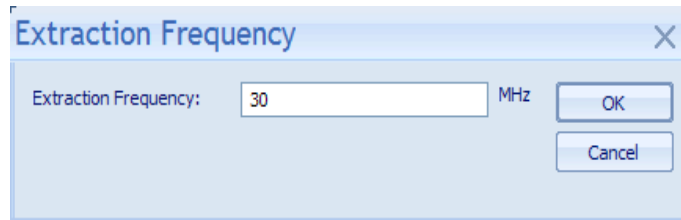
7. Once the pin groupings have been done for all circuits and nets, click the **Save** button to generate a MCP header file, for example **mcp_header_by_gui.ckt**.



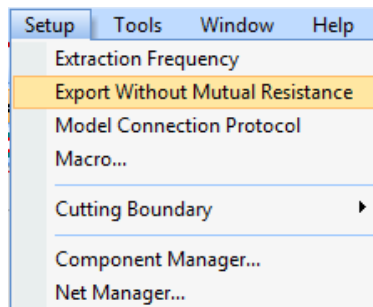
The .ckt file generated in the above steps can be used in the *Select User Grouped Pins in MCP Header* section.

Setup Extraction Frequency

1. Select:
Setup > Extraction Frequency
A pop-up window opens.
2. Update the data in the window.
3. Change the default value. The default value is 30MHz.



4. To ignore mutual resistance in RLGC circuits, select:
Setup > Export Without Mutual Resistance
The output circuit does not include the H-elements.



LESSON TWO: SAVE WORK AREAS

Layout File

1. Click on the Workspace.
2. Click on the **Open Layout File** icon (**green**) to open the project file.
3. Use **Save As** to save the layout file under a different name.

NOTE!

Saving the workspace automatically saves the .spd file.
Saving the.spd file does not automatically save the workspace.


Workspace

1. Click on the Workspace. The Workspace pane opens.
2. View the Workspace toolbar.
3. In the toolbar click
Save Workspace
4. To save the Workspace under a different name, use:
Save As

Open Workspace



LESSON THREE: RUN THE SIMULATION

1. Click on the **Play** button  at the top of the window to start the extraction (simulation).
2. XtractIM only extracts RLCG for a net which has at least one pin at the Die side and at least one pin at the board side.
3. At the beginning of the simulation, if some nets have Die-Board mis-match, a pop-up window opens. Select the next action.
 - **Continue** — Continue the simulation
 - **More Information** — Examine what nets are mis-matched
 - **Stop** — Cancel the simulation

Investigate Mis-matched Nets

The **More Information** window lists all the mis-matched nets.

Investigate the mis-matched nets to see whether it is a special design or a defective design. Decide whether or not to proceed with the simulation.

Choose **Continue**, **Stop** or **More Information**. If 30 seconds pass and the user has not made a choice; then, by default, the simulation continues.

LESSON FOUR: FLY-WIREBOND PACKAGE MODEL EXTRACTION

Introduction

For some wirebond package designs, there are wire connections only among die pads for power and ground nets. These die pads don't have connection to bond fingers or to package pins. Such kind of package is usually named as package with fly-wirebond or jump-wirebond inside. The fly-wirebond is typically used to reduce power IR drop noise.

In this lesson, it is introduced how to get a package model with fly-wirebonds in XtractIM.

Workflow

In general, the fly-wirebonds only happen on the same die in a package. It is only supported in single-die/single-package designs flow. The package type can be either BGA or lead-frame.

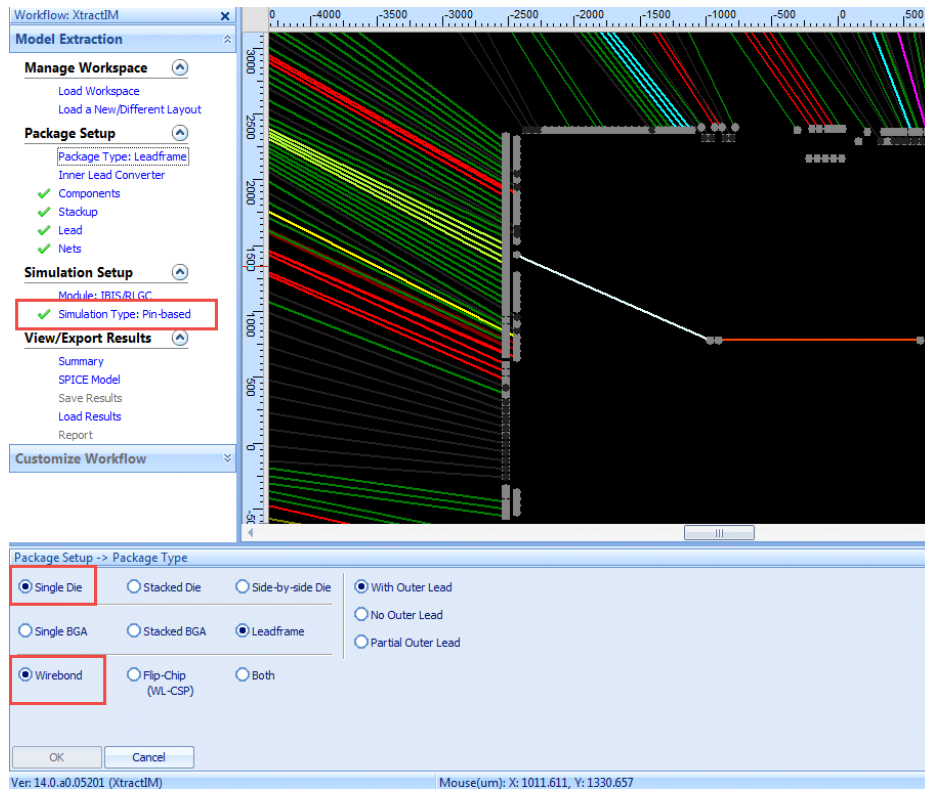
1. Package Setup:
 - a. Select **Single Die**.
 - b. Select **Single BGA** or **Leadframe**.
 - c. Select **Wirebond**.

2. Simulation Setup:

The fly-wirebond is only supported in the pin-based mode.

- a. Select simulation type: **Pin-Based**.

No specific setting is needed.



Result

The fly-wirebonds are modeled separately by the tool.

The fly-wirebond model is wrapped into SPICE subcircuit model named

jobname_PinBaseSPICE.ckt as shown below.

The screenshot shows the XtractIM software interface. The 'View/Export Results' menu is highlighted with a red box, and the 'SPICE Model' option is circled in green. The 'Extractor Result' window displays a list of component values, with a red box highlighting the 'fly-bondwire model' section.

Extractor Result

```

C49_52 CGN_49 CGN_52 1.91063e-014
RG49_52 CGN_49 CGN_52 1.28543e+008
C49_53 CGN_49 CGN_53 1.45915e-014
RG49_53 CGN_49 CGN_53 4.02207e+006
C49_54 CGN_49 CGN_54 7.68331e-014
C50_51 CGN_50 CGN_51 3.56452e-013
RG50_51 CGN_50 CGN_51 2.37823e+006
C50_52 CGN_50 CGN_52 7.09426e-014
RG50_52 CGN_50 CGN_52 3.45591e+007
C50_53 CGN_50 CGN_53 2.22214e-014
RG50_53 CGN_50 CGN_53 6.74714e+007
C50_54 CGN_50 CGN_54 5.08063e-014
C51_52 CGN_51 CGN_52 3.44473e-013
RG51_52 CGN_51 CGN_52 2.3082e+006
C51_53 CGN_51 CGN_53 7.56783e-014
RG51_53 CGN_51 CGN_53 4.01902e+006
C51_54 CGN_51 CGN_54 6.62728e-014
C52_53 CGN_52 CGN_53 4.23178e-013
RG52_53 CGN_52 CGN_53 1.19122e+006
C52_54 CGN_52 CGN_54 4.48427e-014
C53_54 CGN_53 CGN_54 9.14919e-014

Rfb1_1 U1_48 NFB_RL1_1 0.0858952
Lfb1_1 NFB_RL1_1 NFB_Mid_1 7.4464e-010
Rfb2_1 NFB_Mid_1 NFB_RL2_1 0.0858952
Lfb2_1 NFB_RL2_1 U1_24 7.4464e-010
Rfb1_2 U1_460 NFB_RL1_2 0.0827256
Lfb1_2 NFB_RL1_2 NFB_Mid_2 7.14764e-010
Rfb2_2 NFB_Mid_2 NFB_RL2_2 0.0827256
Lfb2_2 NFB_RL2_2 U1_47 7.14764e-010
KFB11_2 Lfb1_1 Lfb1_2 -0.00484792
KFB21_2 Lfb2_1 Lfb2_2 -0.00484792
Cfb0_1 NFB_Mid_1 Node_GND 1.56779e-013
Cfb0_2 NFB_Mid_2 Node_GND 1.51047e-013
CFB11_2 NFB_Mid_1 NFB_Mid_2 3.36799e-015

```

fly-bondwire model

VIEW EXPORT RESULTS

The **View / Exports Results** options are displayed on the left side of the window.

1. Click on **Summary**.
2. View the maximum and minimum R, L, C, and other information in the Summary.
3. Click on **SPICE Model**. The SPICE Model name *.ckt is loaded.
4. View the SPICE Model file.

The screenshot shows the XtractIM software interface. The left sidebar contains the following sections:

- Manage Workspace**
 - Load Workspace
 - Load a New/Different Layout
- Package Setup**
 - Package Type: Wirebond
 - Circuits
 - Stackup
 - Solder Ball
 - Nets
- Simulation Setup**
 - Module: IBIS/RLGC
 - Simulation Type: PinBased
 - Set Reference Net
- View/Export Results**
 - Summary
 - SPICE Model

The main window, titled 'Extractor Result', displays the following data:

```

* 3 BGA1-U26 VSS
* 3 BGA1-U27 VSS
* 3 BGA1-U3 VSS
* 3 BGA1-V1 VSS
* 3 BGA1-V2 VSS
* 3 BGA1-V27 VSS
* 3 BGA1-V28 VSS
* 3 BGA1-W2 VSS
* 3 BGA1-W26 VSS
* 3 BGA1-W27 VSS
* 3 BGA1-W3 VSS
* 3 BGA1-Y1 VSS
* 3 BGA1-Y2 VSS
* 3 BGA1-Y26 VSS
* 3 BGA1-Y27 VSS
* 3 BGA1-Y28 VSS
* 3 BGA1-Y3 VSS
* Ref U1-154 BGA1-P14
*
RD1 U1-112 DrN1 0.119433
VD1 DrN1 DVn1 0
Hd1_2 DVn1 CCVSr1_2 CCVS VD2 0.0390498
Hd1_3 CCVSr1_2 CCVSr1_3 CCVS VD3 0.037191
Hd1_4 CCVSr1_3 CCVSr1_4 CCVS VD4 0.0364626
Hd1_5 CCVSr1_4 CCVSr1_5 CCVS VD5 0.0360892
Hd1_6 CCVSr1_5 CCVSr1_6 CCVS VD6 0.0359549
Hd1_7 CCVSr1_6 CCVSr1_7 CCVS VD7 0.0359489
Hd1_8 CCVSr1_7 CCVSr1_8 CCVS VD8 0.0358705
Hd1_9 CCVSr1_8 CCVSr1_9 CCVS VD9 0.0357969
Hd1_10 CCVSr1_9 CCVSr1_10 CCVS VD10 0.0356331
Hd1_11 CCVSr1_10 CCVSr1_11 CCVS VD11 0.0362686
Hd1_12 CCVSr1_11 CCVSr1_12 CCVS VD12 0.0356264
Hd1_13 CCVSr1_12 CCVSr1_13 CCVS VD13 0.0357708
Hd1_14 CCVSr1_13 CCVSr1_14 CCVS VD14 0.0358375
Hd1_15 CCVSr1_14 CCVSr1_15 CCVS VD15 0.0358785
Hd1_16 CCVSr1_15 CCVSr1_16 CCVS VD16 0.0358522
Hd1_17 CCVSr1_16 CCVSr1_17 CCVS VD17 0.0369935
Hd1_18 CCVSr1_17 CCVSr1_18 CCVS VD18 0.035952
Hd1_19 CCVSr1_18 CCVSr1_19 CCVS VD19 0.0379053
Hd1_20 CCVSr1_19 CCVSr1_20 CCVS VD20 0.0408726
Hd1_21 CCVSr1_20 CCVSr1_21 CCVS VD21 0.0362841

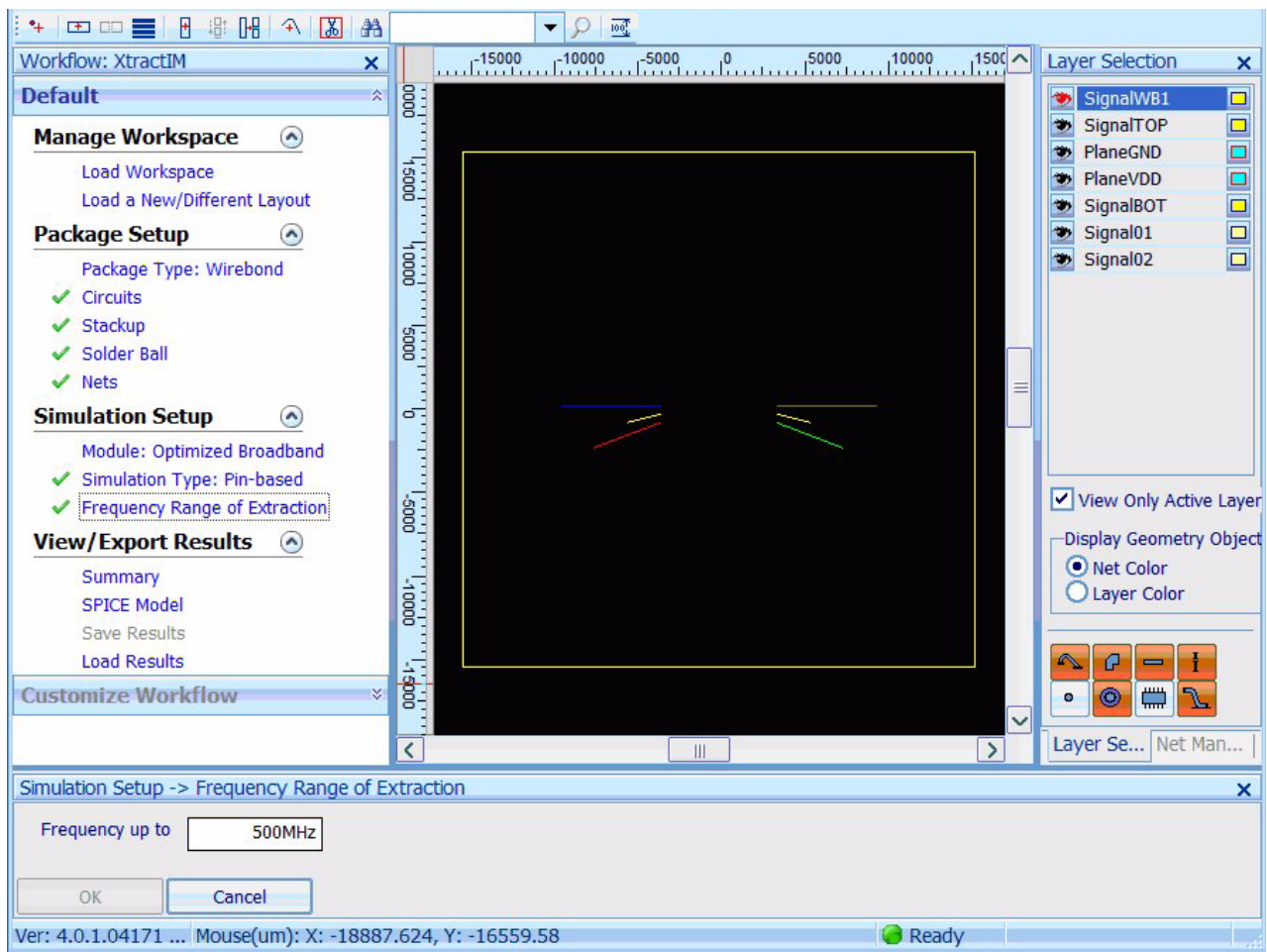
```

The status bar at the bottom indicates: Mouse(mm): X: -23.750, Y: 10.885 and Computing completed.

Optimized Broadband Module

A typical workflow in Iteration Mode is the same as RLGC Module Pin-based Extraction. Additional steps in the Simulation Setup include:

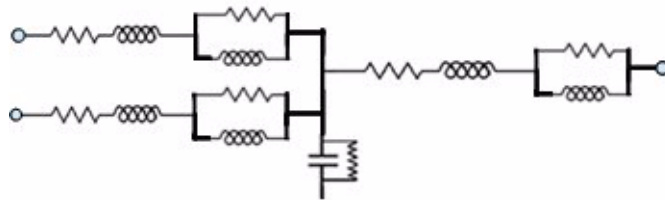
1. Click:
Module > Optimized Broadband
2. Click:
Workspace > Frequency Range of Extraction
A new Edit pane opens at the bottom of the window.
3. Input the highest frequency for simulation.



Circuit Topology

The circuit topology is a generalized T-model with series terms. No multi-sections circuit model is used as those in a net-based Broadband module.

Extraction frequency points for S-parameters are limited to a few points. Frequency band goes up to a few hundred MHz.



IBIS/RLGC Module: Simulation of Leadframe Package

This chapter takes you through the steps to use the XtractIM tool in the simulation of Leadframe package.

PREPARE FOR SIMULATION

Collect this information before you begin the simulation.

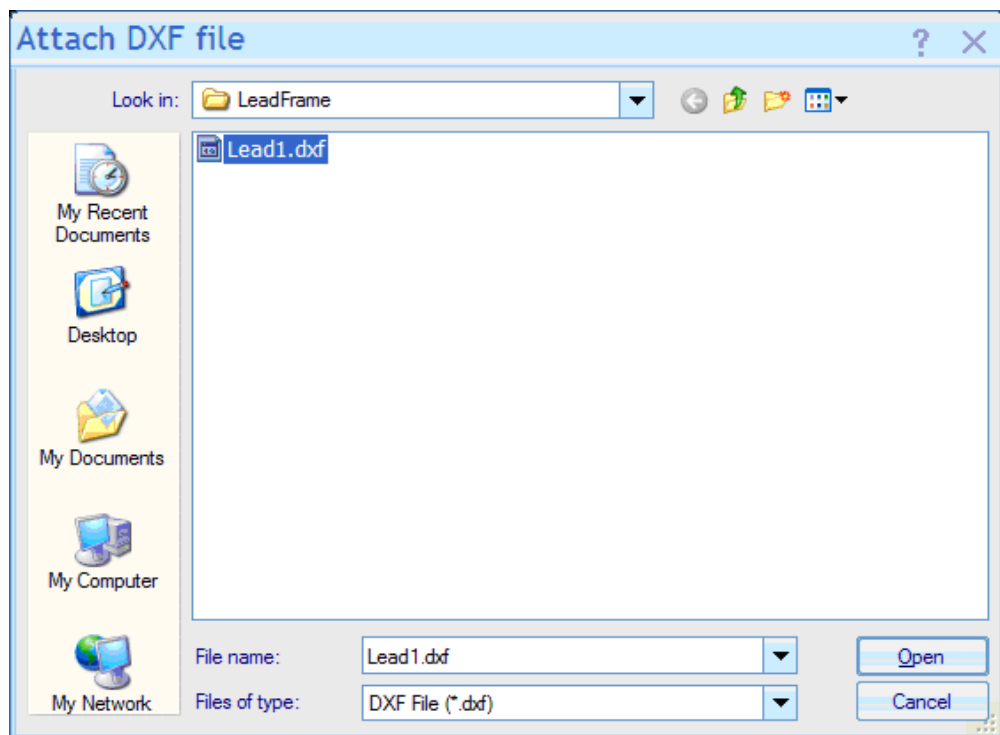
- Make sure the Leadframe file is in DXF or SPD format
- Have the Stackup information ready
- Have the outer lead width, length, height and conductivity ready

If the leadframe file is in DXF format, make note of:

- Ball pad parameters
- Die pads
- Layers you wish to import
- Leadframe conductor Wirebonds

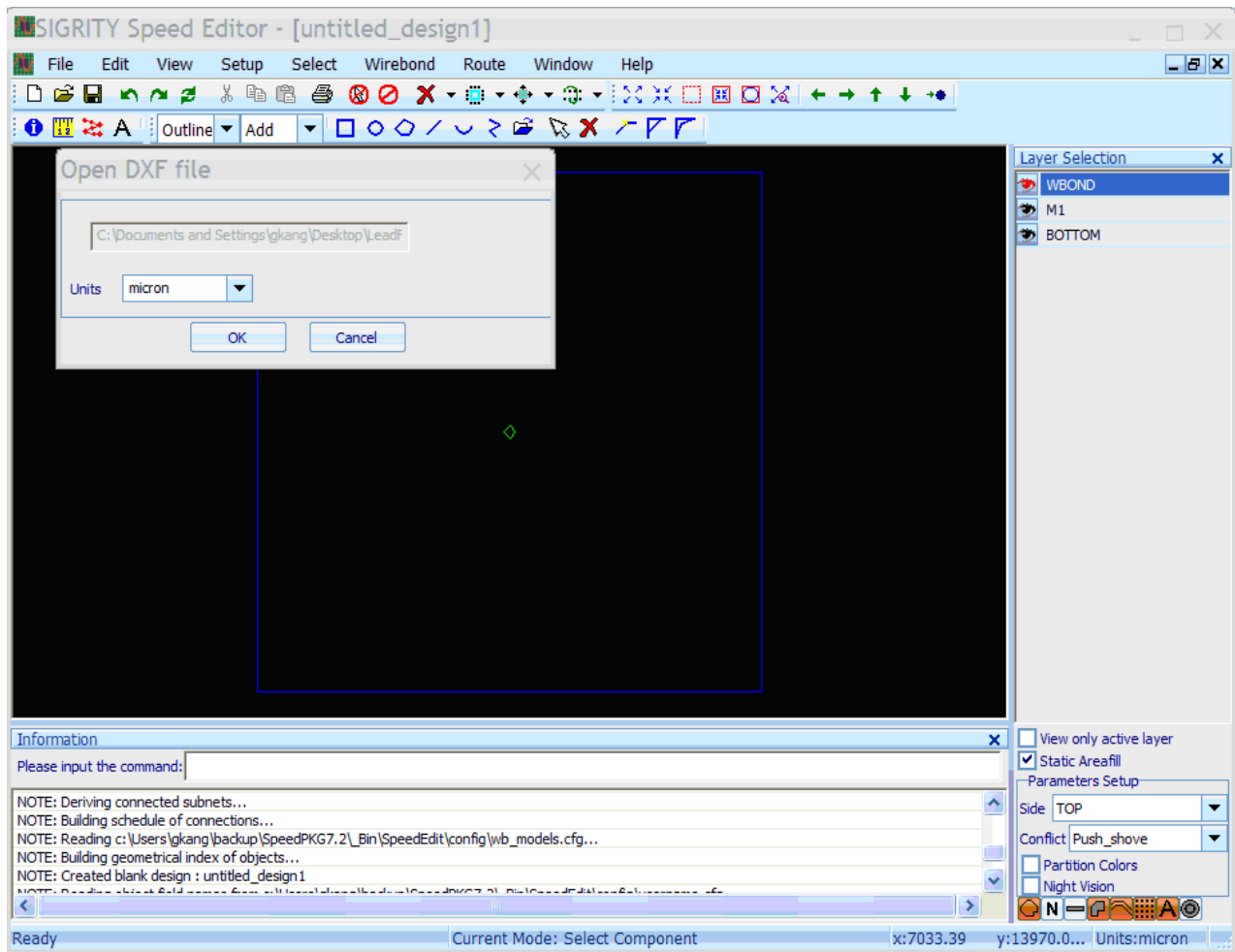
LESSON ONE : SIMULATION SETUP

1. Launch XtractIM.
2. Click **Open** to open an existing workspace.
3. Click:
Load an existing layout
4. Click **OK**.
The **Attach DXF File** window opens.
5. Select the desired file. The example shows only one file selected: **Lead1.dxf**.
6. Click **Open**.

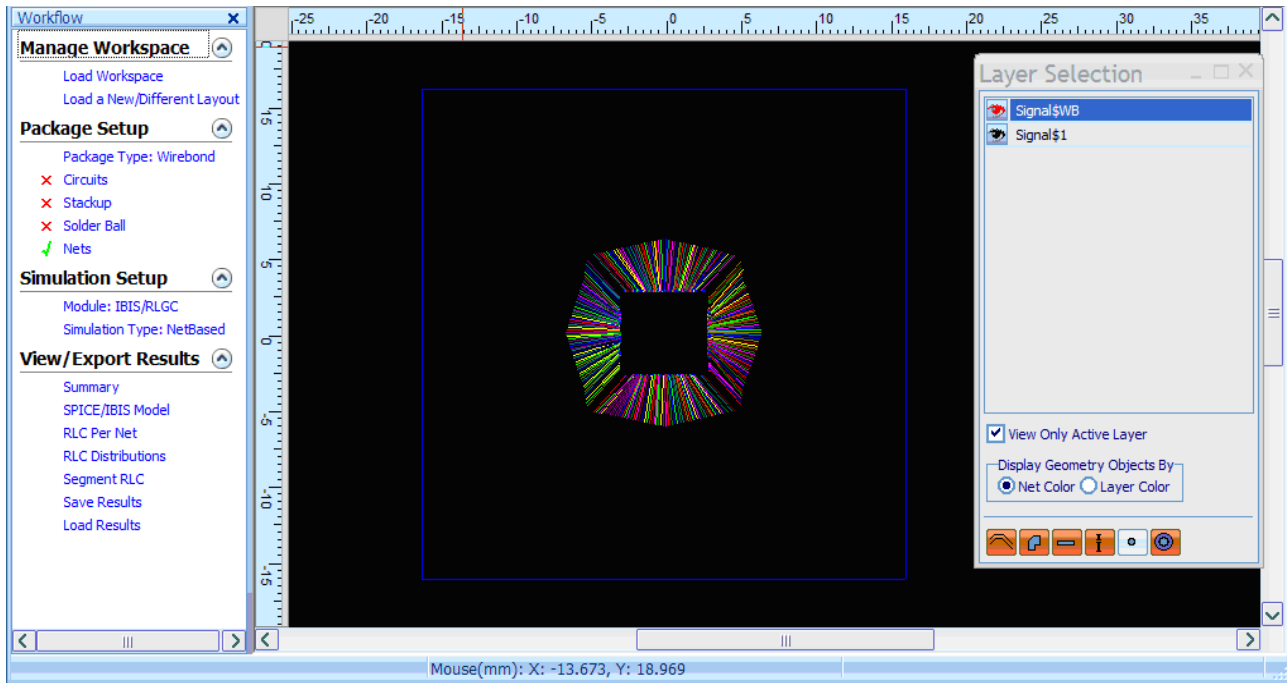


7. Launch XtractIM.
8. Click **New** to create a new workspace;
or select:
Workspace -> New
9. To load the Package Structure, select:
Load a New / Different Layout

10. Click **OK** to load a **DXF file**. The Sigrity Speed Editor is launched.



11. Translate a package file from DXF to SPD format; it is automatically loaded into XtractIM



Package Type

XtractIM classifies the leadframe family package into three kinds of packages:

- **No Outer Lead** — No board pin has outer lead. Typical package is QFN
- **Partial Outer Lead** — Some of the board pins have outer lead
- **With Outer Lead** — Every board pin has outer lead. Typical package is QFP

1. Select **Package Type**.

The default is Single-Die, Single-BGA, Wirebond Package.

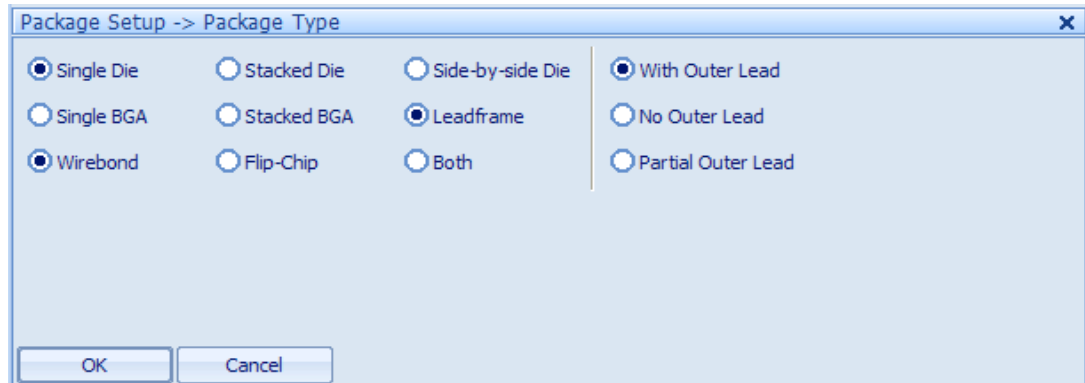
2. Click **Leadframe**.

3. Select one of:

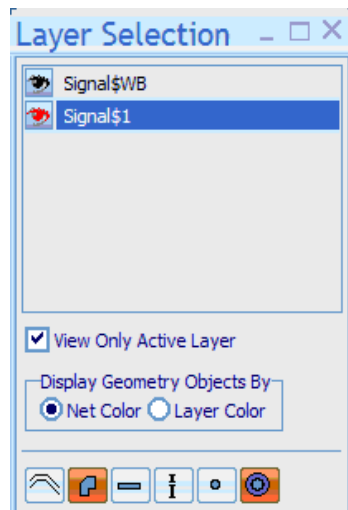
- No Outer Lead
- Partial Outer Lead
- With Outer Lead

4. Click **OK** to save your selection.

5. Click **Cancel** if you want to change your selection, start over, or cancel your session.

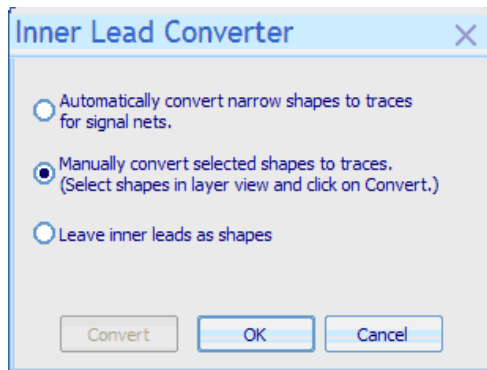


6. Click on the **Single\$1** layer. The **Inner Lead Converter** locates **Single\$1**.

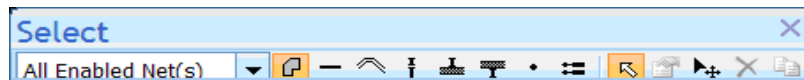


Shape to Trace Conversion

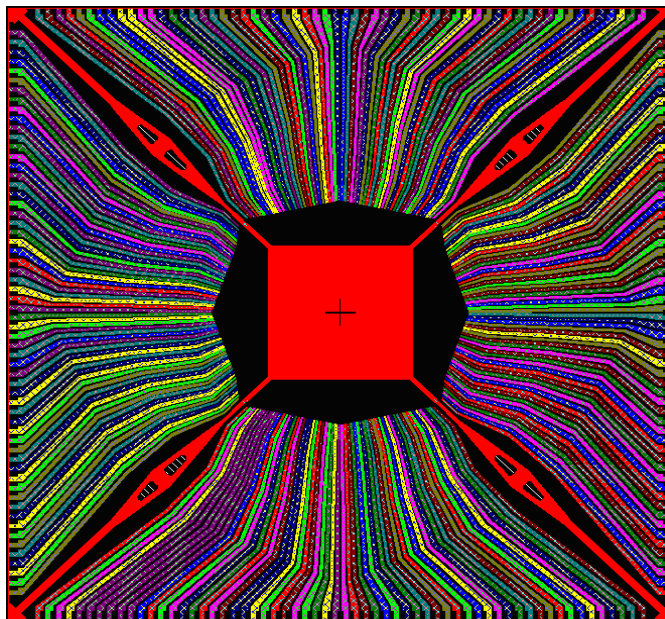
1. Click on **Inner Lead Converter** to convert narrow shapes into traces. The **Inner Lead Converter** window opens.
2. Choose:
Manually convert selected shapes to traces



3. Use the toolbar icon to select shapes in the Layer View.



4. Click **Convert**. All narrow shapes are converted into Traces.



NOTE!

A No Outer Lead Package generally does not need this converter.

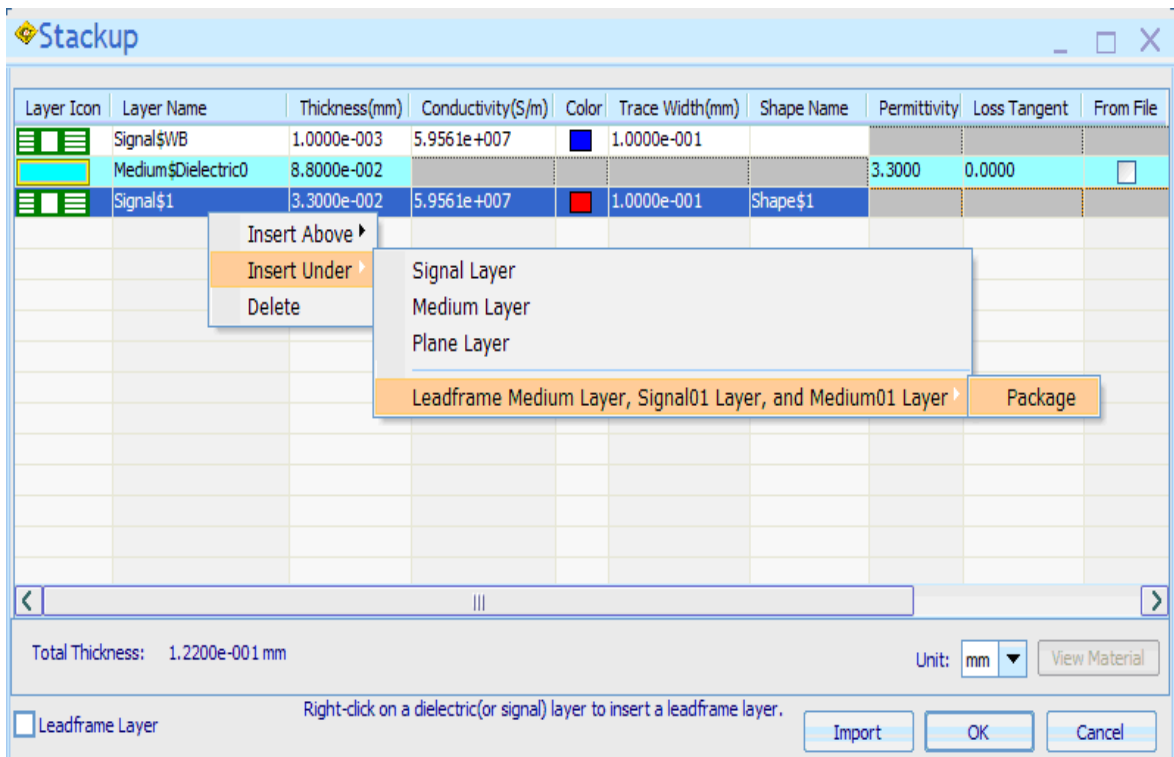
Setup Circuits and Stackup

1. Click on **Circuits** in the Workflow pane to setup circuit data for the leadframe package. A new pane opens in the left side of the workspace.
2. Right-click on the desired circuits.
3. Select it as a **Die circuit**.
4. Click **Next**.
5. Right-click on another desired circuit. Select it as a **Board circuit**.
6. Click **Finish** to finish the circuits setup.
7. Click on **Stackup**. The Stackup window opens.
8. Right-click on the **Signal\$** layer. A pop-up window opens.
9. Select:
 - Insert Under
 A second pop-up menu opens.

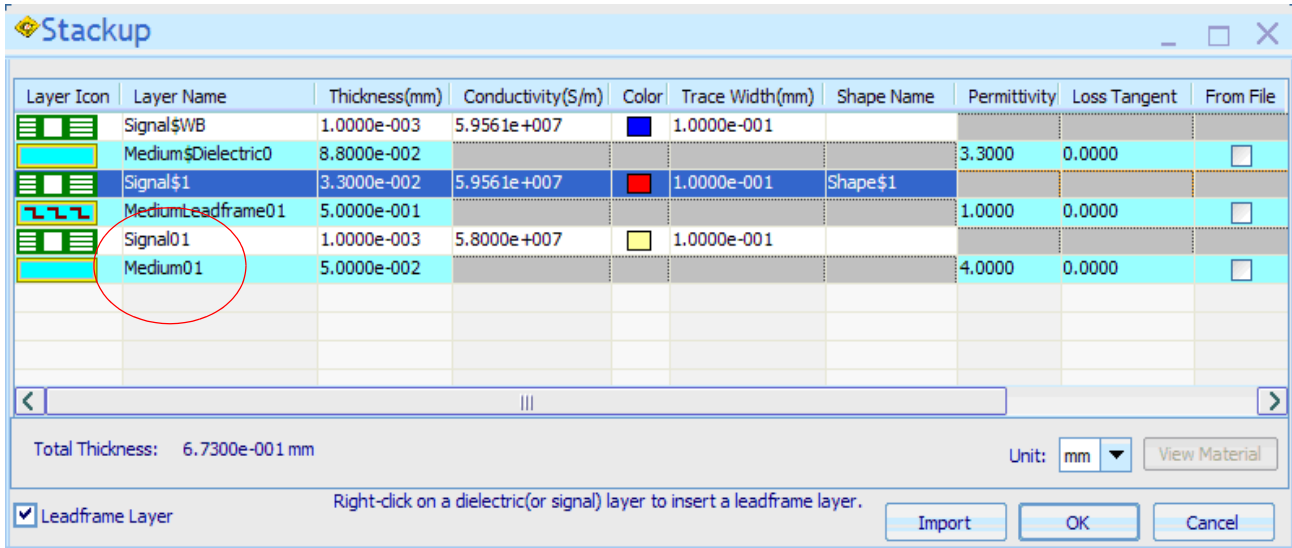
Outer Lead Setup

The following steps are performed for **Outer Lead** only.

1. To insert a Leadframe layer, select
Leadframe Medium Layer, Signal01 Layer, and Medium01 Layer
2. To insert an empty signal layer, select **Package**.



3. Insert a medium layer standing for a PCB medium layer.
4. All layers are inserted into **Signal\$1**. The added signal layer is located at the end of the lead-frame.
5. Click **OK** to close the Stackup window.



Leadframe Data for the Leadframe Package

1. Click on **Leadframe** in the Workflow pane to setup the data for the Leadframe package. A new pane opens up in the bottom portion of the windows.
2. Select:
 - Package Setup -> Leadframe
3. Input the settings for Leadframe (Standard Setup).
 - **Conductivity** — Conductivity of the outer leads
 - **D** — Total horizontal length
 - **H** — Heights of the leads
 - **Hs** — Heights of the lower part
 - **LI** — Length of lower leads
 - **Lu** — Length of upper leads
 - **Medium** — PCB medium thickness
 - **RI** — Radius of lower arc
 - **Ru** — Radius of upper arc
 - **T** — Thickness of the leads
 - **WI** — Width of lower leads
 - **Wu** — Width of upper leads

Standard Setup Example

Package Setup -> Lead

Simplified Setup Standard Setup

Layer Name	Circuit Name	D (mm)	Lu (mm)	Wu (mm)	Ru (mm)	Ll (mm)	Wl (mm)	Rl (mm)	T (mm)	H (mm)	Hs (mm)	Material	Conductivity (S/m)	Medium Thickness (mm)
Mediu...	Package	1	0.5	0.24	0	0.5	0.24	0	0.033	0.5	0	aluminum	5.8e7	0.05

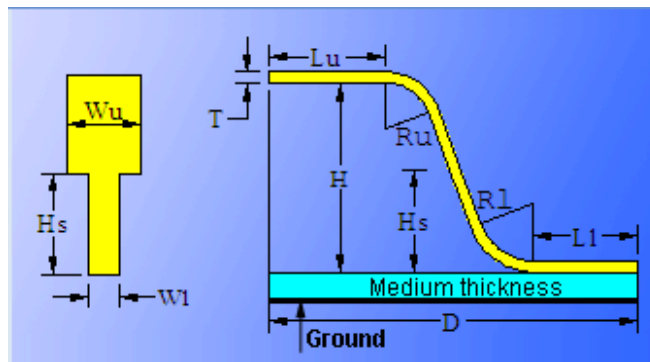
Simplified Setup Example

Package Setup -> Lead

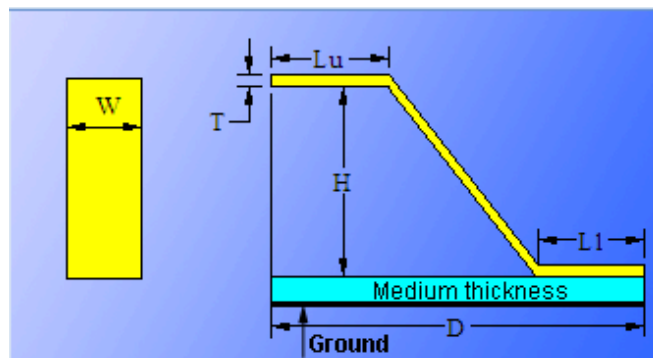
Simplified Setup Standard Setup

Layer Name	Circuit Name	D (mm)	Lu (mm)	W (mm)	Ll (mm)	T (mm)	H (mm)	Material	Conductivity (S/m)	Medium Thickness (mm)
Mediu...	Package	1	0.5	0.24	0.5	0.033	0.5	aluminum	5.8e7	0.05

Standard Lead Plot Example



Simplified Lead Plot Example



4. Click **OK** to save your entries.
5. Click **Cancel** if you do not want to save your changes. You can start over.

Setup Nets

1. Click on **Nets** in the workflow window. The **Net Manager** window opens.
2. Choose any desired nets for RLC extraction.
3. Move the **signal net** into and out of PowerNets and Ground Nets, as needed.
At least one Ground Net must be selected to act as a **reference ground net**.
4. Choose only the desired **Ground Net** as the reference ground net.

Extraction Frequency

1. To change the extraction frequency, select:
Setup -> Frequency of Extraction
A pop-up window opens.
2. Update the data in the pop-up window.
3. Use the Extraction Frequency window to change the default value. The default value is 30MHz.

Threshold for Exporting Mutual Terms

1. Use the XtractIM options to reduce the size of the output circuit during the export stage. XtractIM captures all the coupling during the extraction stage.
2. Open:
Setup > Threshold for Exporting Coupling Terms
A pop-up window opens.
3. Choose the number of strongest coupling neighbors to be kept in the circuit model.
The default on number of strongest coupling neighbors is 10; which means only outputting the 10 strongest neighbors (including self).
4. Ignore mutual capacitance or inductance if the ratio of mutual terms over self term is less than a percentage.
The default percentage threshold for ignoring mutual capacitance and inductance is 0.005.
If the mutual capacitance or inductance is less than the 0.5% of the minimum of the two self-capacitances / inductances, then it does not output the mutual capacitance / inductance.

LESSON TWO: SAVE WORK AREAS

Layout File

1. Click on the workspace.
2. Click on the **Open Layout File** icon (**green**) to open the project file.
3. Click on the **Save Layout File** icon (**green**) to save the project file.
4. To save the layout file under a different name, select:
Save as


NOTE!

Saving the workspace automatically saves the .spd file.
Saving the .spd file **does not** automatically saves the workspace.

Workspace

1. Click on the Workspace. The workspace opens.
2. Click on the **Save Workspace** icon (**yellow**) in the toolbar.
3. Use **Save as** to save the Workspace under a different name.

LESSON THREE: RUN THE SIMULATION

1. Click on the **Play** button  at the top of the window to start the extraction (simulation).
2. XtractIM only extracts RLCG for a net which has at least one pin at the Die-side and at least one pin at the board side.
3. At the beginning of the simulation, if some nets have Die-Board mis-match, a pop-up window opens.
4. Select the next action.
 - **Continue** — Continue the simulation
 - **More Information** — Examine what nets are mis-matched
 - **Stop** — Cancel the simulation

Investigate Mis-matched Nets

The **More Information** window lists all the mis-matched nets.

1. Investigate the mis-matched nets to see whether it is a special design or a defective design.
2. Decide whether or not to proceed with the simulation.
3. Choose **Continue**, **Stop** or **More Information**.

If 30 seconds pass and the user has not made a choice; then, by default, the simulation continues.

LESSON FOUR : OBSERVE AND SAVE SIMULATION RESULTS

XtractIM performs calculations for each net. The calculations include:

- Conductance
- Mutual capacitance with other nets
- Mutual loop inductance
- Resistance
- Self capacitance
- Self loop inductance

The inductance and capacitance are matrices.

In the Inductance Matrix, the Diagonal Element is the Self Inductance of each net.

The off-diagonal elements are mutual Inductance.

There are two concepts for capacitance matrix.

- Maxwell Capacitance Matrix
- SPICE Capacitance Matrix

Maxwell Capacitance Matrix — Each diagonal element is the loading capacitance

Example

Capacitance-to-ground when other nets are grounded. This represents the worst-case capacitive loading. Off-diagonal elements are mutual capacitance with negative values.

SPICE Capacitance Matrix — Each diagonal element is capacitance-to-ground. Off-diagonal elements are mutual capacitance with positive values.

View the relationship between Maxwell capacitance and SPICE capacitance matrix.

R, L and C

1. View **Resistance** for each net.
2. View **Self-inductance** for each net.
3. View **Self-capacitance** for each net.

Mutual Terms

1. View **Mutual Terms**.
2. View **Mutual Inductance**.
3. View **SPICE Mutual Capacitance**.

Usually conductance is very low, so there is no view for conductance.

Summary of the Extracted Results

1. Click on **Summary**.
2. View the data for R, L and C.
 - Extraction Frequency
 - Full RLC Matrix
 - Maximum / Minimum R, L, C
 - Nets Extracted
 - Package Name
3. Reorder the list if you wish.
4. Click on **R/L/C** full matrix. The matrix is saved on hard disk in .csv format.

SPICE Model Files Saved

Upon completing the simulation, both model files are saved in the same directory as the .spd file.

The total number of elements (R, L, M, C and G where M is the mutual inductance) in the circuit is displayed at the bottom of the window.

The SPICE Model is saved as a SPICE sub-circuit with the extension .ckt.

The SPICE model is a T-circuit.

IBIS Model Saved

The IBIS Model is saved as an IBIS package model.

The saved model has the extension .pkg.

Pin Model: IBIS Format

An .ibs format file is saved.

The saved file includes each single net R, L and C.

All power nets and ground nets are lumped together.

Pin Model: Excel Format

1. Click on **Pin Model: Excel format** in the SPICE / IBIS Model window.
2. A .csv file is loaded. The .csv file includes information for each Signal Net.
 - Net Length
 - Net Name
 - Pin Name
 - Self-C
 - Self-L
 - Self-R
 - Time Delay

Self-C is the Maxwell Capacitance.

The information for Power Nets does not include Net Length.

DC Resistance

1. Click:
DC Resistance
2. View the .csv file. DC Resistance is given for each of the Power, Ground and Signal Nets. A .csv file is saved on hard disk.

RLC Distributions

1. Click:
RLC Distributions
2. View the full matrix value of R, L and C.
RLC Distributions offers eight kinds of views.
3. View the RLC distributions.

Segment RLC

1. Click on **Segment RLC** in the workflow pane under:
View / Export Results
For each signal net, XtractIM outputs the segment RLC of each metal layer.
2. View the Segment RLC values. Note the three bars for Resistance, Inductance and Capacitance across the bottom of the screen.
3. Click on the **Resistance** bar. The Resistance values are displayed.
4. Click on the **Inductance** bar. The Inductance values are displayed.
5. Click on the **Capacitance** bar. The Capacitance values are displayed.

Save Simulation Results

1. In the Workflow pane click:
Save Results
The Save Extractor Result window appears.
2. Enter a file name.
3. Click on **Save**. The results are saved in a binary file. The file is named:
result_spd_file_name.xim
4. Click on **Cancel** if you do not want to save the results in the file name you entered.

Simulation Output Files

The **result** and **result*.xim** files save all the output data including:

- Package Model Files.
- SPICE Circuit
- Summary

The SPICE file and two IBIS files are automatically saved by the tool.

The result file is created only when the user chooses to save all the output data.

View the output files on hard disk.

- One **IBIS Package Model File** — The *.pkg file includes both L and C coupling elements
- One **Pin Model in Excel Format** — The *.csv file includes each signal net length, self-R, self-L, self-C, and time delay. No coupling elements are included
- One **Pin Model in IBIS Format** — The*.ibs file includes each signal net self-R, self-L, and self-C. No coupling element is included
- One **Summary Content in Excel Format** — The *.csv file includes the RLC Full Matrix
- Two **SPICE Circuit Files** — The Pi-model is named *.ckt; the T-model is named *_t.ckt
- Three **Segment RLC in Excel Format** — This segment includes the RLC of each metal layer with *.csv files

Load in Saved Results

1. Select **Load Results** in the workflow pane to load the saved results. The main window shows the selected result.
2. View **present results** or the **loaded results**.
 - **Loaded Curves** — Shows the loaded results
 - **Present Curves** — Present extracted results
3. To unload a loaded result, click on the toolbar icon:
Unload Extractor Result

LESSON FIVE: BATCH MODE SIMULATION

1. To run a simulation in batch mode, select:
Start > Run
2. Change to the directory where the XtractIM.exe file is located.
3. Upon completing the simulation, all output files are automatically saved in the same directory as the *.spd file.
 - *.ckt files
 - *.ibs files
 - *.pkg files
 - .csv files

Electrical Performance Assessment

This chapter takes you through the steps to use the XtractIM tool to analyze the electrical performance of the Power / Ground / Signal distribution system. XtractIM checks the Power / Ground distribution system by checking:

- Power-ground Net Pair: Inductance, Capacitance and Broadband Impedance
- Per pin Resistance and Inductance
- Current Density: Via Current, Plane Current Density, Voltage Distribution (PowerDC license required)

XtractIM checks the Signal Distribution System by checking:

- Wirebond / Trace Layout: Impedance and Coupling
- Net Couplings: Mutual LC and Near-ended Crosstalk
- Insertion and Return Loss

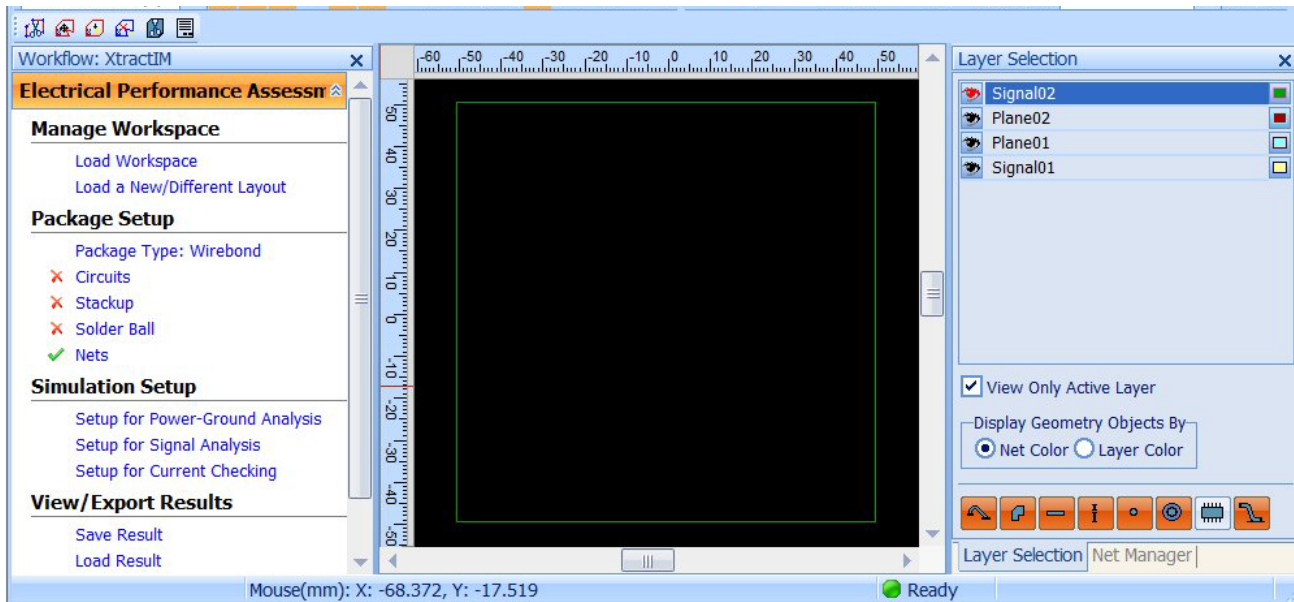
XtractIM can also create Html report including all features in electrical performance assessment:

- Html report can be manually created after the simulation is completed
- Html report can be automatically created upon the simulation's completion

LESSON ONE: SIMULATION SETUP

1. Launch **XtractIM**.
2. Select:
Mode > Elec. Perf. Assessment (EPA)

The **Electrical Performance Assessment Workflow** appears.



Setup Steps

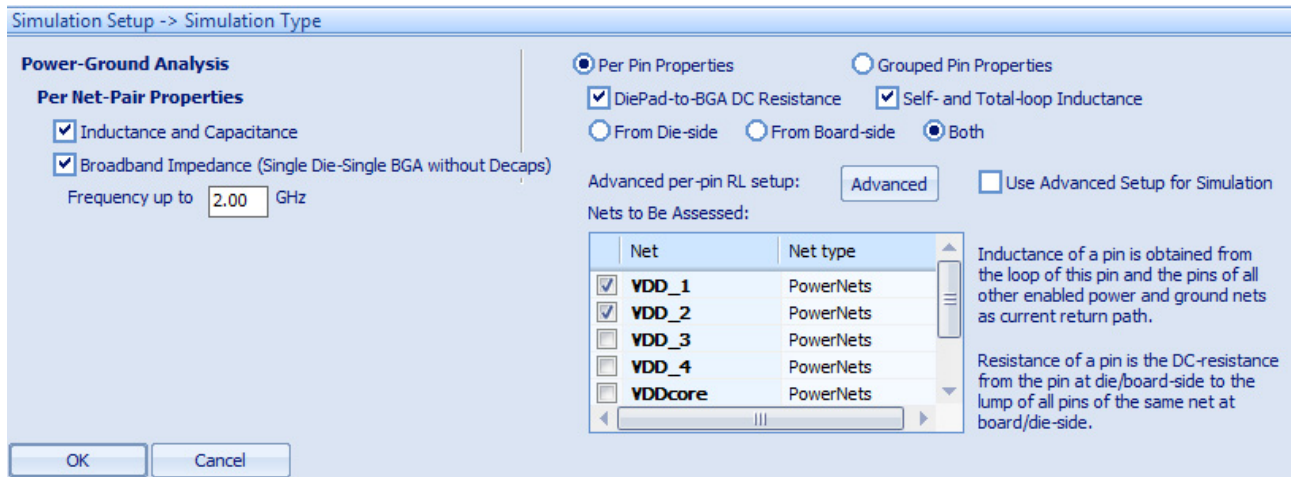
Follow these steps to perform a **Type Workflow** in **Interactive Mode**.

1. Load an existing file (.xml file), if any.
2. Open a layout file (.spd file).
3. Select a package type.
4. Setup the circuits.
5. Select or deselect Die-circuit and Board circuit.
6. Setup the Stackup.
7. Set parameters for the Bump or Solderball Medium layer.
8. Set the Bump data if it is a Flip-chip package.
9. Set the Solderball data.
10. Select the nets for simulation.
11. Simulation Setup.
12. Select automatically generate and save report.
13. Save the Workspace and Layout file.

Except for Step 11 and 12, all steps are exactly the same as the steps described in *IBIS / RLGC Module: Net-Based Simulation Single-Die Single-BGA Packages*.

Setup for Power/Ground Analysis

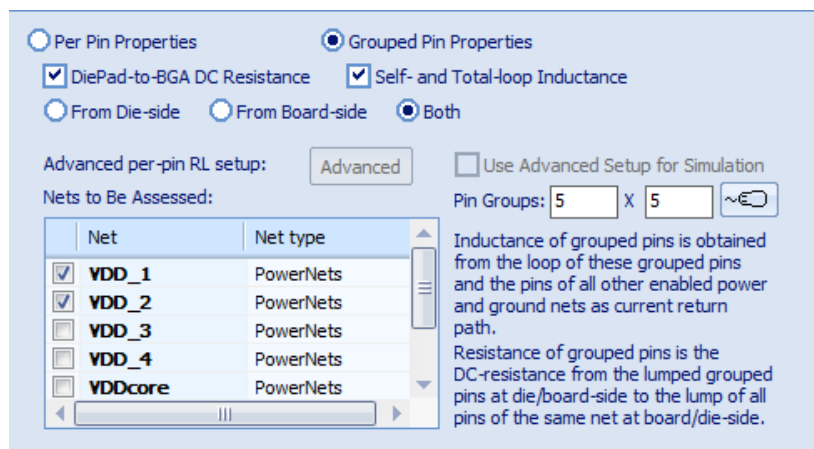
1. Select:
Simulation Setup > Setup for Power / Ground Analysis



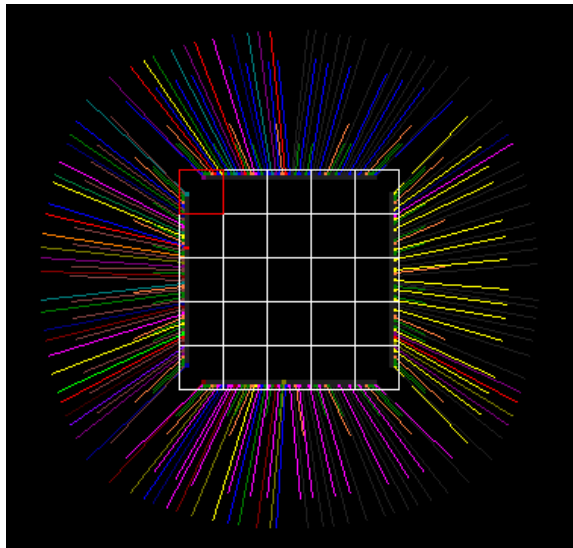
2. Select any or all of the following:
 - (Power to Ground) **Inductances and Capacitances**
 - **Broadband Impedance (Single Die-Single BGA without Decaps)** — Edit the highest frequency
 - **Bump-to-BGA DC Resistance** — Select Nets to be assessed
 - **Self- and Total-loop Inductance** — Select Nets to be assessed
3. Click **OK** to accept the selections.

Grouped Pin Property

If **Grouped Pin Property** is selected, user can choose $n * n$ groups.



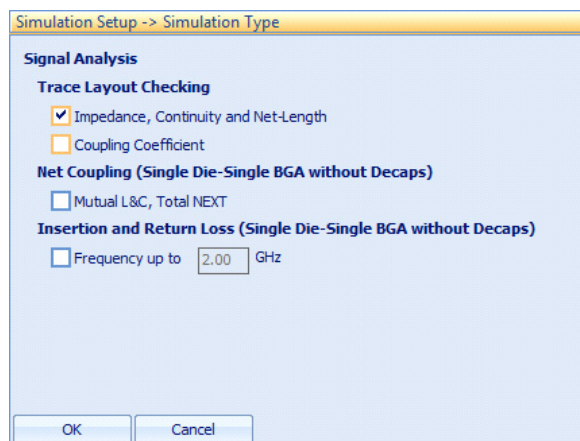
For example, enter 5 * 5 and it will give 25 cell as the following figure shows.



In each of the cells, instead of per pin assessment, all pins of the under assessment net will be lumped and assessed as one. The return paths are kept the same as per-pin properties assessment.

Setup for Signal Analysis

1. Select
Simulation Setup > Setup for Signal Analysis



2. Select any or all of the following:

Trace Layout Checking

Impedance, Continuity and Net-Length: Before running coupling and insertion and return loss analysis, it is helpful to run this check first to generate a length report for filtering out

the worse nets for insertion and return loss analysis, which is usually completed in seconds.

Signal Net Name	Net Length (mm)
FCHIP_A1	2785.115
FCHIP_A2	3663.313
FCHIP_A3	4550.800
FCHIP_A6	3442.505
FCHIP_A7	2442.132
FCHIP_A12	2484.810
FCHIP_A13	3407.297
FCHIP_A16	4623.287
FCHIP_A17	3678.313
FCHIP_A18	2785.115
FCHIP_B3	2865.140
FCHIP_B4	3758.338
FCHIP_B5	4659.820
FCHIP_B6	3613.363
FCHIP_B13	3671.353
FCHIP_B14	4651.536
FCHIP_B15	3758.338

Coupling Coefficient

Net Couplings (Single Die-Single BGA without Decaps)

Mutual L&C, Total NEXT

Insertion and Return Loss (Single Die-Single BGA without Decaps)

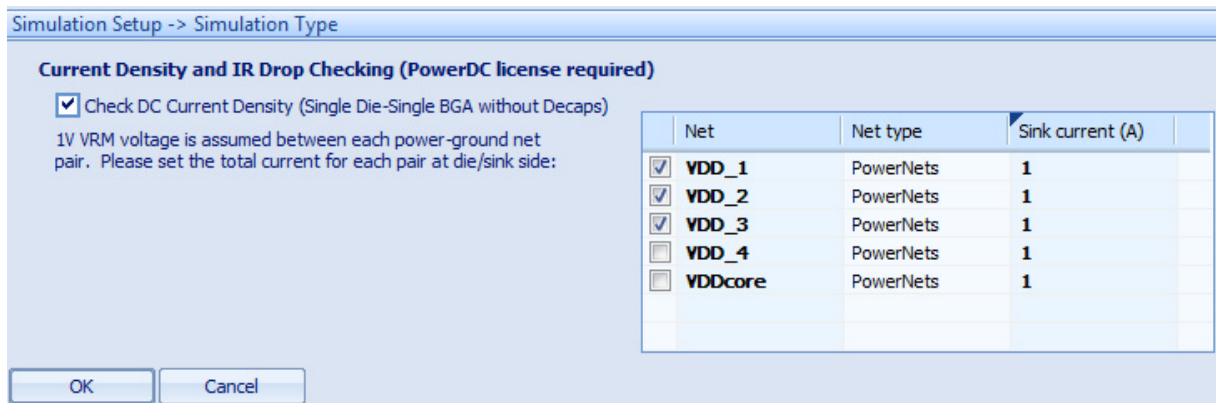
Frequency up to GHz

Insert the highest frequency in the GHz box.

3. Click **OK** to accept the selections.

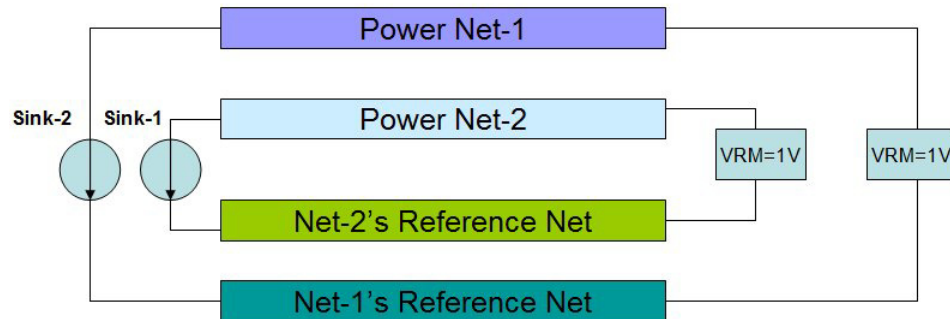
4. Select

Simulation Setup > Setup for Current Checking



- **Check DC Current Density (Single Die-Single BGA without Decaps)** — Every VRM voltage is set as 1V internally

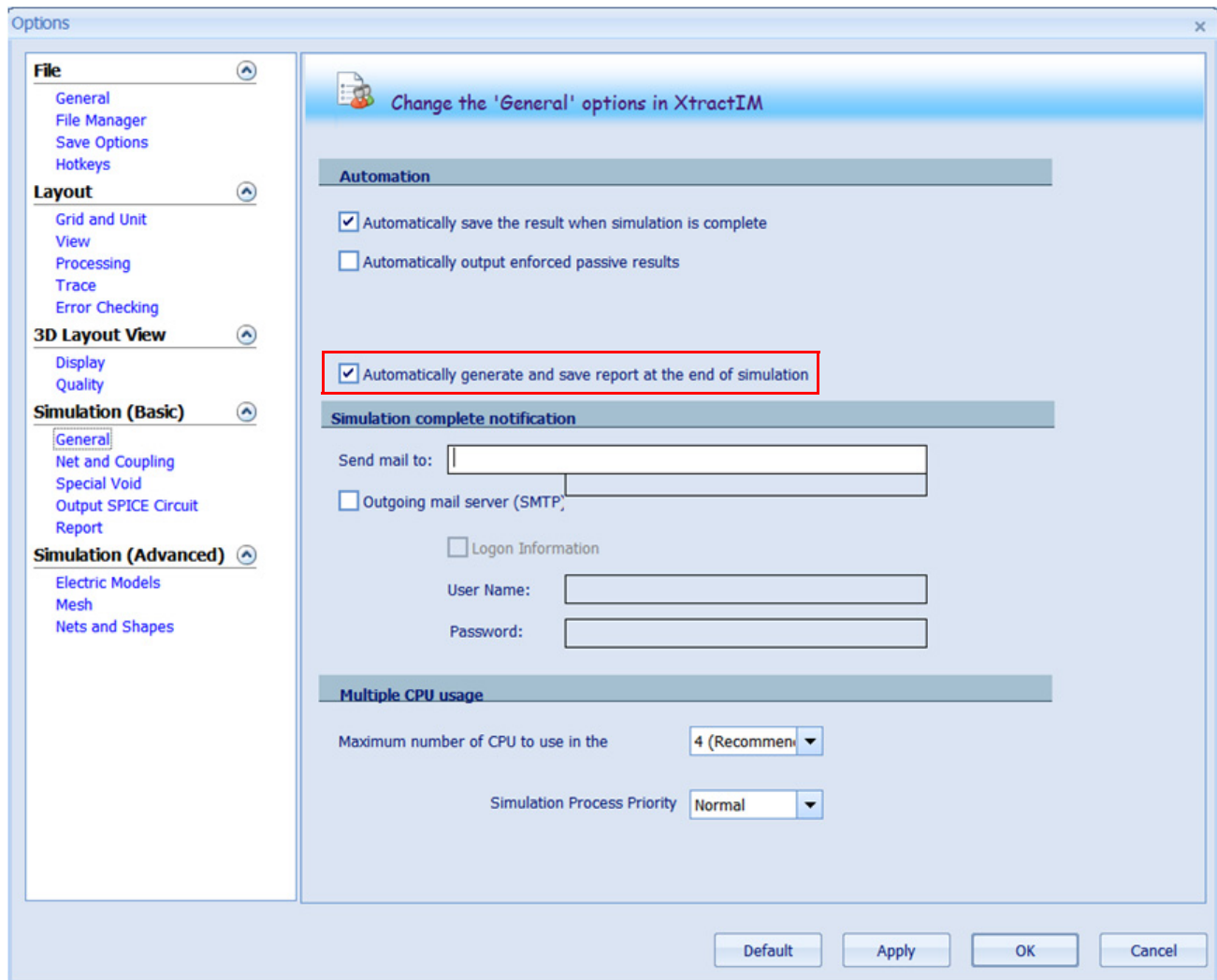
5. Set the **Sink Current**. Sink current is set for each power net and its reference ground net. The simulation will be based on equal voltage at the Sink Side.



6. Click **OK** to accept the selections.

Select Automatically Generate and Save Report


1. To automatically generate and save report upon simulation's completion, select Tools > Options > Edit Options... > Simulation (Basic) > General




2. Select the **Automatically generate and save report at the end of simulation** option.
3. Click **OK**.

Save Workspace

1. To save the workspace, click:
Workspace > Save
or


2. Click  to save both workspace and SPD file.


LESSON TWO: RUN AND SIMULATION


Click on the **Play** button  at the top of window to start the extraction.

LESSON THREE: OBSERVE AND SAVE SIMULATION RESULTS


The results are displayed after the simulation is finished.

View/Export Results 


Power-Ground Analysis 


Per Net-Pair Properties 

- Inductance and Capacitance
- Broadband Impedance


Per Pin Properties 


- R&L Histogram
- R&L by Layer
- R&L Distributions
- R&L Per Pin
- R&L 2D View

Signal Analysis 


Trace Layout Checking 

- Net Length Summary
- Net Impedance Summary
- Net Coupling Summary
- Impedance Plot (collapsed)
- Impedance Plot (expanded)
- Impedance Table
- Impedance by Layer
- Coupling Coefficient Plot (collapsed)
- Coupling Coefficient Plot (expanded)
- Coupling Coefficient Table
- Coupling Coefficient by Layer


Net Coupling 

Single-ended Based 


- Mutual Inductance and Capacitance
- Total NEXT Histogram

Diffpair and Single-ended 

- Mutual Inductance and Capacitance
- Total NEXT Histogram

Insertion and Return Loss 

- Insertion Loss
- Return Loss

Current Checking 

- Via Counts
- Via Current Histogram
- Via Current by Layer
- Via Current Table
- Voltage Distribution by Layer
- Plane Current Density by Layer
- Save Result

Power-Ground Analysis

Per Net-Pair Property

The Workspace lists the options to display all results. Click on the desired option.

Per Net-Pair Properties

[Inductance and Capacitance](#)

[Broadband Impedance](#)

1. Click:

Inductance and Capacitance

A table is displayed.

Power Net	Ref Ground Net	L(nH)	C(pF)	Ground Net	L(nH)
VDD_1	VSS	0.454952	43.3595	VSS	0.454952
VDD_2	VSS	0.458492	43.3065	VSScore	0.590788
VDD_3	VSS	0.451241	43.4001		
VDD_4	VSS	0.455836	43.2714		

- **Power Net** — Power Net Names
- **Ref Ground Net** — Reference Ground Net Name of smallest loop Inductance.
- **L(nH)** — Loop Inductance referring to the Ref Ground Net.
- **C(pF)** — Capacitance referring to the Ref Ground Net.
- **Ground Net** — Ground Net Name. Displays when Net Name is clicked.
- **L(nH)** — Inductance when the Power Net uses each Ground Net as the current return path. Displays when Net Name is clicked.

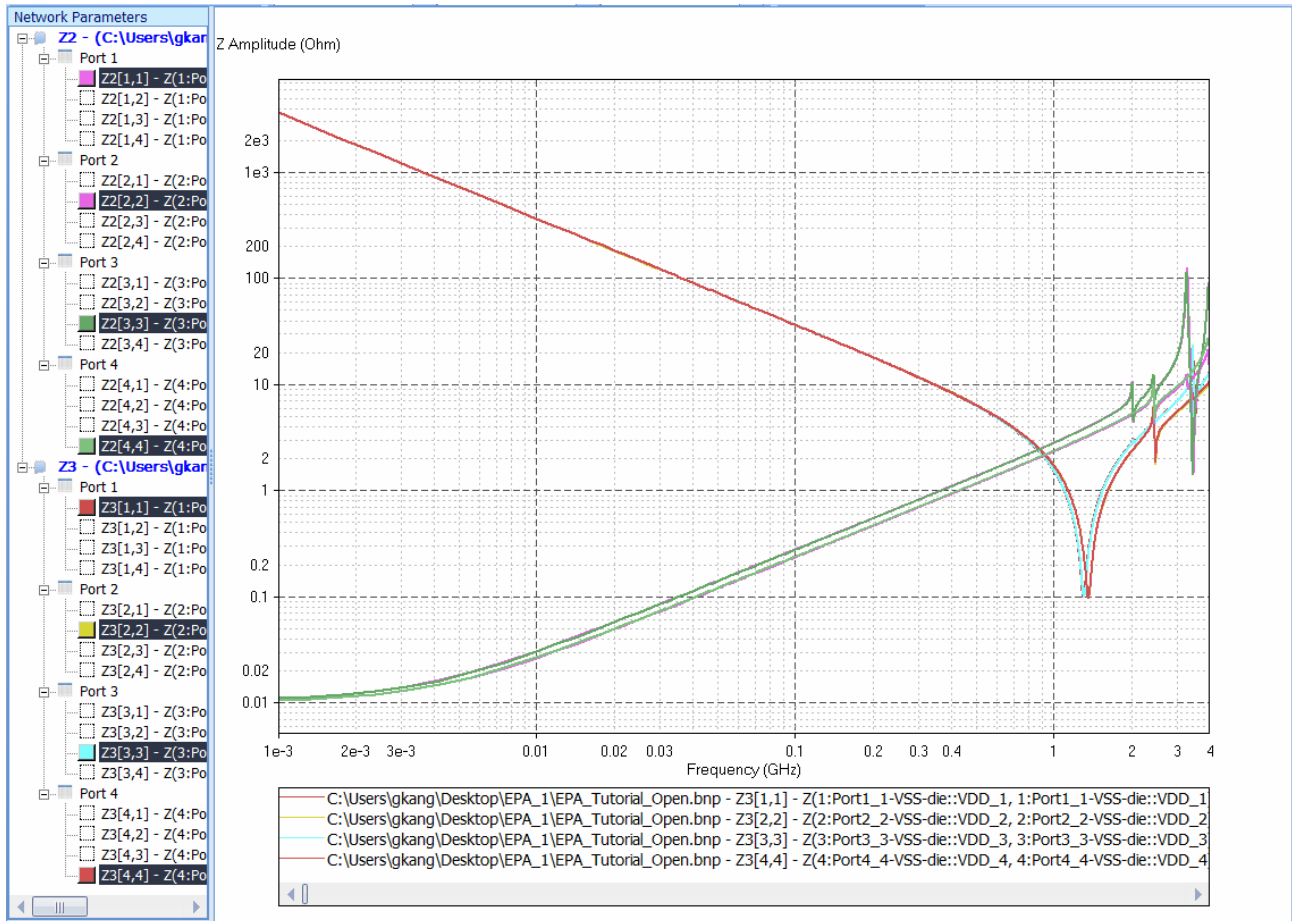
2. Click:

Broadband Impedance

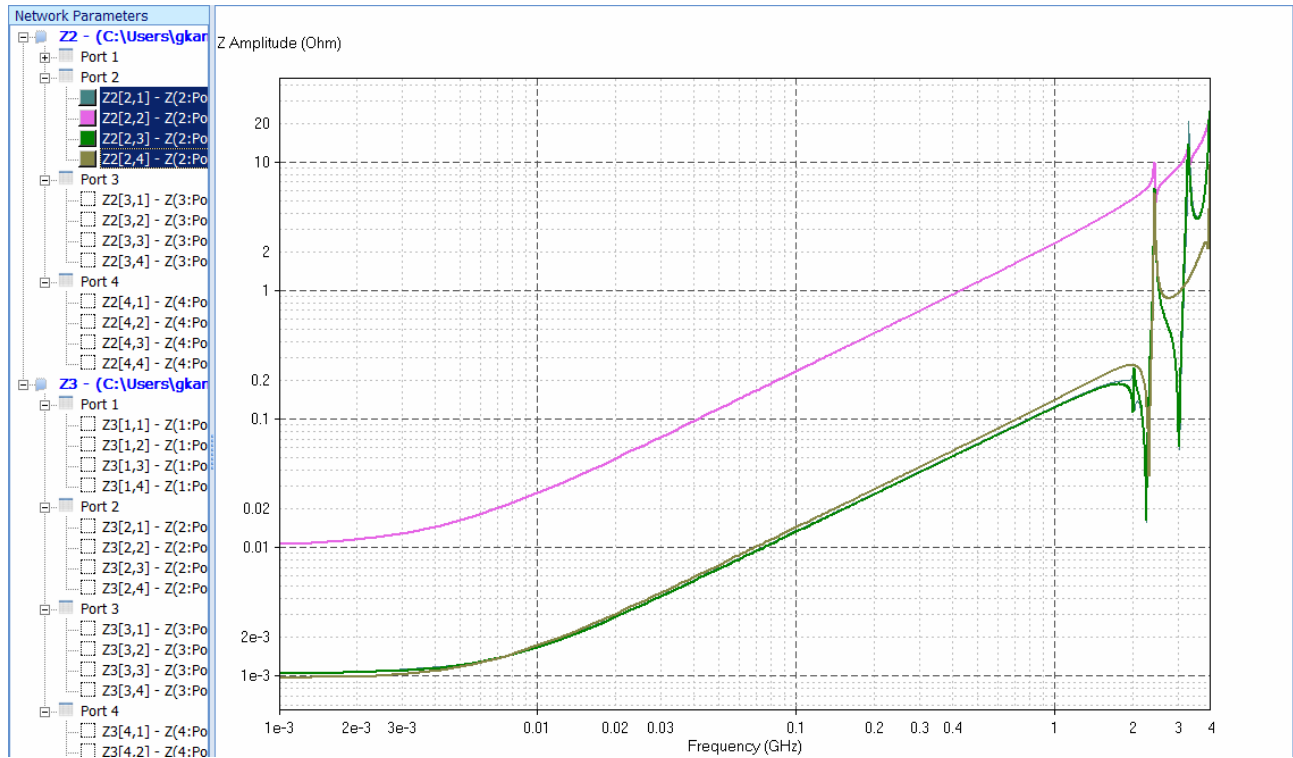
Short and Open Impedance (Z-parameter) vs. **Frequency** (1MHz-Fmax) are shown in the same plot. The **Observation Ports** are at Die Side. Each Port is defined as a Power Net refers to its Reference Ground Net.

Definition of Short and Open

- **Short** — Short each Power Net and its Reference Net at the Board Side.
- **Open** — Keep its Power Net and its reference Net open at the Board Side.



Enable all curves of one port, both the self-impedance and transfer impedance are shown.



Per Pin Property

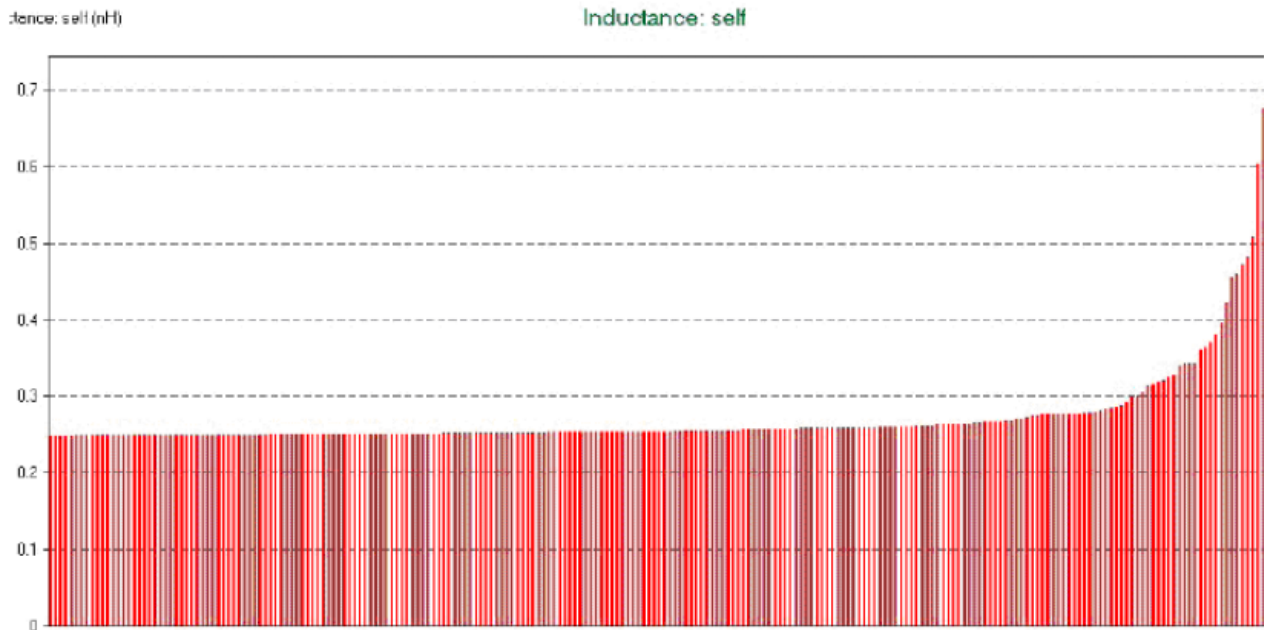
The Workspace lists the options to display all results. Click on the desired option.

Per Pin Properties

- R&L Histogram
- R&L by Layer
- R&L Distributions
- R&L Per Pin
- R&L 2D View

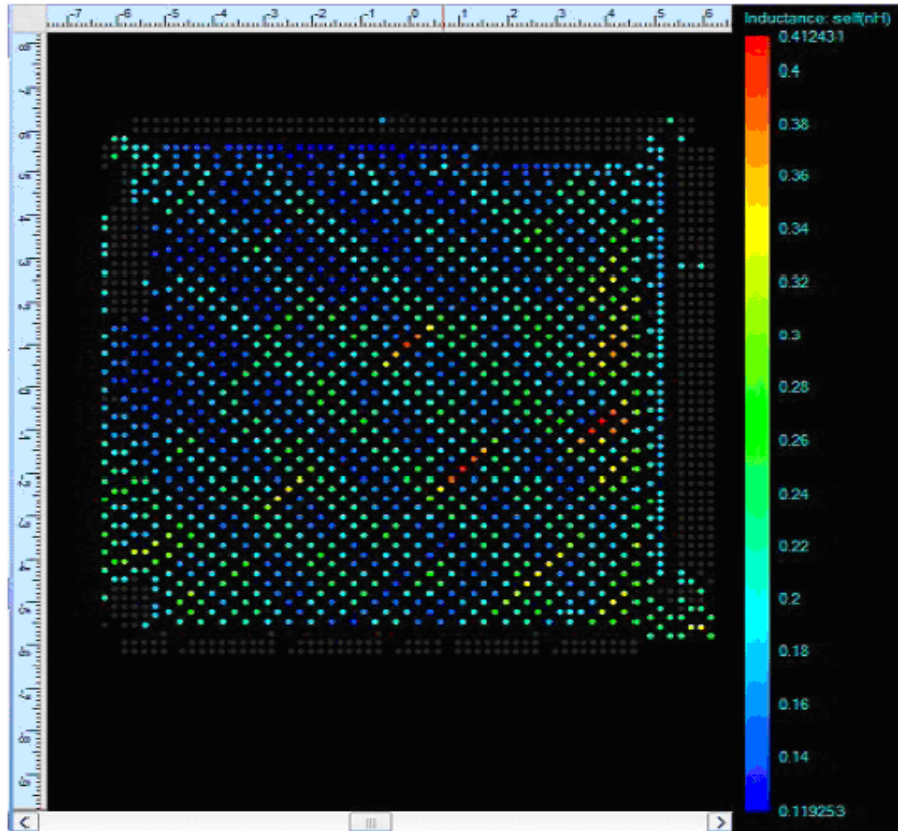
R&L Histogram

All pin RL values are plotted from the smallest (left) to the target.

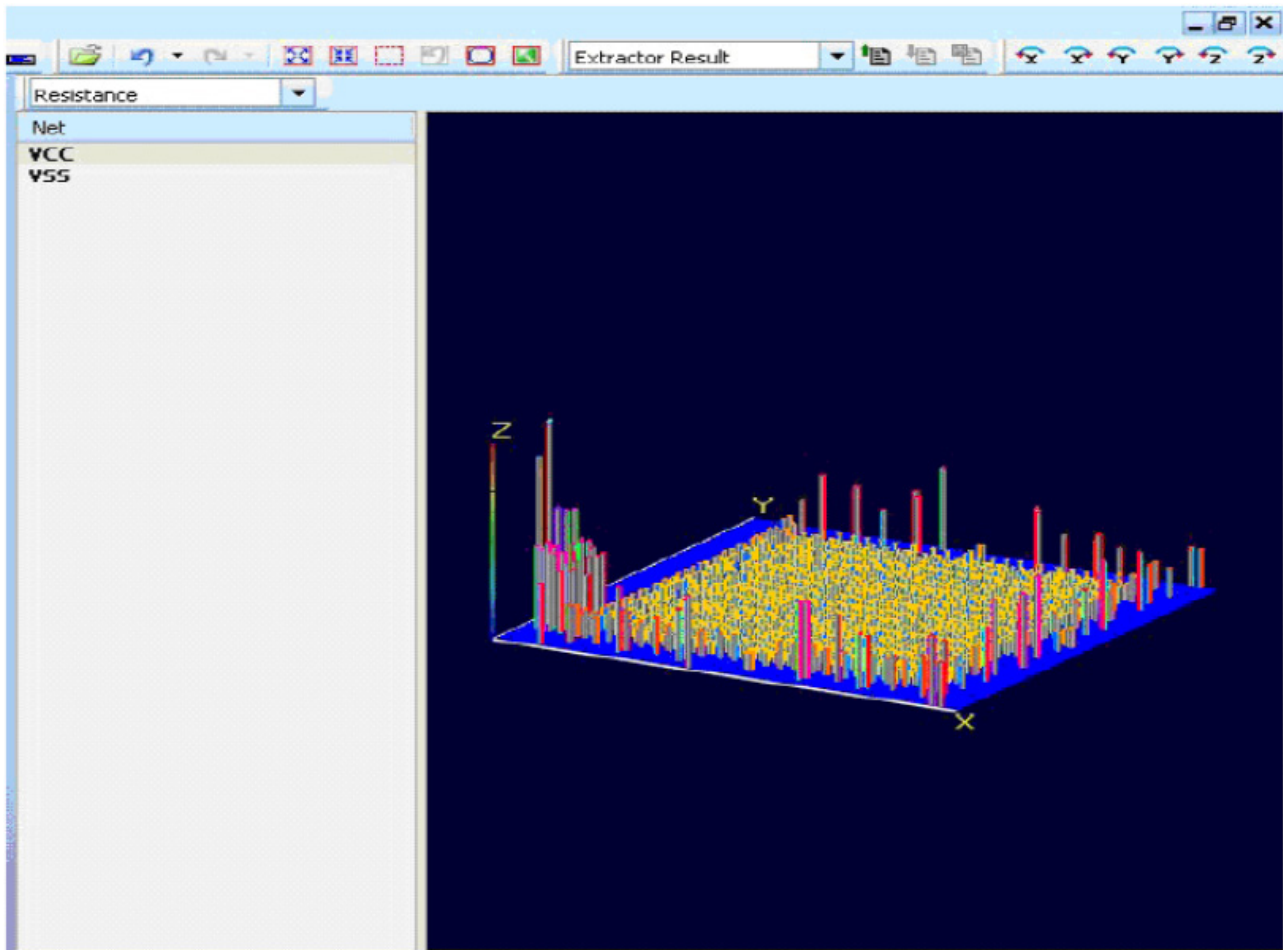


R&L by Layer

Inductance or resistance values are super-displayed in the layout.



R&L Distributions



- Use the **Rotation** icon to choose the preferred view.
- To save a file to any preferred name, select the name and click **Save**.

R&L Per Pin

Net	Pin NodeName	Self L(nH)	Total L(nH)	R(mOhm)	Induced Voltage(V)	Current(A)
FCHIP	Node03060!!A2::VDD	1.872	2.332	6.151	1.466	1.000
VDD	Node03069!!A11::VDD	1.845	2.315	6.149	1.454	1.000
VDD_15	Node03097!!D3::VDD	1.099	1.558	3.289	0.979	1.000
VSS	Node03104!!D10::VDD	1.071	1.534	2.966	0.964	1.000
BGA	Node03112!!E6::VDD	0.694	0.975	2.508	0.613	1.000
VDD	Node03114!!E8::VDD	0.817	1.301	14.615	0.818	1.000
VDD_15	Node03124!!F6::VDD	0.700	1.024	14.178	0.643	1.000
VSS	Node03126!!F8::VDD	0.784	1.227	14.229	0.771	1.000
	Node03136!!G6::VDD	0.761	1.212	14.036	0.762	1.000
	Node03138!!G8::VDD	0.728	1.078	14.593	0.677	1.000
	Node03148!!H6::VDD	0.813	1.238	14.529	0.778	1.000
	Node03150!!H8::VDD	0.792	1.176	14.647	0.739	1.000
	Node03157!!J3::VDD	1.053	2.196	3.233	1.380	1.000
	Node03164!!J10::VDD	0.961	1.968	2.931	1.237	1.000
	Node03170!!K4::VDD	1.288	2.423	34.876	1.522	1.000
	Node03175!!K9::VDD	1.190	2.190	34.574	1.376	1.000
	Node03192!!M2::VDD	1.993	2.362	6.120	1.484	1.000
	Node03201!!M11::VDD	1.634	2.040	6.132	1.282	1.000

- Column 1 - Net names
- Column 2 - Pin node name of the selected net
- Columns 3 and 4 - DC Resistance and Loop Inductance of each pin
- Columns 5 and 6 - Induced Voltage and Current of each pin

These two columns provide a current-weighted per-pin power/ground RL assessment before running a system-level PI/SI analysis if you have a current vector.

- Induced Voltage is calculated by $dv=L*(di/dt)$
- The induced Current is calculated by $[L_matrix]_{N*N}[Current]$

N is pin number for a net. By default, all the pins have the same current value 1A.

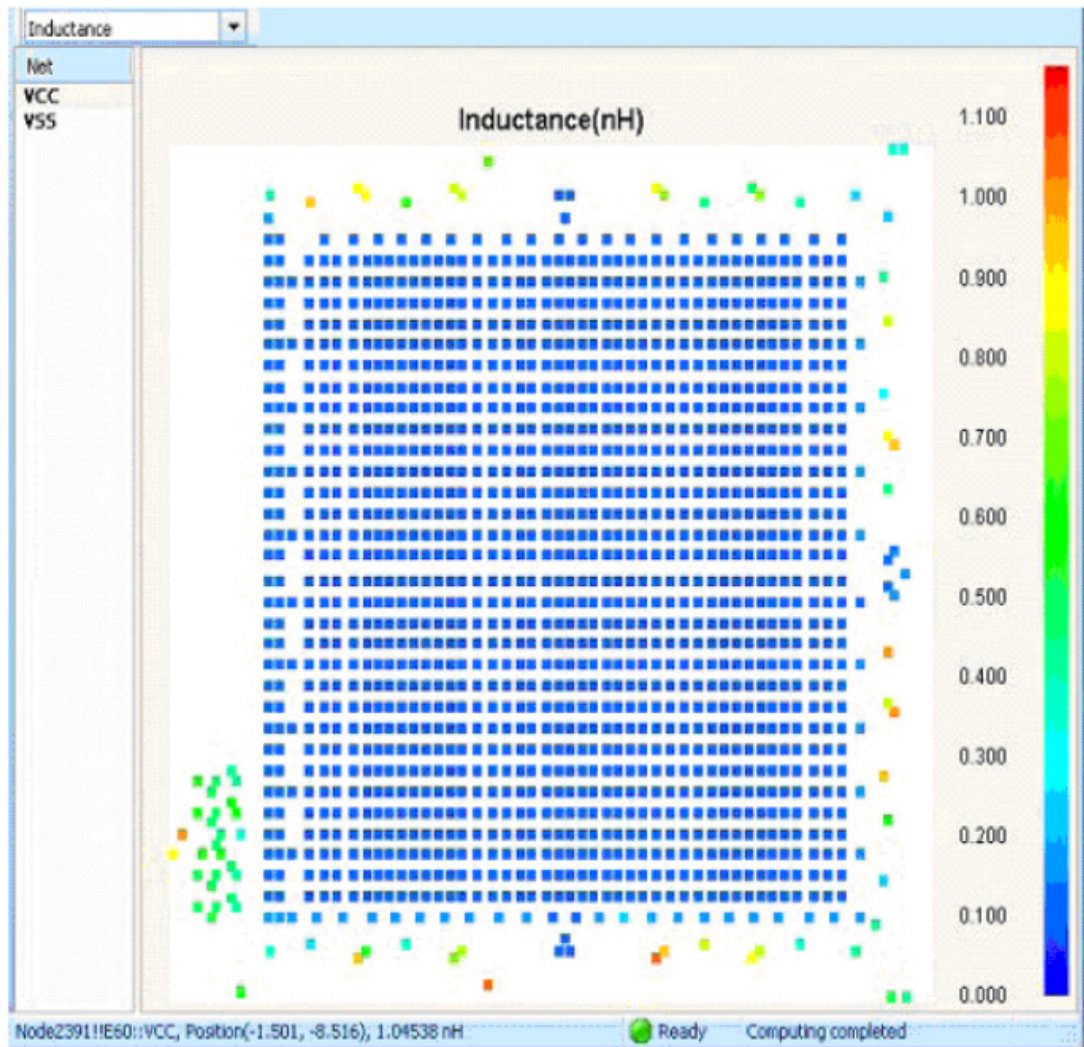
1. Click the **E** button in the Current column of a pin, and input the pin Current value.

The Induced Voltage result will be updated instantly.

Induced Voltage(V)	Current(A)	
2.054	1.500	E
1.527	1.000	
0.995	1.000	
0.972	1.000	
0.620	1.000	
0.834	1.000	
0.645	1.000	
0.777	1.000	
0.763	1.000	
0.679	1.000	
0.779	1.000	
0.740	1.000	
1.383	1.000	
1.238	1.000	
1.526	1.000	
1.378	1.000	
1.485	1.000	
1.282	1.000	

2. Click:
Pin Node Name
3. Sort the list in ascending or descending order.
4. Click:
R(mOhm) or L(nH)
5. Sort the items in ascending or descending order. The results are displayed in a table.

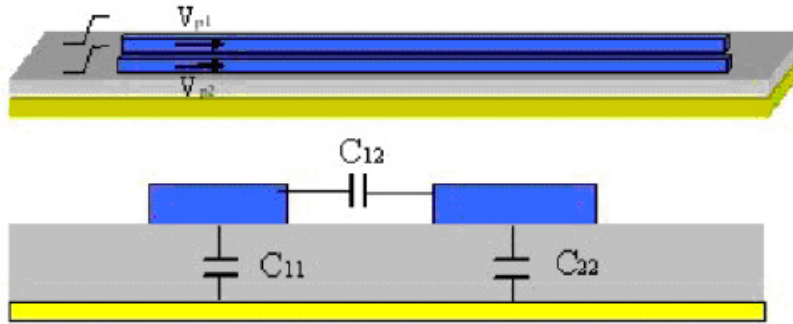
R&L 2D View



1. Select from the drop-down menu to see **Resistance** or **Inductance**.
2. Move the cursor across the Layout window.
3. Pause the cursor on a point of interest. The display shows:
 - Node Name
 - X-Y coordinates
 - Actual number

Signal Distribution System Checking

Trace coupling is defined with Near-ended Crosstalk as a victim.



Aggressor: Z_{10} , L_{11} , C_{11}

Victim: Z_{20} , L_{22} , C_{22}

$$K = \frac{V_p}{4} \left(C_{12} Z_{20} + \frac{L_{12}}{Z_{10}} \right)$$

Where, $\frac{2}{V_p} = \frac{1}{V_{p1}} + \frac{1}{V_{p2}}$

$$V_{p1} = \frac{1}{\sqrt{L_{11} C_{11}}} \quad V_{p2} = \frac{1}{\sqrt{L_{22} C_{22}}}$$

$$Z_{10} = \sqrt{\frac{L_{11}}{C_{11}}} \quad Z_{20} = \sqrt{\frac{L_{22}}{C_{22}}}$$

Definitions


K	The near-end coupling coefficient from aggressor Net on victim Net.
C_{11} / C_{22}	The loading capacitance per unit length of Signal Net to its Reference Net.
L_{11} / L_{22}	The self-inductance per unit length of Signal Net.
C_{12}	The mutual capacitance per unit length between aggressor and victim Net.
L_{12}	The mutual inductance per unit length between aggressor and victim Net.
V_{p1} / V_{p2}	The signal velocity propagates on Signal Net.
Z_{10} / Z_{20}	The characteristic impedance of Signal Traces.


Trace / Wirebond Layout Checking

The Workspace lists all results to be displayed. The first three summaries are for all enabled **Signal**

Nets in the package.

The rest of the summaries are for a specific path from one component to another component. For the Single-die Single-BGA package, the path is from Die to Board.

Signal Analysis 

Trace Layout Checking 

- [Net Length Summary](#)
- [Net Impedance Summary](#)
- [Net Coupling Summary](#)
- [Impedance Plot \(collapsed\)](#)
- [Impedance Plot \(expanded\)](#)
- [Impedance Table](#)
- [Impedance by Layer](#)
- [Coupling Coefficient Plot \(collapsed\)](#)
- [Coupling Coefficient Plot \(expanded\)](#)
- [Coupling Coefficient Table](#)
- [Coupling Coefficient by Layer](#)

1. Click

Net Length Summary.

A summary table for enabled signal nets is displayed.

Signal Net Name	Net Length (mm)
FCHIP_A1	2785.115
FCHIP_A2	3663.313
FCHIP_A3	4550.800
FCHIP_A6	3442.505
FCHIP_A7	2442.132
FCHIP_A12	2484.810
FCHIP_A13	3407.297
FCHIP_A16	4623.287
FCHIP_A17	3678.313
FCHIP_A18	2785.115
FCHIP_B3	2865.140
FCHIP_B4	3758.338
FCHIP_B5	4659.820
FCHIP_B6	3613.363
FCHIP_B13	3671.353
FCHIP_B14	4651.536
FCHIP_B15	3758.338
FCHIP_B16	2865.140
FCHIP_C2	3758.338
FCHIP_C17	3783.338
FCHIP_F2	3588.363
FCHIP_F17	3563.363
FCHIP_H2	2639.099
FCHIP_H17	2639.099
FCHIP_K2	3729.343
FCHIP_K17	3654.784
FCHIP_M2	2748.339
FCHIP_M17	2699.454
FCHIP_U3	3640.140
FCHIP_U5	3638.069
FCHIP_U6	2846.734
FCHIP_U13	2753.008

2. Click:

Net Impedance Summary

A summary table is displayed. The table includes the following information for all selected Signal Nets.

- Net Name
- Number of Trace Reference Discontinuity
- Number of Vias
- Maximum Impedance
- Minimum Impedance
- Dominant Impedance
- Dominant Impedance Length Percentage
- Trace / Wirebond Length

Net Count	Net Name	No. of Trace Ref...	No. of Vias	Maximum Impedance (ohm)	Minimum Impedance (ohm)	Dominant Impedance (ohm)	Dominant Imp Length (%)	Trace ,wirebond total length(n
1	Net_1	0	2	74.012	35.423	74.012	92.567	6.727
2	Net_2	0	2	74.012	35.423	74.012	91.363	5.790
3	Net_3	0	2	74.012	35.423	74.012	91.562	5.927
4	Net_4	0	2	74.012	35.423	74.012	92.618	6.774
5	Net_5	0	2	74.012	35.423	74.012	93.888	8.181
6	Net_6	0	2	74.012	35.423	74.012	92.951	7.094
7	Net_7	0	2	74.012	35.423	74.012	92.412	6.590
8	Net_8	0	2	74.012	35.423	74.012	91.860	6.143
9	Net_9	0	2	74.012	35.423	74.012	91.255	5.718
10	Net_10	0	2	74.012	35.423	74.012	90.623	5.333
11	Net_11	0	2	74.012	35.423	74.012	89.975	4.988
12	Net_12	0	2	74.012	35.423	74.012	89.315	4.680
13	Net_13	0	2	74.012	35.423	74.012	88.811	4.469
14	Net_14	0	2	74.012	35.423	74.012	88.227	4.247

3. Click:

Net Coupling Summary

A summary table is displayed. It includes the following information for all selected Signal Nets.

- Net Name
- Aggressor Net with Max Coupling
- Maximum Coupling Coefficient
- % Length with Max Coupling over the total length
- % Length with Coupling Coefficient > 0.05
- % Length with Coupling Coefficient 0.03 - 0.05
- % Length with Coupling Coefficient 0.02 - 0.03

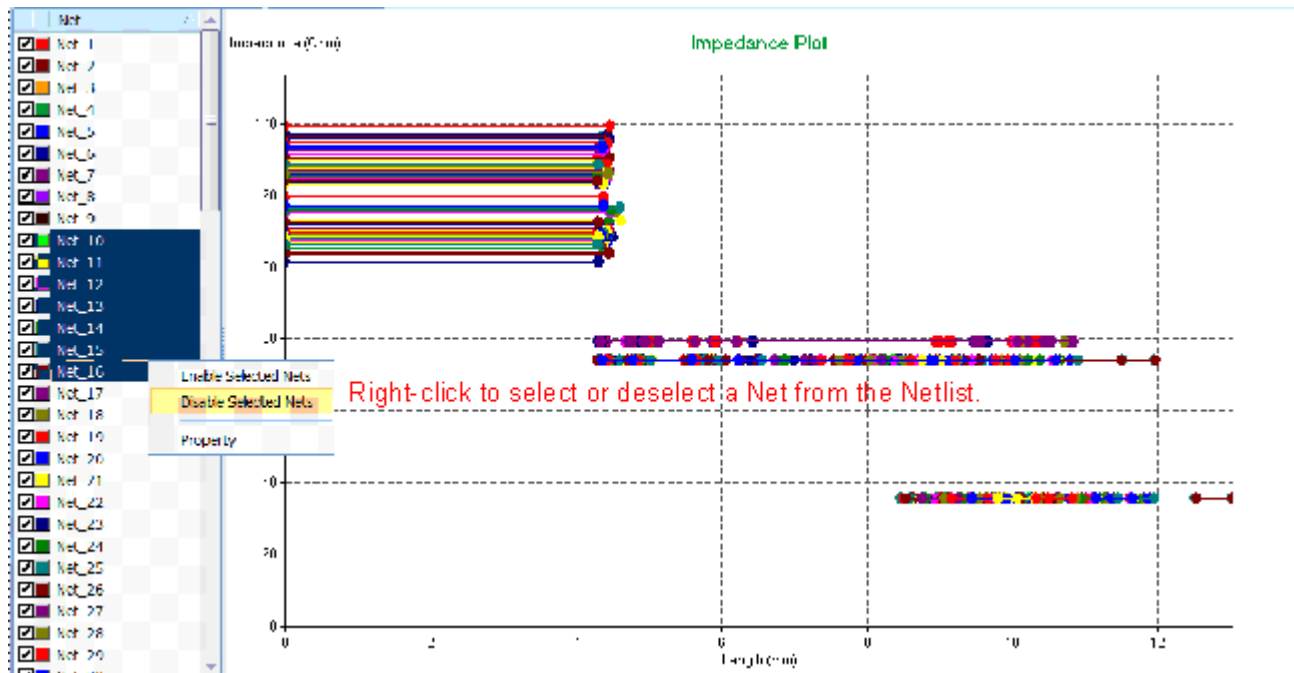
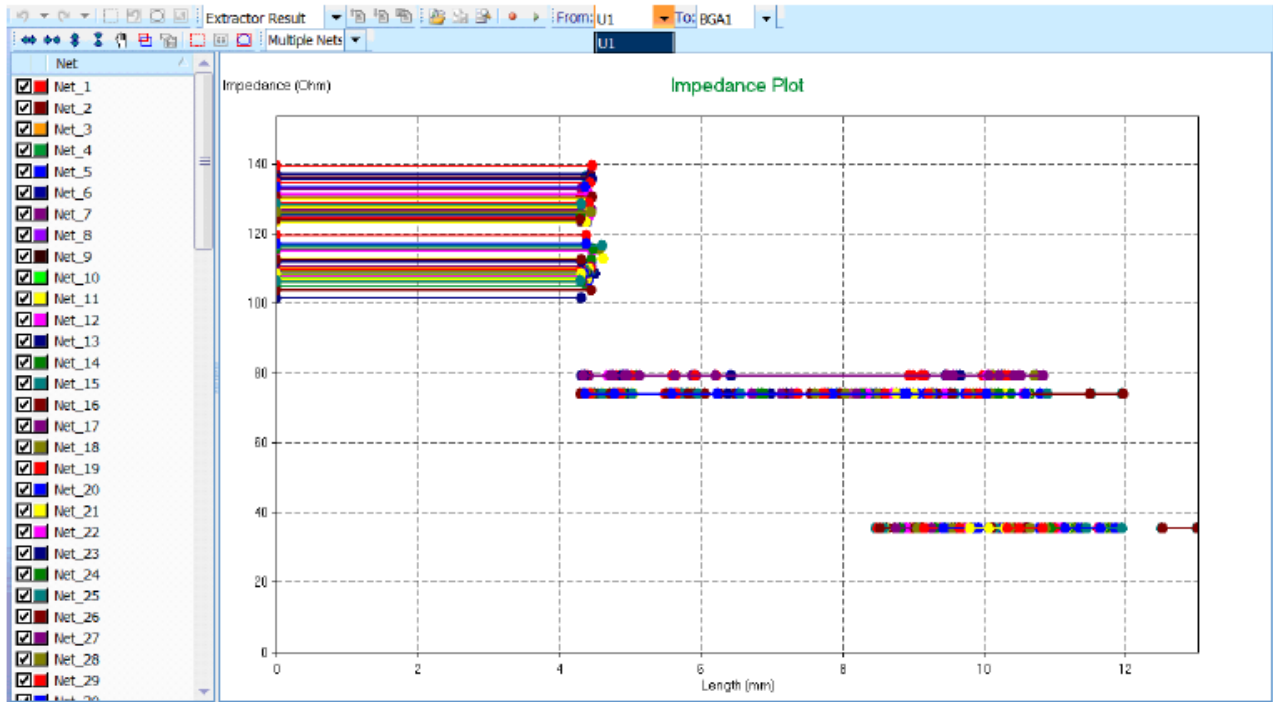
Net count	Net name	Aggressor net with max coupling	Max coupling coefficient	% length with max coupling	% length with coupling coef > 0.05	% length with coupling coef 0.03-0.05	% length with
1	Net_1	Net_10	0.109	39.193	39.193		
2	Net_2	Net_13	0.106	43.369	43.369		
3	Net_3	Net_18	0.042	42.764		42.764	
4	Net_4	Net_21	0.140	39.293	80.033		
5	Net_5	Net_24	0.057	34.417	34.417		
6	Net_6	Net_7	0.036	37.776		37.776	
7	Net_7	Net_8	0.057	39.445	39.445		
8	Net_8	Net_9	0.110	41.265	41.265		
9	Net_9	Net_8	0.111	42.986	42.986		
10	Net_10	Net_1	0.109	44.843	44.843		
11	Net_11	Net_12	0.043	46.771		46.771	
12	Net_12	Net_2	0.044	48.573		48.573	
13	Net_13	Net_2	0.107	49.801	49.801		

4. Click:

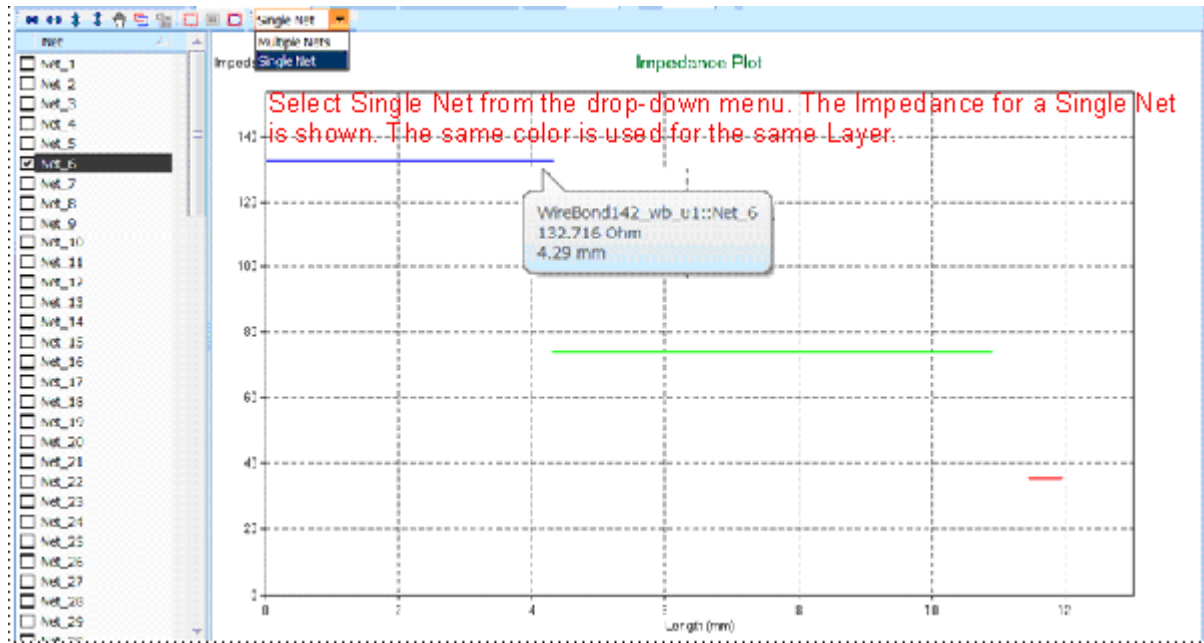
Impedance Plot (collapsed)

The **Trace and Wirebond Impedance** is displayed (collapsed) from Die to Board Circuit.

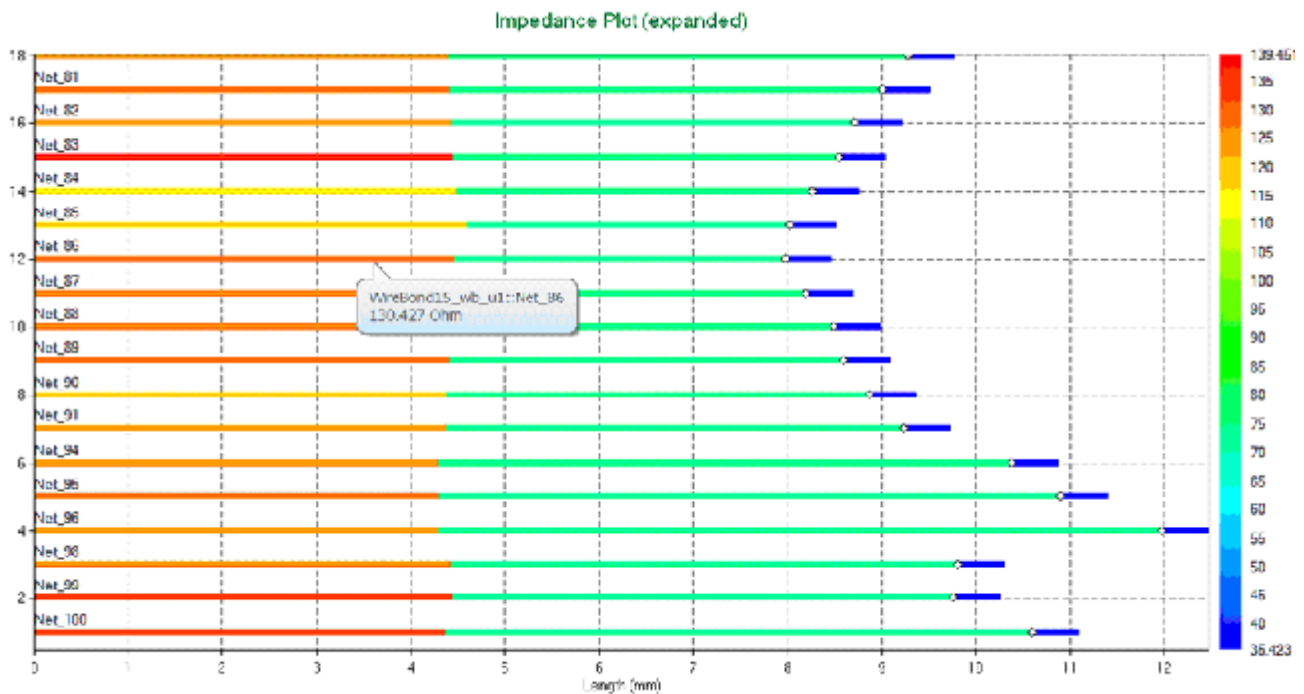
NOTE!	<p>If it is a Multi-die package, then follow these steps.</p> <ol style="list-style-type: none"> 1. Select a Component Name in the From: drop-down list. 2. Select a Component Name in the To: drop-down list. <p>The Trace and Wirebond Impedance along the path of the Start-Component to the End-Component is shown for all Nets between the selected two components.</p>
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If there are any reference changes on the same layer, those changes are clearly marked.

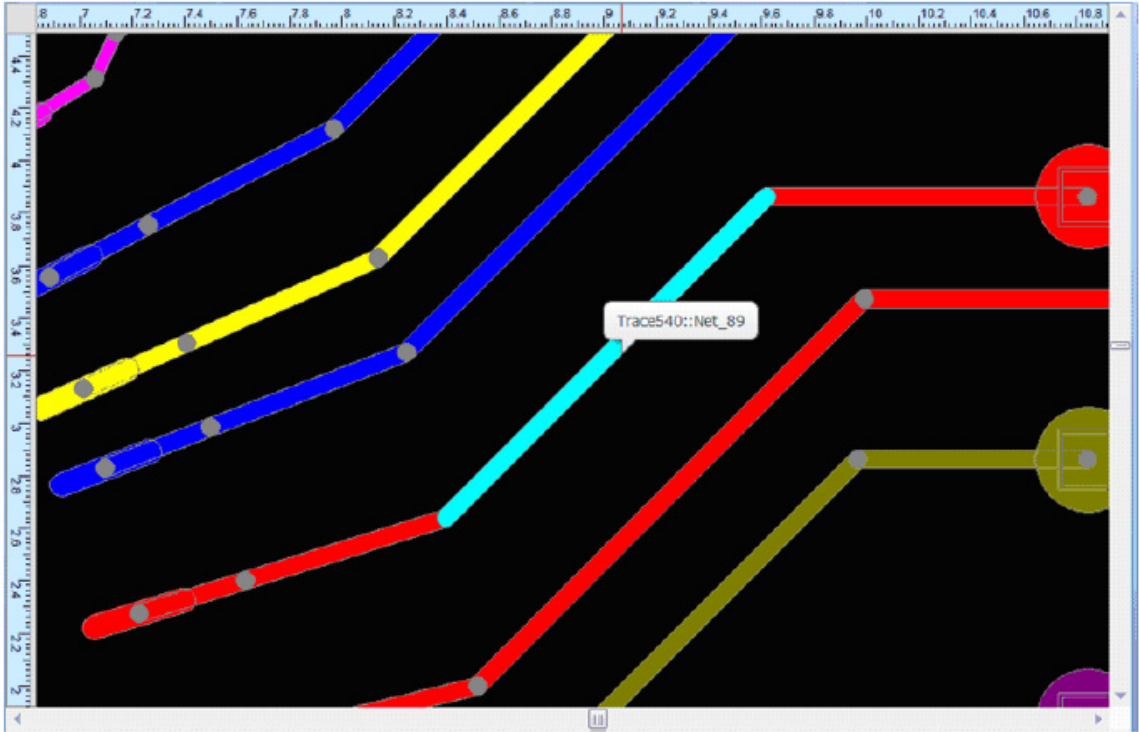


- Click: Impedance Plot (expanded)
Trace and Wirebond Impedance is displayed from Die to Board Circuit (expanded).



Place your cursor on a Curve or Line. Detailed information about the selected Curve or Line is displayed.

NOTE! To use the Cross Probe feature, double-click on any Trace section in the plot. The Trace is shown in the layout with the highlighted line.



Impedance

1. Click:

Impedance Table

For each Net, the table displays each:

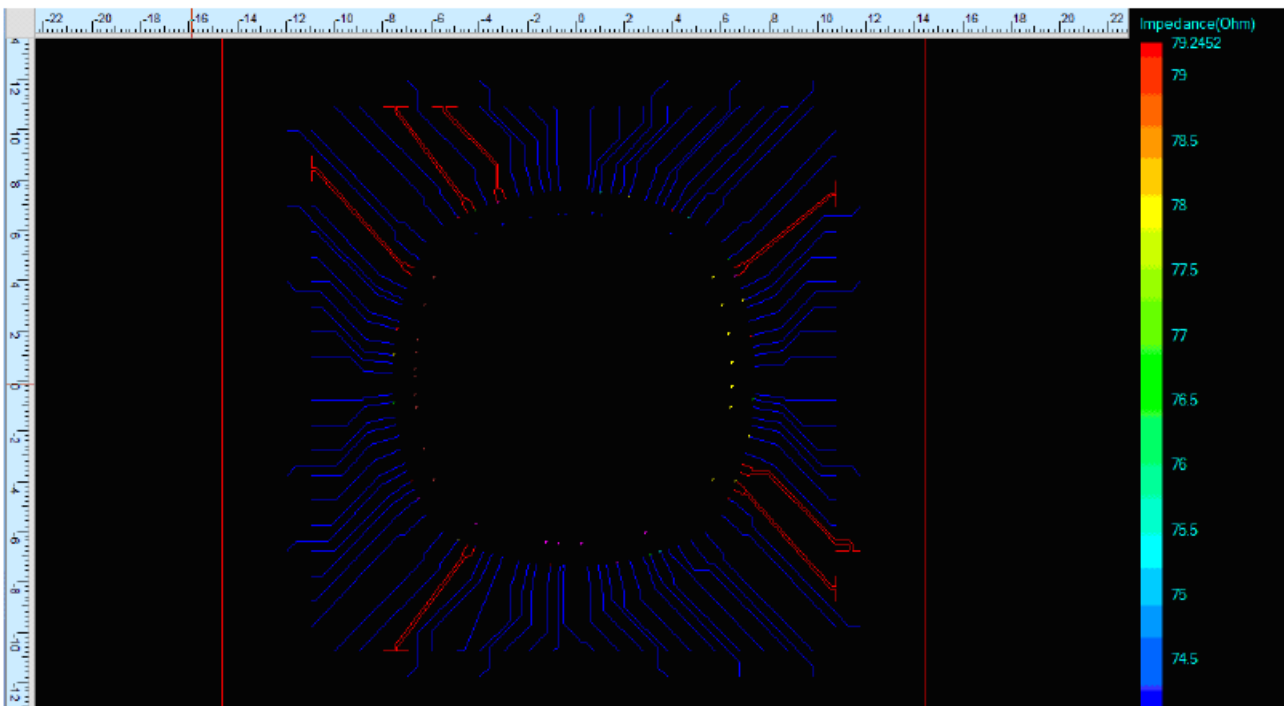
- Section name
- Length percentage over the whole length
- Impedance
- Total length
- Distance from starting component

Net	Trace/wirebond Name	% of its net length	Impedance(Ohm)	Length(mm)	Trace/wirebond distance from Starting Component(mm)
Net_1	WireBond175_wb_u...	37.32%	106.885	4.336	0.000
Net_2	Trace701::Net_1	3.68%	74.012	0.427	4.336
Net_3	Trace700::Net_1	6.89%	74.012	0.800	4.763
Net_4	Trace699::Net_1	27.08%	74.012	3.146	5.563
Net_5	Trace698::Net_1	11.24%	74.012	1.306	8.710
Net_6	Trace697::Net_1	4.72%	74.012	0.548	10.015
Net_7	Trace239::Net_1	4.30%	35.423	0.500	11.118
Net_8					
Net_9					
Net_10					

2. Click:

Impedance in Layout

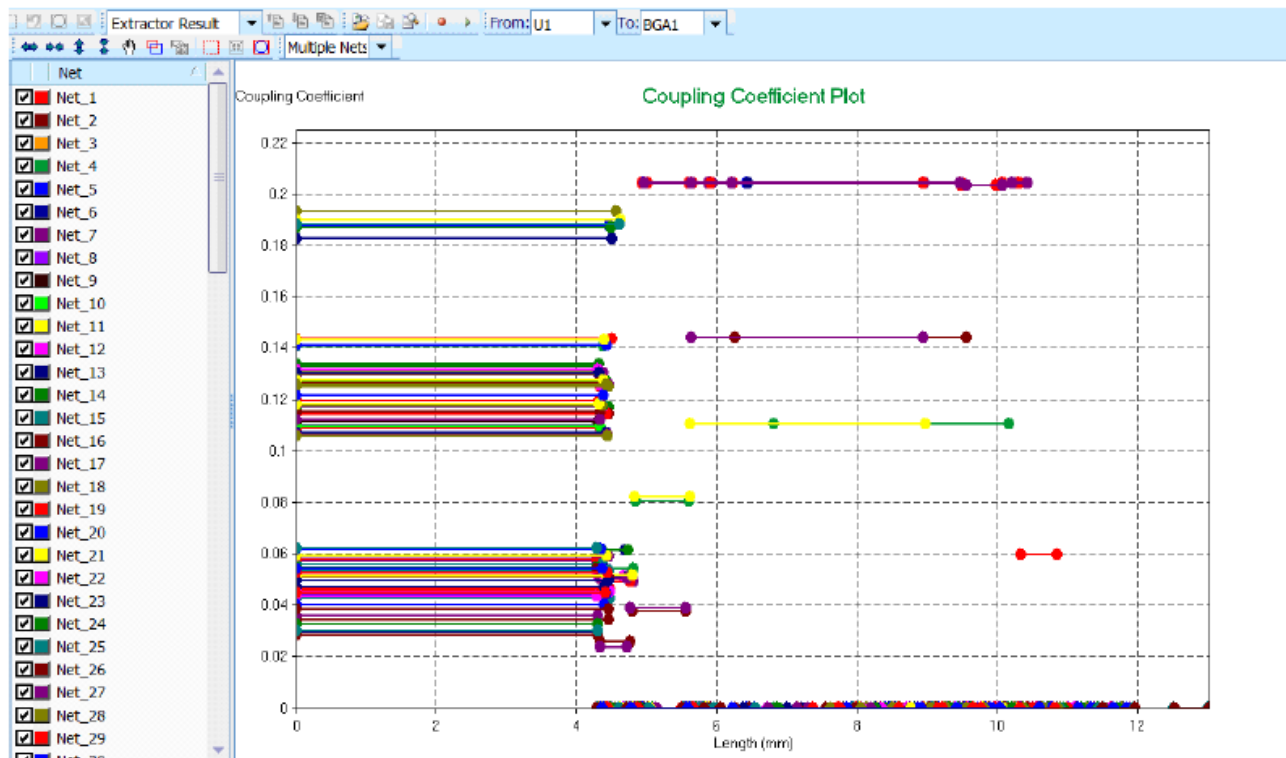
3. Select a Component Name in the **From:** drop-down list.
4. Select a Component Name in the **To:** drop-down list. The Impedance along the Traces and Wire-bonds between the two selected components is shown.



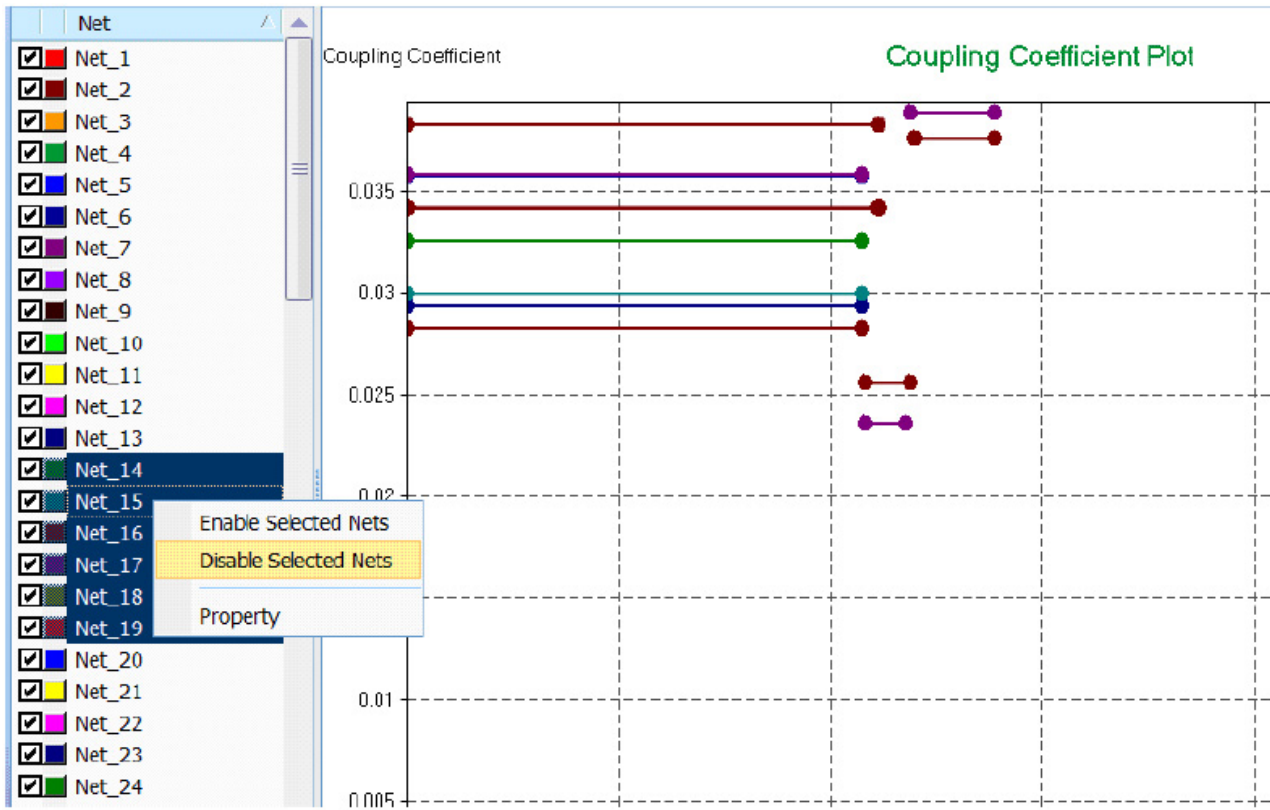
Coupling Coefficient

1. Click:
Coupling Coefficient Plot (collapsed)
2. Select a Component Name in the **From:** drop-down list.
3. Select a Component Name in the **To:** drop-down list.

The strongest coupling coefficient of each Trace and Wirebond section is displayed (collapsed) from the **Start Component** to the **End Component**.



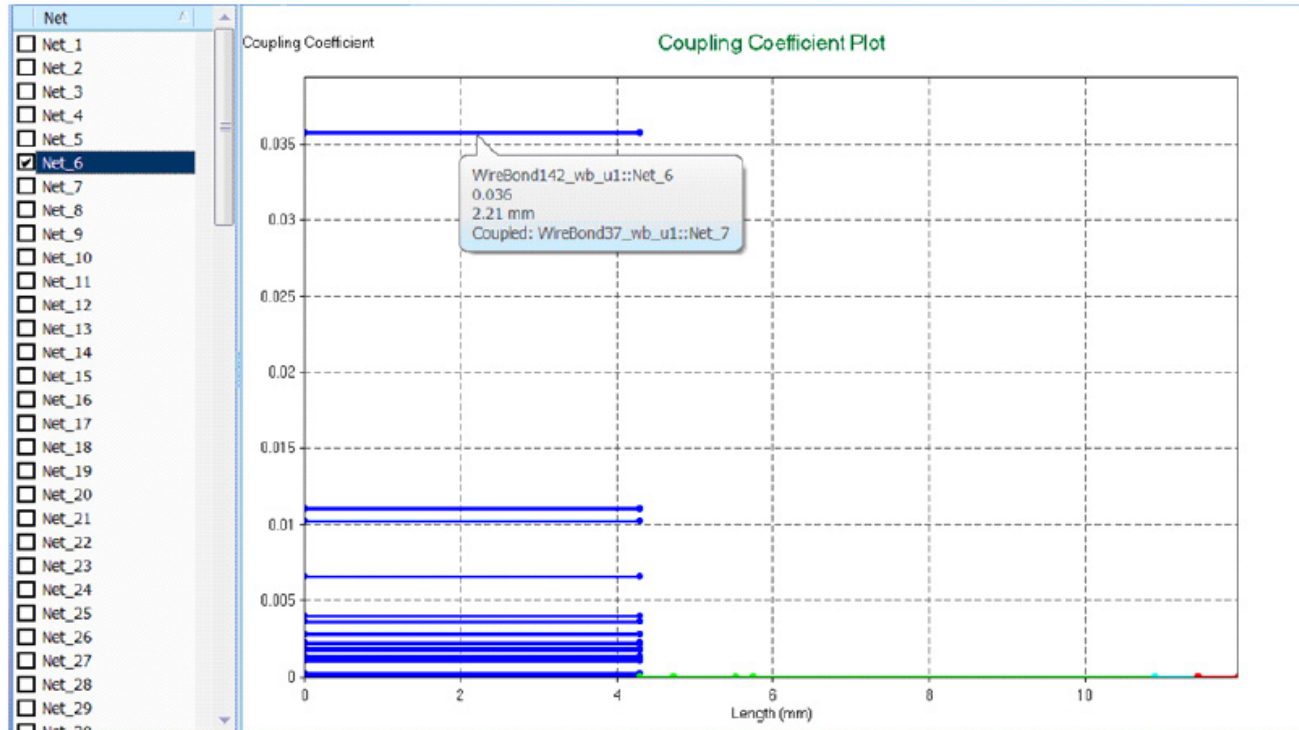
- 4. Select Nets in the Netlist.
- 5. Right-click to select or deselect the Net.



6. Select **Single Net** from the top drop-down menu. A **Single Net Coupling Coefficient** is displayed. It includes a few of the strongest couplings to each section.

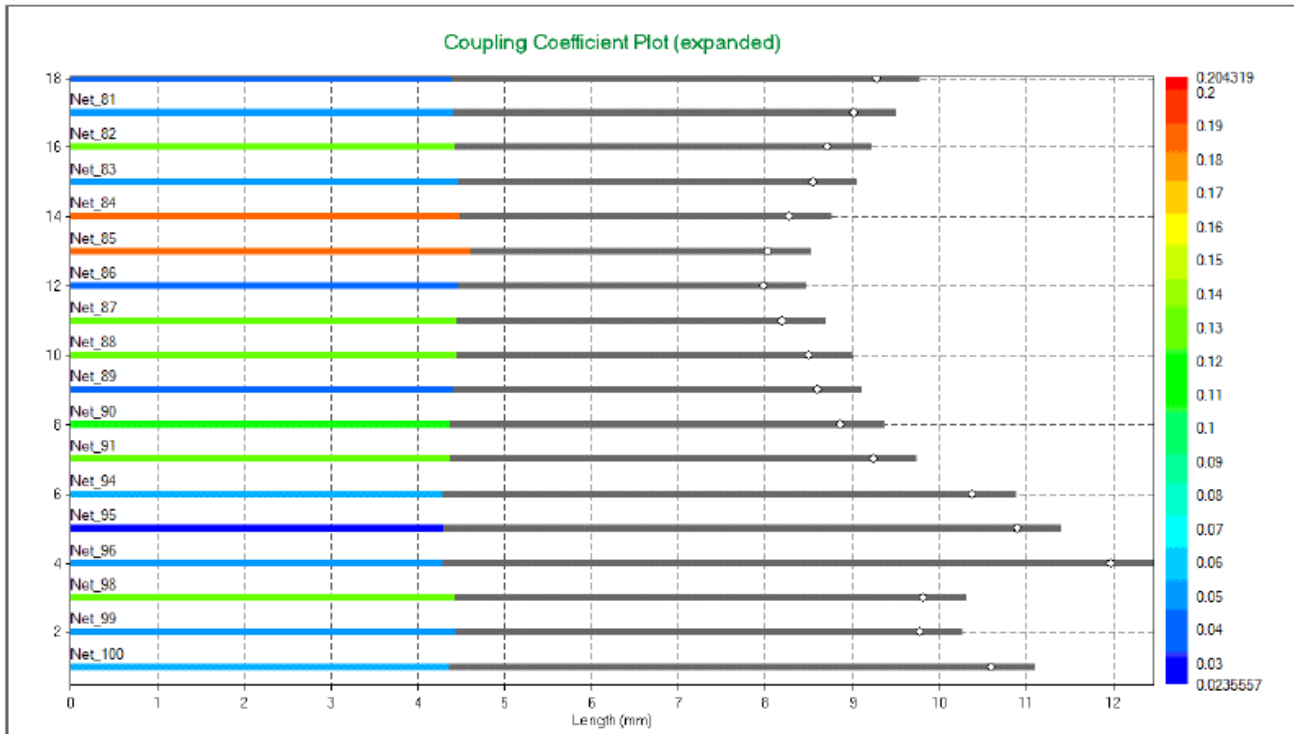
The same color is used for the same layer.

7. Place your mouse on a Curve. Detailed information about the Curve is displayed.



8. Click:
Coupling Coefficient Plot (expanded)
9. Select a Component Name in the **From:** drop-down list.
10. Select a Component Name in the **To:** drop-down list.

The strongest **Coupling Coefficient** for each Trace and Wirebond section is displayed (expanded) from the **Start Component** to the **End Component**.



11. Click:
Coupling Coefficient Table
12. Select a Component Name in the **From:** drop-down list.
13. Select a Component Name in the **To:** drop-down list.
The strongest Coupling Coefficient for each Trace and Wirebond section is listed with the table.
14. Choose a specific Net to view the detailed results.

Net	Length(mm)	Trace/wirebond Name	Length(mm)	% of its net length	Coupled Lines	Coupling Coefficient
Net_1	11.618	WireBond175_wb_u...	4.336	37.32%	WreBond67_wb_u1::Net_10	0.109
Net_2	10.779	Trace701::Net_1	0.427	3.68%		
Net_3	10.910	Trace700::Net_1	0.800	6.89%		
Net_4	11.713	Trace699::Net_1	3.146	27.08%		
Net_5	13.030	Trace698::Net_1	1.306	11.24%		
Net_6	11.956	Trace697::Net_1	0.548	4.72%		
Net_7	11.438	Trace239::Net_1	0.500	4.30%		
Net_8	11.014					
Net_9	10.584					
Net_10	10.224					

15. Click:

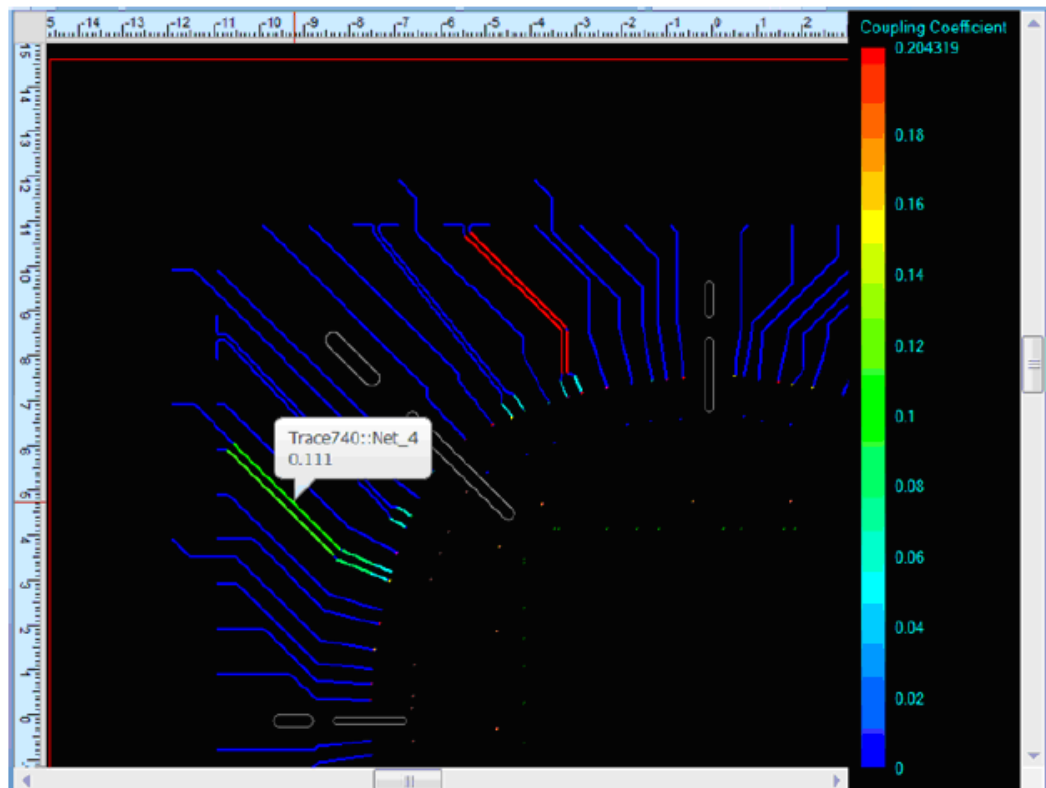
Coupling Coefficient in Layout

16. Select a Component Name in the **From:** drop-down list.

17. Select a Component Name in the **To:** drop-down list.

The strongest Coupling Coefficient of each Trace and Wirebond section is overlaid on the Layout.

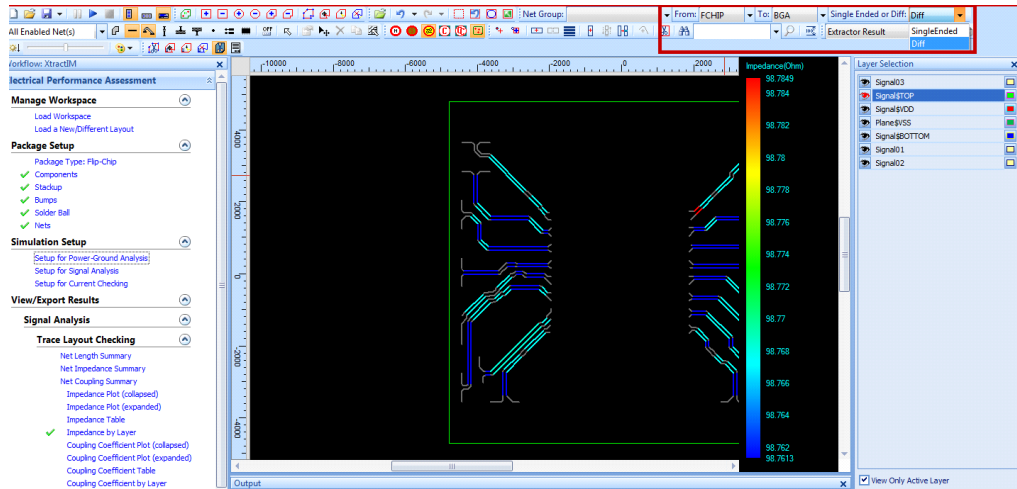
18. Move your cursor onto the Layout. The **Net Name and Coupling Coefficient** is shown.



Single-Ended and Diff. Pair Net Checking Switching

If there are differential pair signal nets defined and enabled in Net Manager, you can switch

the trace checking report and plot between single-ended and differential pair signal nets. The impedance and coupling coefficient table and plot can be switched by choosing **SingleEnded** or **Diff** from the **Single Ended or Diff** column.



Net Couplings

This feature is for Single-die Single-BGA package only. Using all Power and Ground Nets and Reference Nets, couplings report the:

- Mutual Inductance
- Mutual Capacitance
- Crosstalk among all Signal Nets

Every signal net can be considered as a single-ended net. Or, if differential pair exists, it can be considered as a whole in discussing crosstalk with other nets, i.e. Differential pair vs. Single-ended or another differential pair.

Net Coupling	⬆
Single-ended Based	⬆
Mutual Inductance and Capacitance	
Total NEXT Histogram	
Diffpair and Single-ended	⬆
Mutual Inductance and Capacitance	
Total NEXT Histogram	

Single-ended Based

1. Click:

Mutual Inductance and Capacitance (under Single-ended Based)

A table shows:

- Resistance
- Mutual Inductance and Capacitance
- Near-ended Crosstalk
- Total Near-ended Crosstalk of each Net as Victim
- Far-ended Crosstalk assuming the Rise Rime is 100 ps

Net i	Net j	Rij (mOhm)	Lij (nH)	Cij (pF)	NEXT (%)	Total NEXT (%)	FEXT (%)	Tr (ps)
Net_1	Net_1	271.466	6.77129	1.40194		8.56234		
Net_1	Net_10	0	0.673844	0.0543725	3.63607		-3.00417	100
Net_1	Net_9	0	0.433952	0.0181933	1.99271		-2.49417	100
Net_1	Net_8	0	0.254391	0	0.958141		-1.83376	100
Net_1	Net_11	0	0.160449	0	0.629086		-1.16111	100
Net_1	Net_7	0	0.123555	0	0.456147		-0.884778	100
Net_1	Net_12	0	0.0781773	0	0.310549		-0.566104	100
Net_1	Net_6	0	0.076406	0	0.280166		-0.547804	100
Net_1	Net_14	0	0.0263146	0	0.10684		-0.191491	100
Net_1	Net_16	0	0.0235187	0	0.096987		-0.172855	100
Net_1	Net_15	0	0.0232635	0	0.0956424		-0.169863	100
Net_2	Net_2	257.394	6.36301	1.3223		8.51554		
Net_2	Net_13	0	0.671347	0.0534184	3.83533		-3.01932	100
Net_2	Net_12	0	0.419509	0.0188933	2.09137		-2.38551	100
Net_2	Net_14	0	0.161937	0	0.679096		-1.17841	100
Net_2	Net_11	0	0.161062	0	0.651631		-1.16554	100
Net_2	Net_15	0	0.0884465	0	0.375694		-0.645807	100
Net_2	Net_10	0	0.0877581	0	0.352181		-0.635655	100
Net_2	Net_9	0	0.0378359	0	0.149022		-0.272522	100
Net_2	Net_16	0	0.0315619	0	0.13446		-0.23197	100
Net_2	Net_8	0	0.0315379	0	0.122435		-0.227339	100
Net_2	Net_17	0	0.0299699	0	0.124315		-0.217064	100
Net_3	Net_3	259.857	6.4191	1.33039		7.15329		
Net_3	Net_18	0	0.371279	0.0182203	1.87086		-2.05114	100
Net_3	Net_19	0	0.331794	0.0120447	1.58481		-2.01174	100
Net_3	Net_20	0	0.22027	0	0.88141		-1.59764	100
Net_3	Net_17	0	0.21053	0.00616289	0.991971		-1.31208	100
Net_3	Net_16	0	0.106873	0	0.453499		-0.78548	100
Net_3	Net_21	0	0.103712	0	0.41142		-0.754952	100

Change Rise Time

Use the following steps to change the Rise Time.

1. Select several lines.
2. Click in the corner of **Tr (ps)**. One cell is enabled for change.
3. Change the enabled cell to a new number.
4. Click **Enter**. All selected lines are changed.

FEXT (%)	Tr (ps)
3.00417	100
-2.49417	100
-1.83376	100
-1.16111	100
-0.884781	100
-0.566105	100
-0.547804	100
-0.191492	100
-0.172854	100
-0.169863	100
3.01932	100
-2.38551	100
-1.17841	100
-1.16554	100

FEXT (%)	Tr (ps)
-3.00417	100
-2.49417	100
-1.83376	100
-1.16111	100
-0.884778	100
-0.566104	100
-0.547804	100
-0.191491	100
-0.172855	100
-0.169863	100
-3.01932	100
-2.38551	100
-1.17841	100
-1.16554	100

FEXT (%)	Tr (ps)
-1.50209	200
-1.24708	200
-0.916881	200
-0.580556	200
0.442391	200
0.283052	200
-0.273902	200
-0.0957459	200
-0.0864272	200
-0.0849313	200
3.01932	100
-2.38551	100
-1.17841	100
-1.16554	100

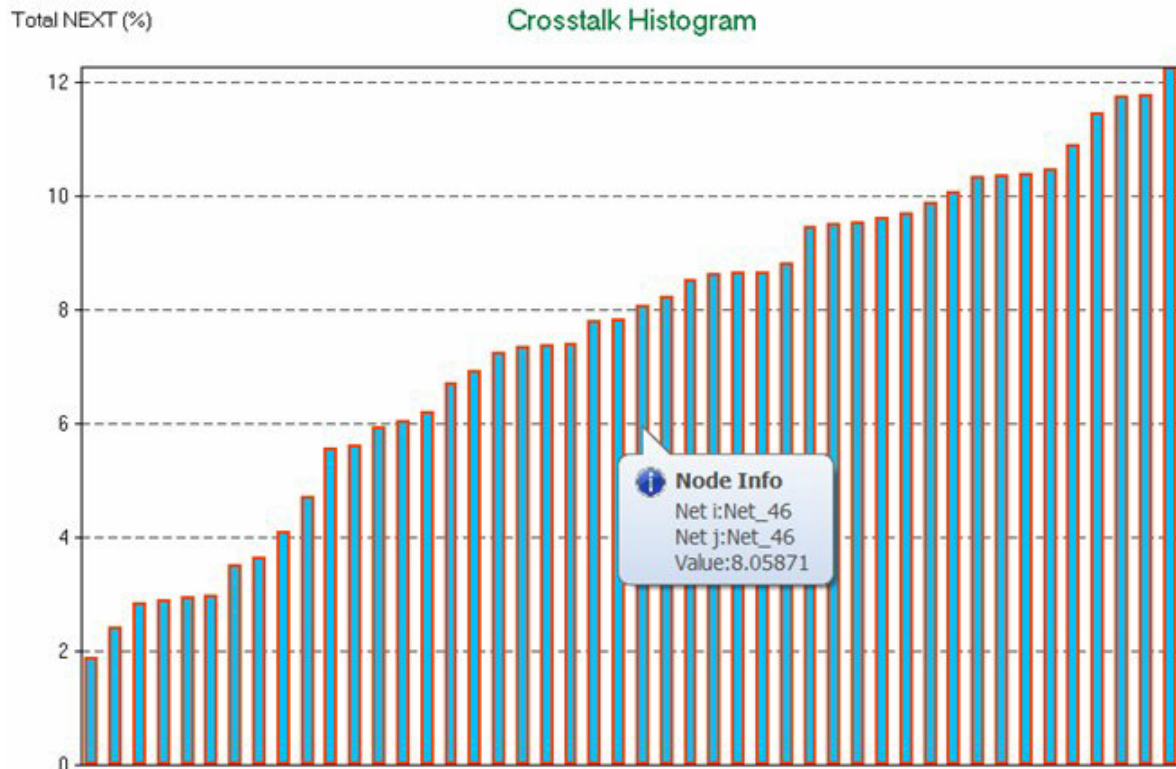
Histogram View

1. Click:

Total NEXT Histogram View

The total NEXT for each Net as victim is plotted left-to-right and smallest-to-largest.

2. Stop your mouse on a Bar. Detailed information for the Bar is displayed.



Diffpair and Single-ended

1. Click

Mutual Inductance and Capacitance (Under Diffpair and Single-ended)

A table shows:

- Nets: differential pair are shown a whole unit
- Resistance (*see definition of R for differential pair*)
- Mutual Inductance and Capacitance
- Near-ended Crosstalk
- Total Near-ended Crosstalk of each Net (or differential pair) as Victim
- Far-ended Crosstalk assuming the Rise Rime is 100 ps

Net i	Net j	Rij (mOhm)	Lij (nH)	Cij (pF)	NEXT (%)	Total NEXT (...)	FEXT (%)	Tr (pS)
Diff_L_05N-L_05P	Diff_L_05N-L_05P	832.524	10.8655	0.583		9.64		
Diff_L_05N-L_05P	Single_2	0	0.7882	0.097	5.57		1.51	100
Diff_L_05N-L_05P	Diff_L_08N-L_08P	0	0.4329	0.126	3.34		0.42	100
Diff_L_05N-L_05P	Single_1	0	0.1097	0.006	0.74		0.58	100
Diff_L_08N-L_08P	Diff_L_08N-L_08P	1213.52	12.6047	0.971		4.65		
Diff_L_08N-L_08P	Diff_L_05N-L_05P	0	0.4329	0.126	3.09		-0.07	100
Diff_L_08N-L_08P	Single_2	0	0.1642	0.015	0.79		-0.51	100
Diff_L_08N-L_08P	Single_1	0	0.1180	0.015	0.76		-0.30	100
Single_1	Single_1	217.127	3.5739	0.711		2.30		
Single_1	Single_2	0	0.1343	0.006	0.88		-0.64	100
Single_1	Diff_L_08N-L_08P	0	0.1180	0.015	0.73		-0.25	100
Single_1	Diff_L_05N-L_05P	0	0.1097	0.006	0.68		0.51	100
Single_2	Single_2	345.325	5.5739	0.942		7.12		
Single_2	Diff_L_05N-L_05P	0	0.7882	0.097	5.32		1.13	100
Single_2	Diff_L_08N-L_08P	0	0.1642	0.015	0.84		-0.61	100
Single_2	Single_1	0	0.1343	0.006	0.96		-0.73	100

Change Rise Time

Use the following steps to change the Rise Time (Similar to Single-ended Based).

1. Select several lines.
2. Click in the corner of **Ts (ps)**. One cell is enabled for change.
3. Change the enabled cell to a new number.
4. Click **Enter**. All selected lines are changed.

Histogram View

Use the following steps to show the Histogram View (Similar to Single-ended Based).

1. Click:

Total NEXT Histogram View

The total NEXT for each Net as victim is plotted left-to-right and smallest-to-largest.

2. Stop your mouse on a Bar. Detailed information for the Bar is displayed.

Insertion and Return Loss

Insertion and Loss is reported for all Signal Nets by using Power and Ground Nets as Reference Nets. This feature is only available for Single-die Single-BGA packages.

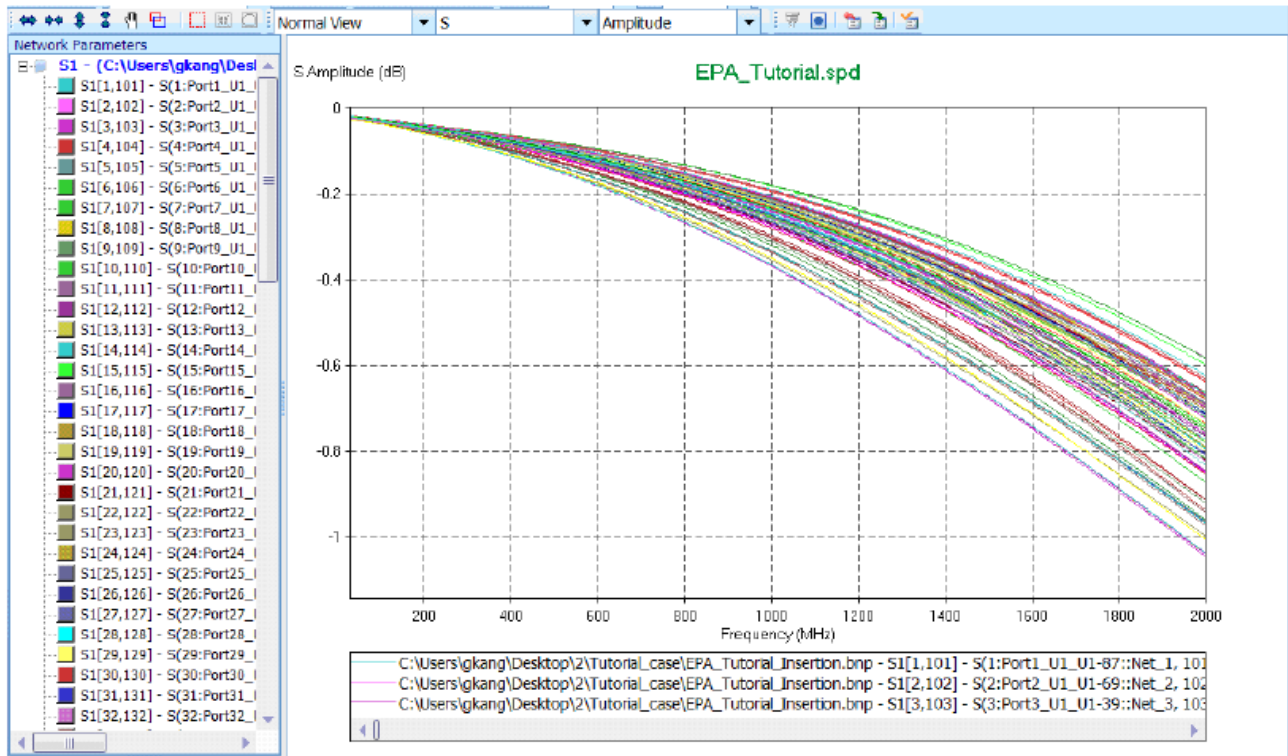
Insertion and Return Loss

- Insertion Loss
- Return Loss

1. Click:

Insertion Loss

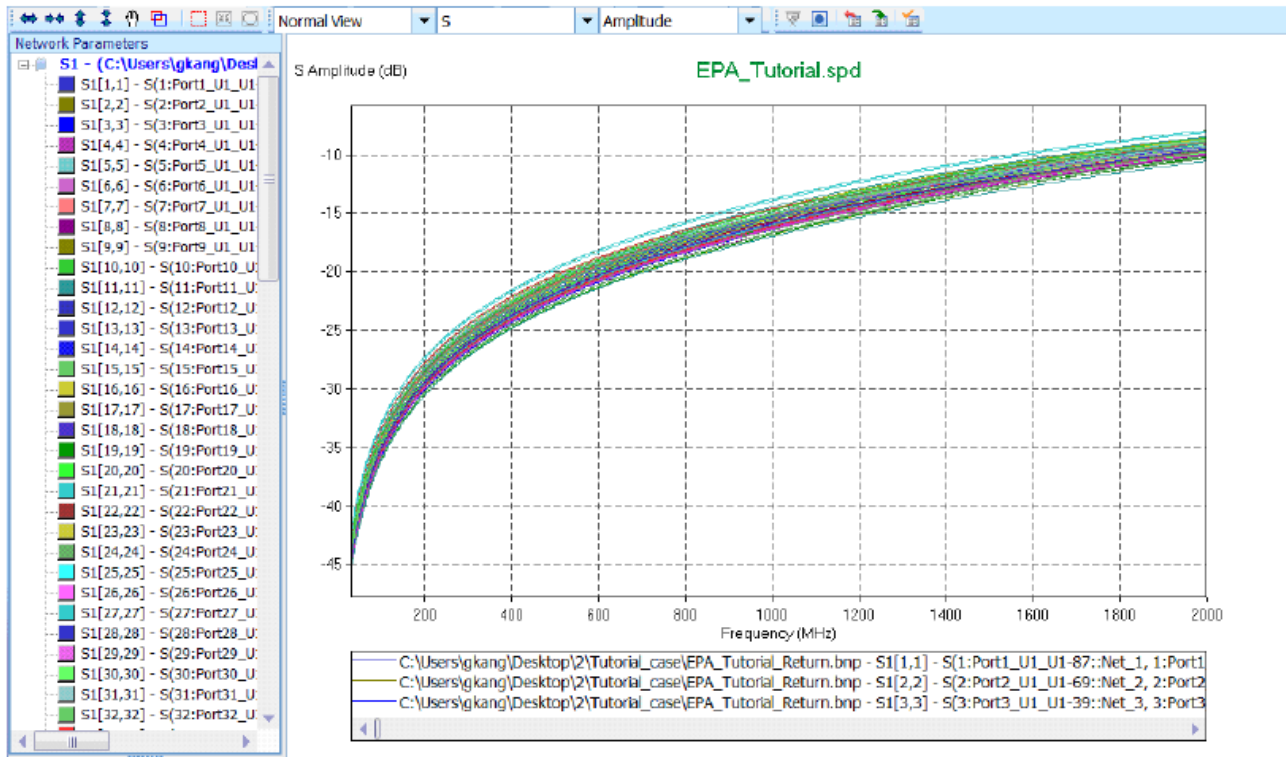
The Insertion Loss for all Signal Nets is shown.



- Click:

Return Loss

The Return Loss for all Signal Nets is shown.



Current Checking

The Workspace lists options to display results. Click on the desired option.

Current Checking

- Via Counts
- Via Current Histogram
- Via Current by Layer
- Via Current Table
- Voltage Distribution by Layer
- Plane Current Density by Layer

- Click:

Via Counts

The **Via Counts Table** is shown for each Power / Ground Net. The number is classified at each Via starting layer.

Net	Signal\$M1->Signal\$VSS	Signal\$VSS->Signal\$VDD	Signal\$VDD->Signal\$M4
VSS	28	256	256
VDD_1	4	4	14
VDD_2	4	4	14
VDD_3	4	4	14
VDD_4	4	4	14

2. Click:

Via Current Table

A detailed table showing **Current Density** is displayed. The table includes:

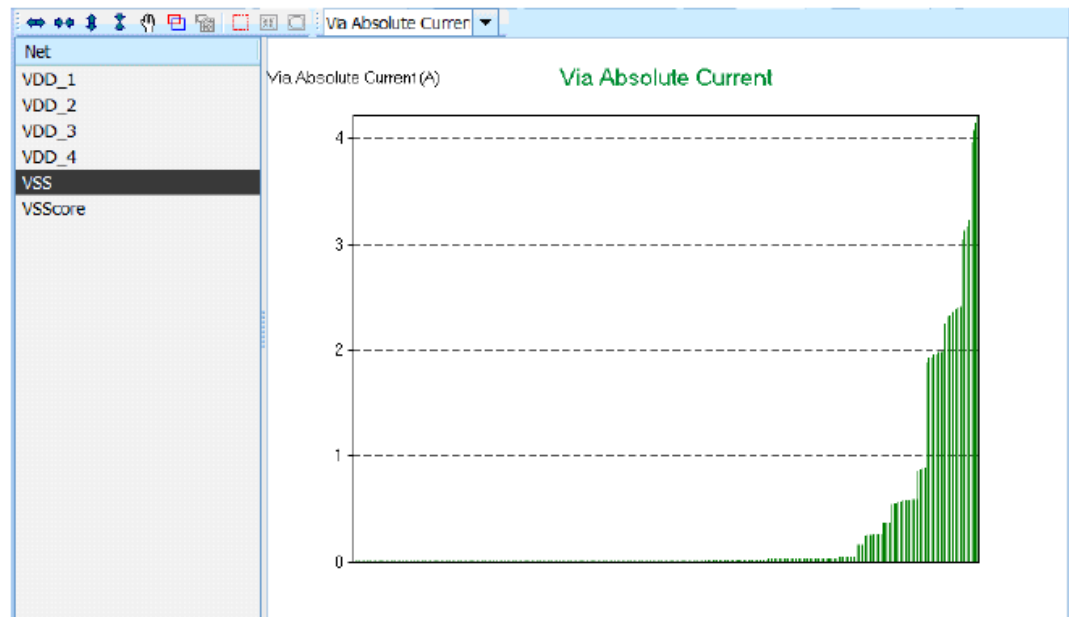
- Via Name
- Via Net
- Actual Current
- Current Density
- X,Y Coordinates
- Start Layer
- Upper Node Name
- End Layer
- Lower Node Name
- Padstack

Via Name	Net	Current (A)	Current Density (A/mm ²)	PosX (mm)	PosY (mm)	StartLayer	Upper Node	EndLayer	Lower Node	PadStack
Via254::VDD_1	VDD_1	-0.0807358	2.5699	-13.8536	-6.8536	Signal\$VDD	Node2598:...	Signal\$M4	Node477:...	via4003
Via264::VDD_1	VDD_1	-0.0620086	1.9738	-13.8536	-8.8536	Signal\$VDD	Node2600:...	Signal\$M4	Node493:...	via4003
Via273::VDD_1	VDD_1	-0.0372965	1.18719	-13.8536	-10.8536	Signal\$VDD	Node2602:...	Signal\$M4	Node507:...	via4003
Via302::VDD_1	VDD_1	-0.0134064	0.42674	-13.8536	-12.8536	Signal\$VDD	Node2604:...	Signal\$M4	Node561:...	via4003
Via334::VDD_1	VDD_1	-0.0133563	0.425144	-13.8536	12.8536	Signal\$VDD	Node2620:...	Signal\$M4	Node593:...	via4003
Via343::VDD_1	VDD_1	-0.0371082	1.18119	-13.8536	10.8536	Signal\$VDD	Node2622:...	Signal\$M4	Node607:...	via4003
Via370::VDD_1	VDD_1	-0.0618354	1.96828	-13.8536	8.8536	Signal\$VDD	Node2624:...	Signal\$M4	Node657:...	via4003
Via378::VDD_1	VDD_1	-0.0803316	2.55703	-13.8536	6.8536	Signal\$VDD	Node2626:...	Signal\$M4	Node669:...	via4003
Via388::VDD_1	VDD_1	-0.0935236	2.97695	-13.8536	4.8536	Signal\$VDD	Node2628:...	Signal\$M4	Node685:...	via4003

3. Click:

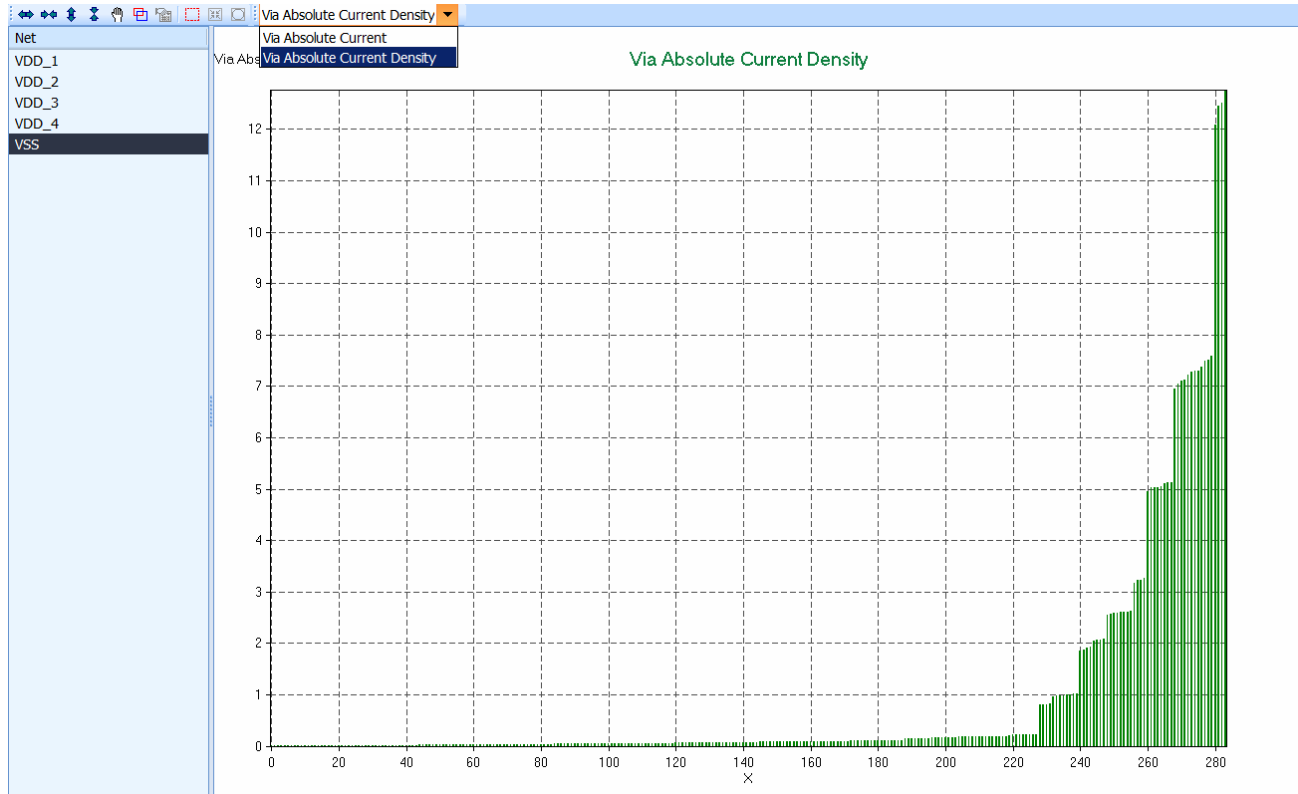
Via Current Histogram View

The **Via Absolute Current** window appears.



4. For each Net, the **Via Current** is plotted from the smallest (left) to the largest (right), click:
Net Name
The **Via Current** is changed.

- 5. Select **Via Absolute Current Density**.
It is plotted from the smallest (left) to the largest (right)
- 6. Click the desired Net Name.
The via current density is changed.



7. Click:

Current Checking > Via Current in Layout

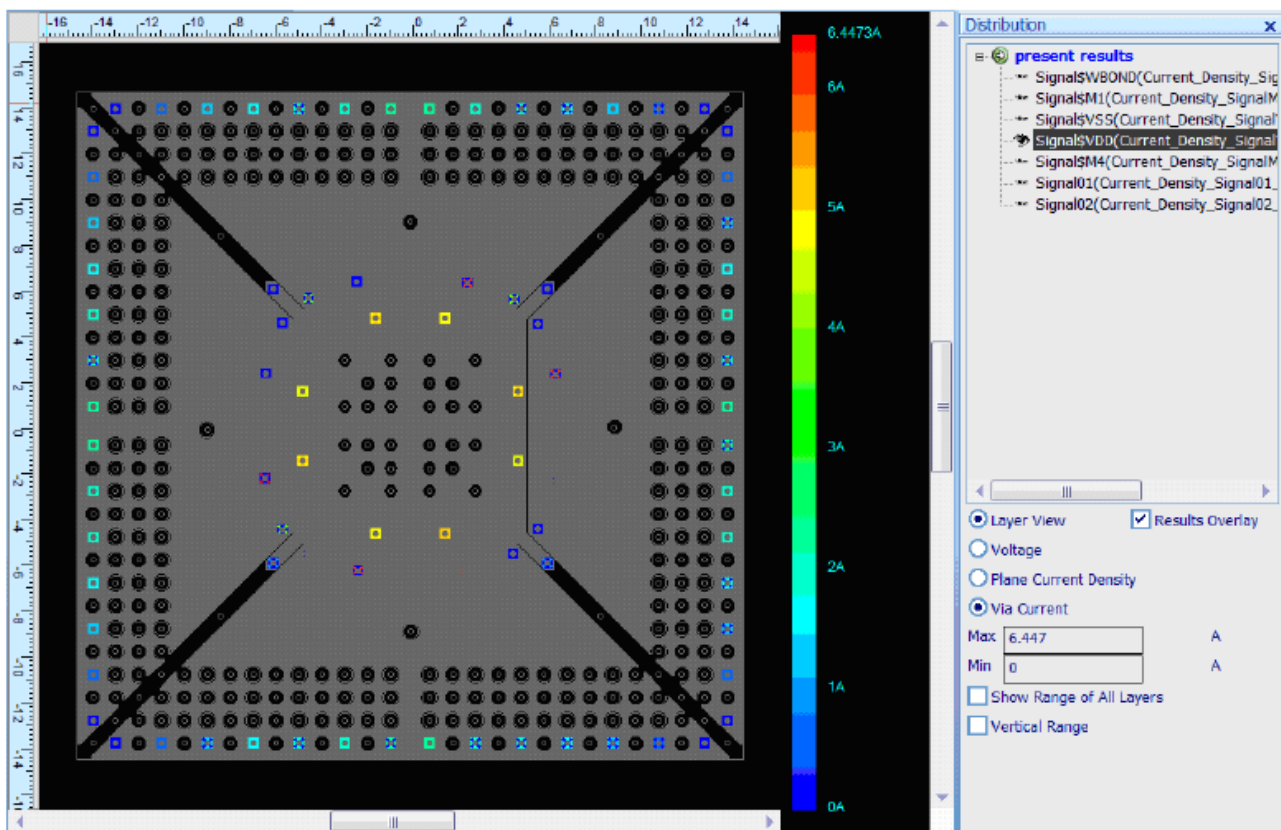
The **Via Current** is overlaid on the layout to quickly identify the location. The **Color Map** is used as a current value scale.

8. In the **Present Results** window, click on a Layer Name. The Layer changes to reflect the selected Layer Name.

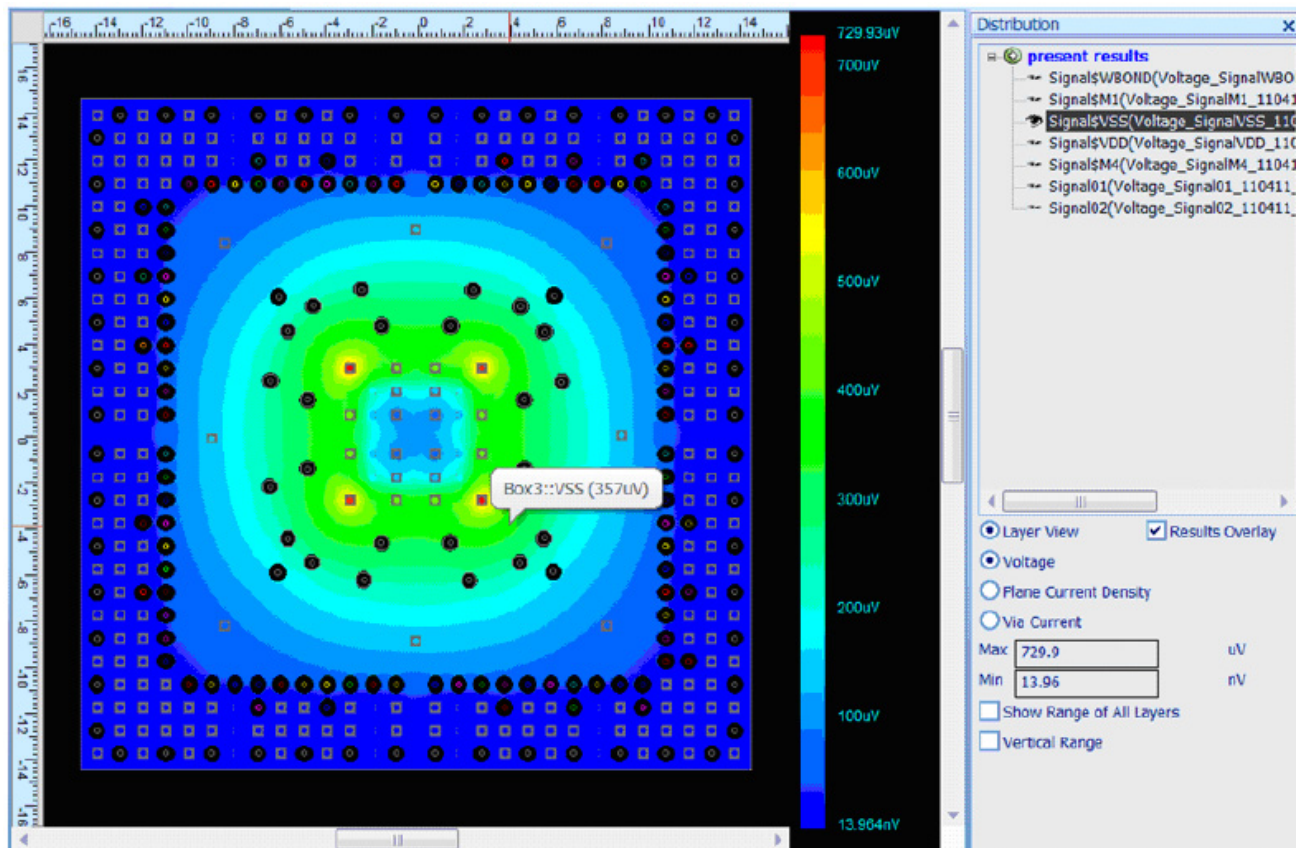
9. Select or Deselect:

Results Overlay

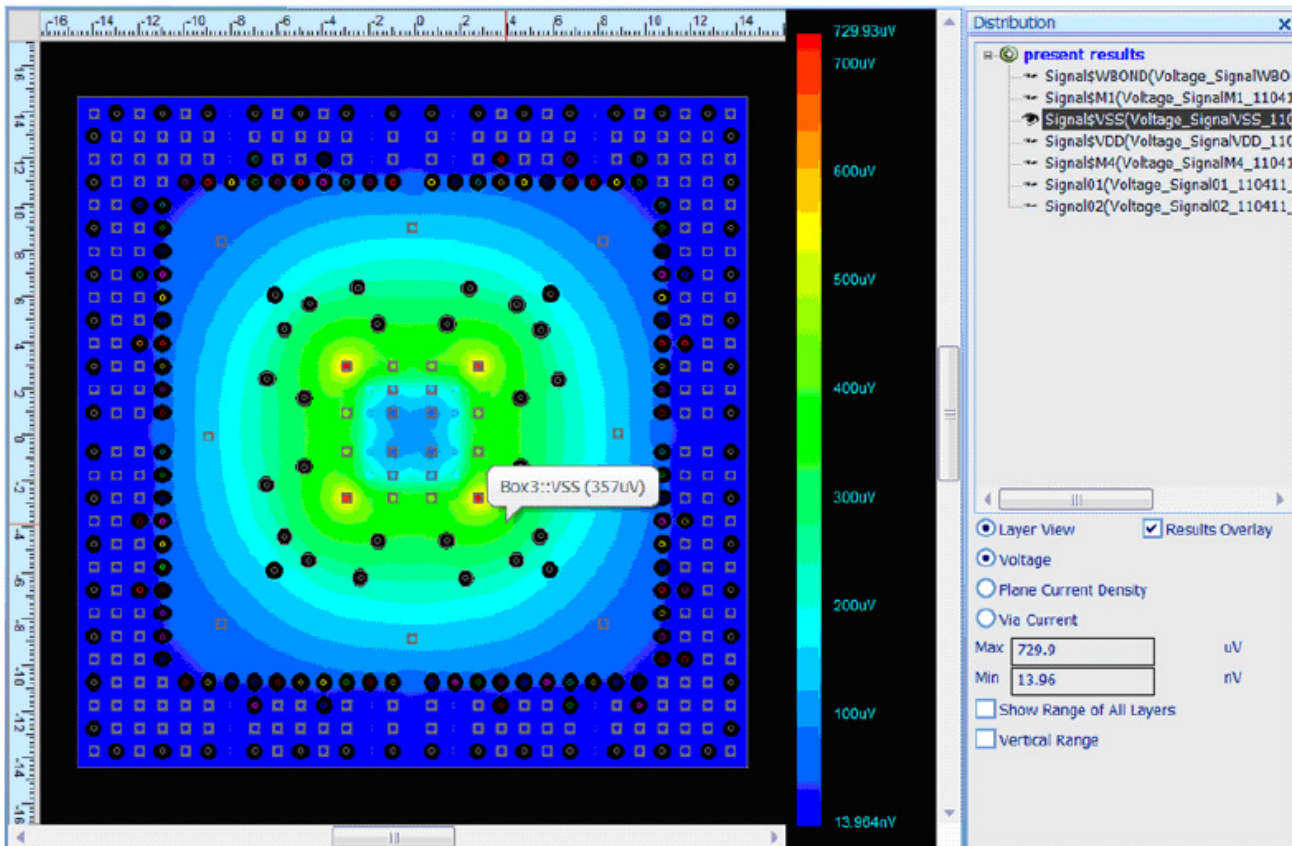
The display changes between overlay results and the physical layout.



10. Click:
Current Checking > Voltage Distribution in Layout
Voltage distribution (IR Drop) is overlaid for each layer.
11. Select a different layer. The display changes according to the selected layer.
12. Stop the mouse cursor on the display, The actual value is shown.

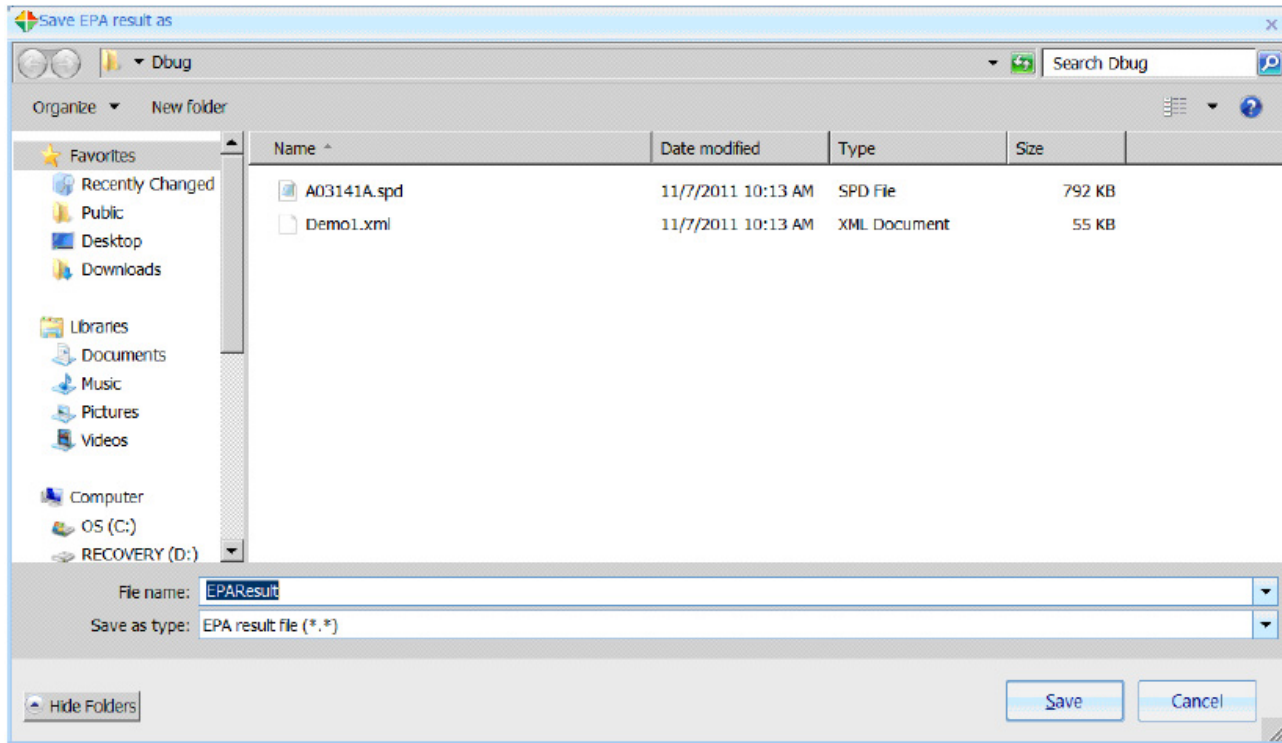


13. Click:
Current Density Checking > Plane Current Density in Layout
Each **Plane Current Density** is overlaid on each layer.
14. Select a different layer. The display changes according to the selected layer.
15. Stop the mouse cursor on the display, The actual value is shown.



Save Results

1. Click:
Workspace > Save Results
2. Input a file name.
3. Click **OK** to save the results.



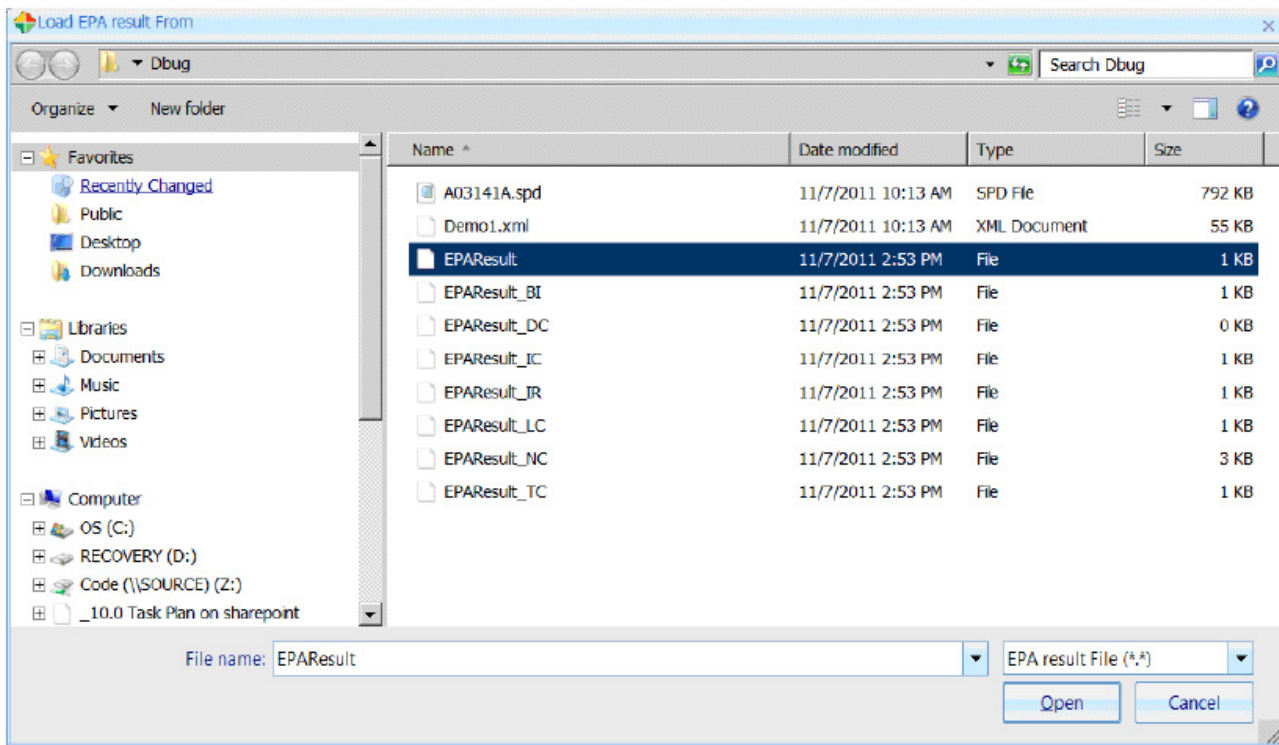
Load Results

1. Launch XtractIM.
2. Load in the Workspace file.
3. Load in the SPD file.

4. Click:

Workspace > Load Results

The Load Result window opens.



5. Select the file you want to open.

6. Click **Open** to view the results.

All results can be displayed with the same operation.

NOTE!

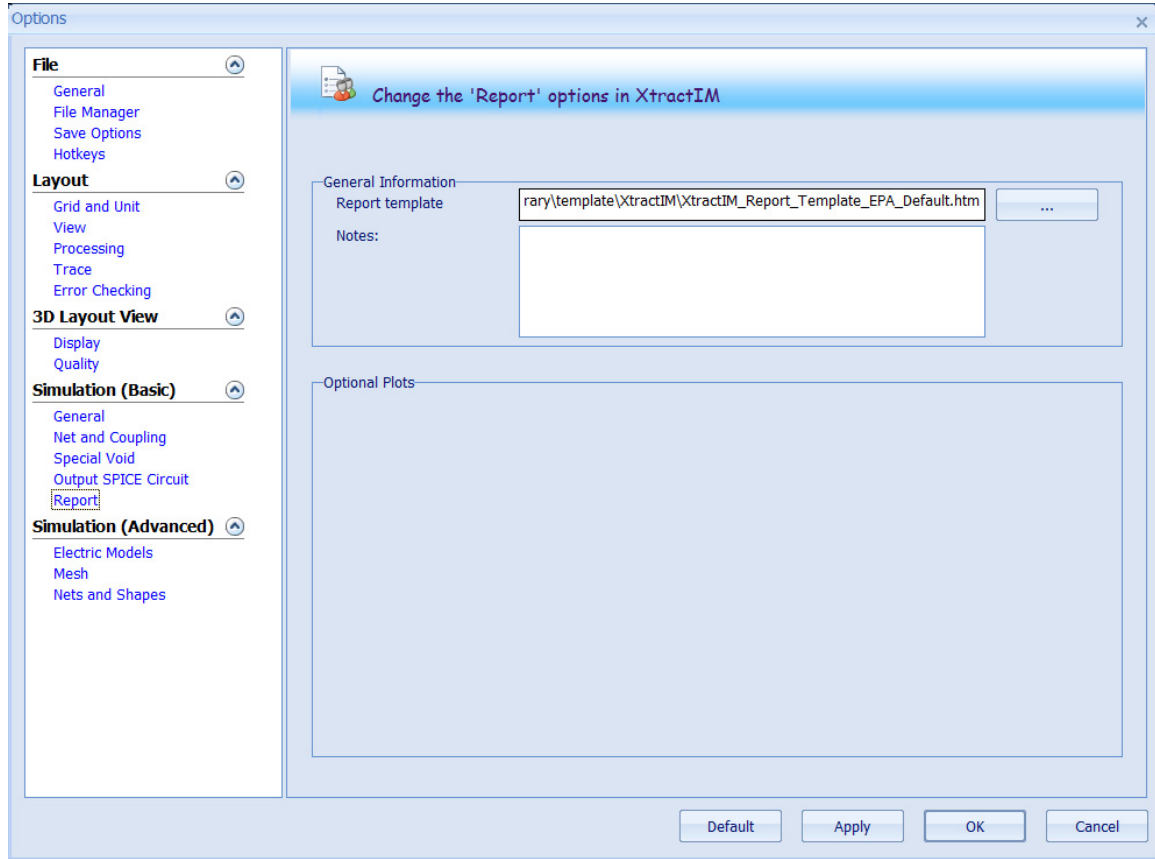
If the XML and SPD file is not loaded before loading the saved results, all overlay features will not work.

Create Report

1. Select

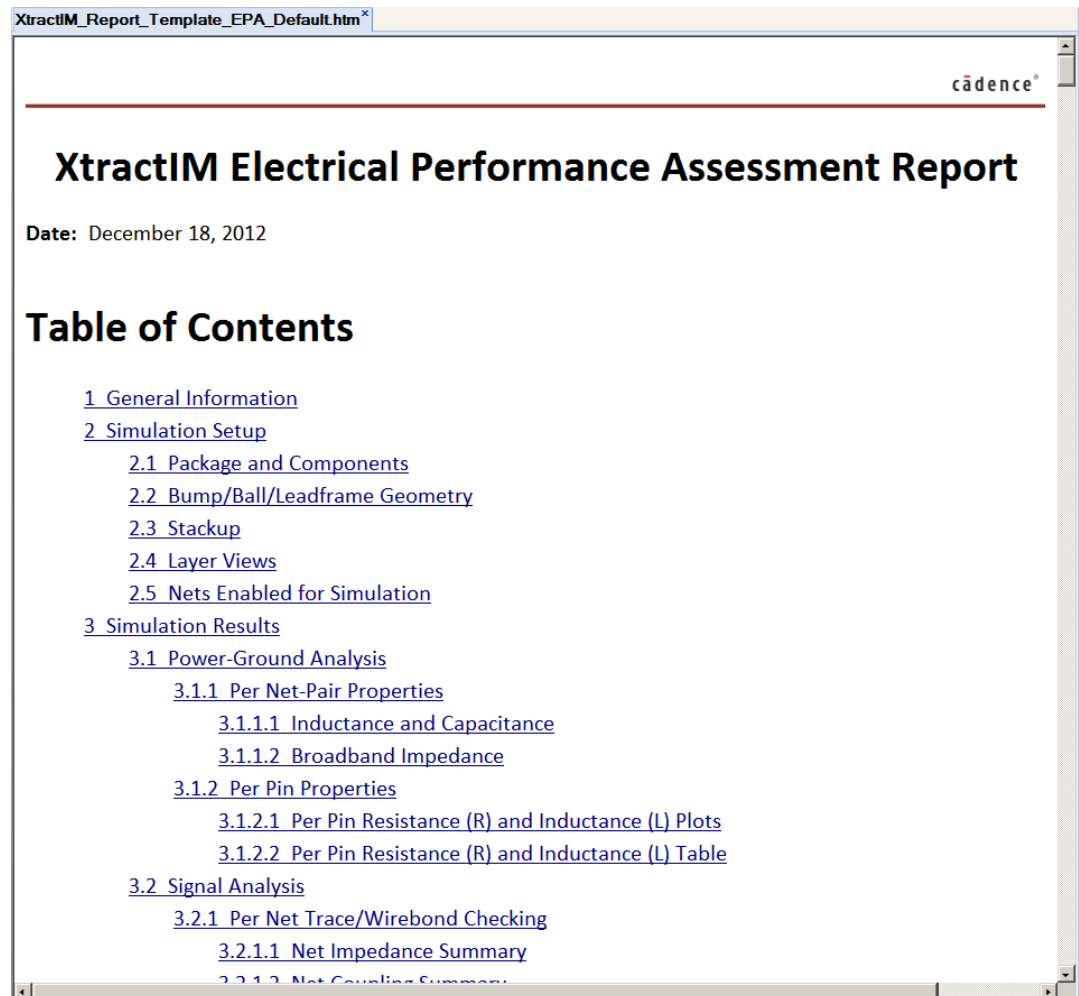
View / Export Results > Report

The following window pops up. A default *.htm template is loaded and highlighted.

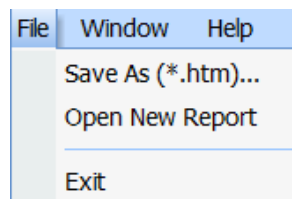


2. Click **OK**.

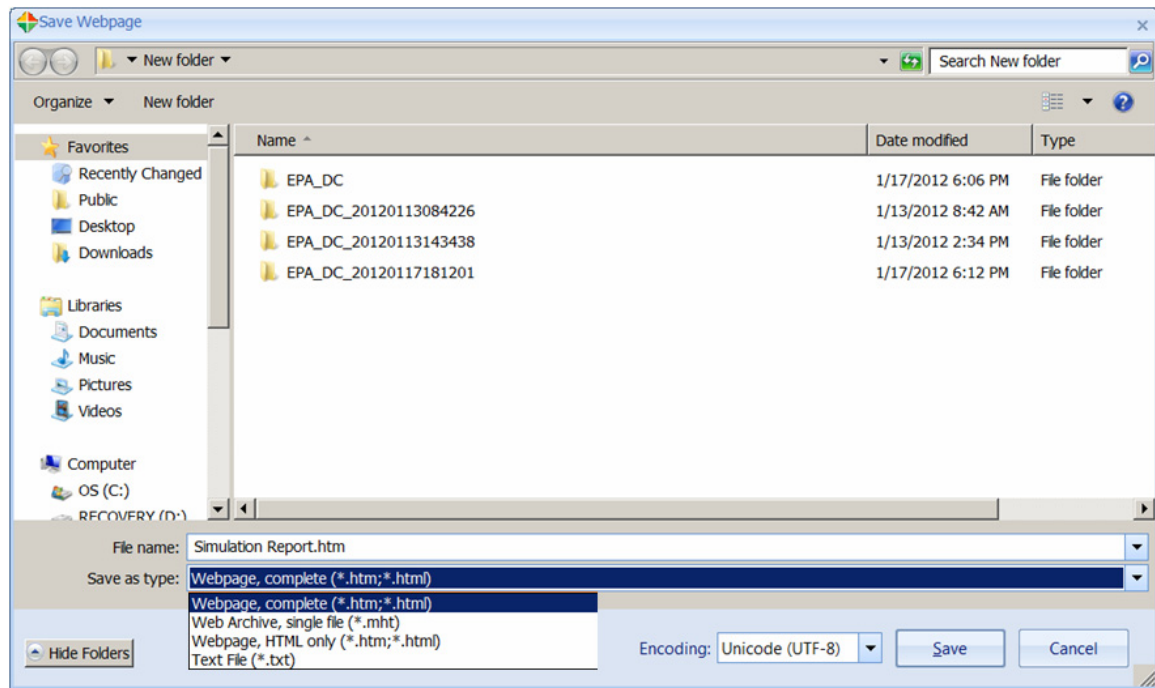
The report file is created.



3. To save the report file as *.htm, *.html, or *.mht format, select File > Save As (*.htm)...




The **Save Webpage** window opens.



4. Select the location, file name and type.
5. Click **Save** to save the file.

Load Previously Saved Results

1. Click  to open an XtractIM workspace file *.ximx.

Save Result
[Load Result](#)
[Report](#)

2. Click **Load Result** in the **Workflow** pane.
The result should be related with above *.ximx project.
3. Click **Report**.
A new report can be created.

SUMMARY OF ELECTRICAL PERFORMANCE ASSESSMENT FEATURES

DISTRIBUTION SYSTEM	FEATURES		BGA PACKAGES	LEADFRAME
Power and Ground	Power-Ground Net Pair	Inductance & Capacitance	Single-die Multi-die Stacked-BGA	No
		Broadband Impedance	Single-die Single-BGA	No
	Per-pin Property	Inductance & Resistance	Single-die Multi-die Stacked-BGA	No
	DC Current Density	Current Density	Single-die Single-BGA	No
Signal	Layout Checking	Trace / Wirebond Impedance & Coupling Coefficient	Single-die Multi-die Stacked BGA	Single-die Multi-die
	Net Couplings	Mutual LC and NEXT	Single-die Single-BGA	No
	Insertion and Return Loss	Insertion & Return Loss	Single-die Single-BGA	No

TCL Command Support for Workspace Setup

This chapter takes you through the steps to use TCL command for workspace setup in the XtractIM tool.

PREPARE FOR THE SIMULATION

Get the following issues ready before you begin the simulation.

- The Bump diameters, length, heights and conductivity
- The Stackup information
- The files to be simulated in SPD format

LESSON ONE: RUNNING TCL COMMAND FOR WORKSPACE SETUP

Introduction

TCL (Tool Command Language) scripts can be used to configure and automate frequently used command in Allegro Sigrity tools. They can also be launched outside the Sigrity tools in batch mode to automate company design flows.

New TCL command is developed to support workspace setting in XtractIM.

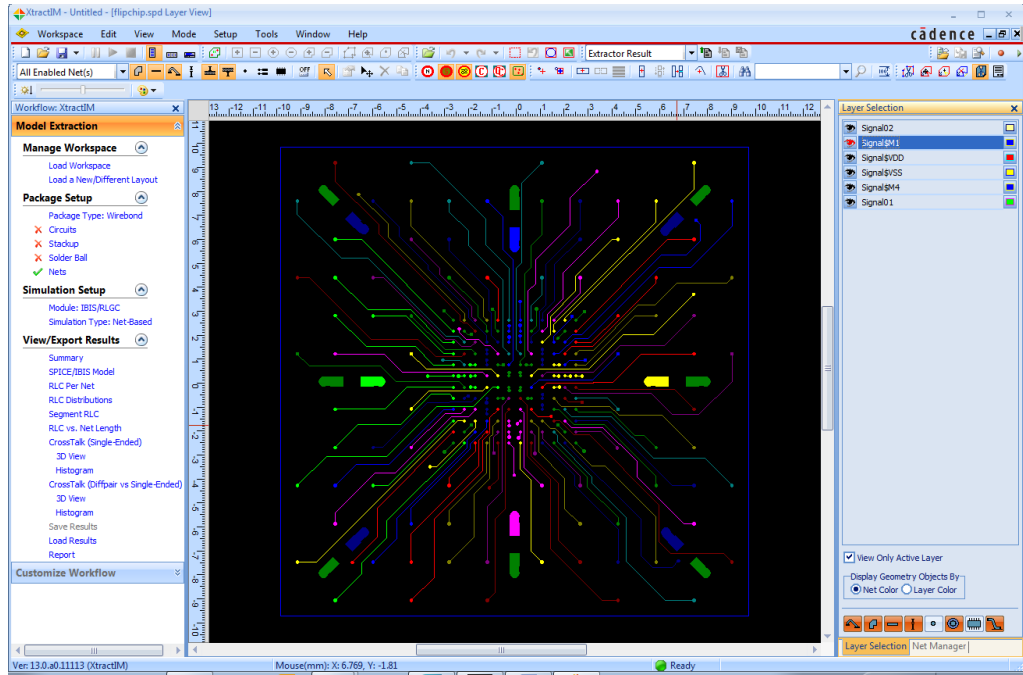
For the other existing TCL command, please refer to *Tcl_Scripting_Reference.pdf* in <ASI_INSTALL_DIR>\Update3\Doc\Common Documents\ for details.

Three package types are used in this tutorial to practice the new TCL command.

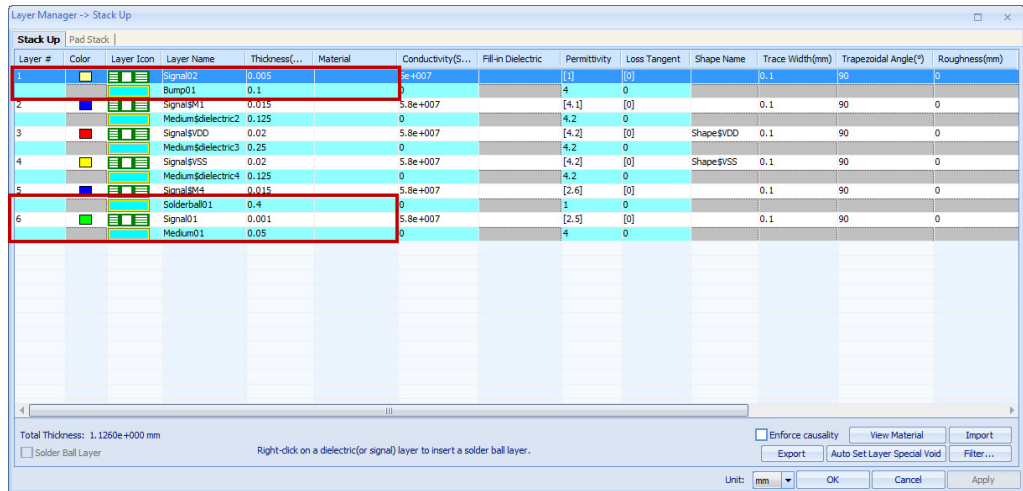
Single-Die BGA Package Sample

1. Load *flipchip.spd*.

It is typically located in <ASI_INSTALL_DIR>\Update3\SpeedXP\Samples\XtractIM\Single-Die_Sample_files\.



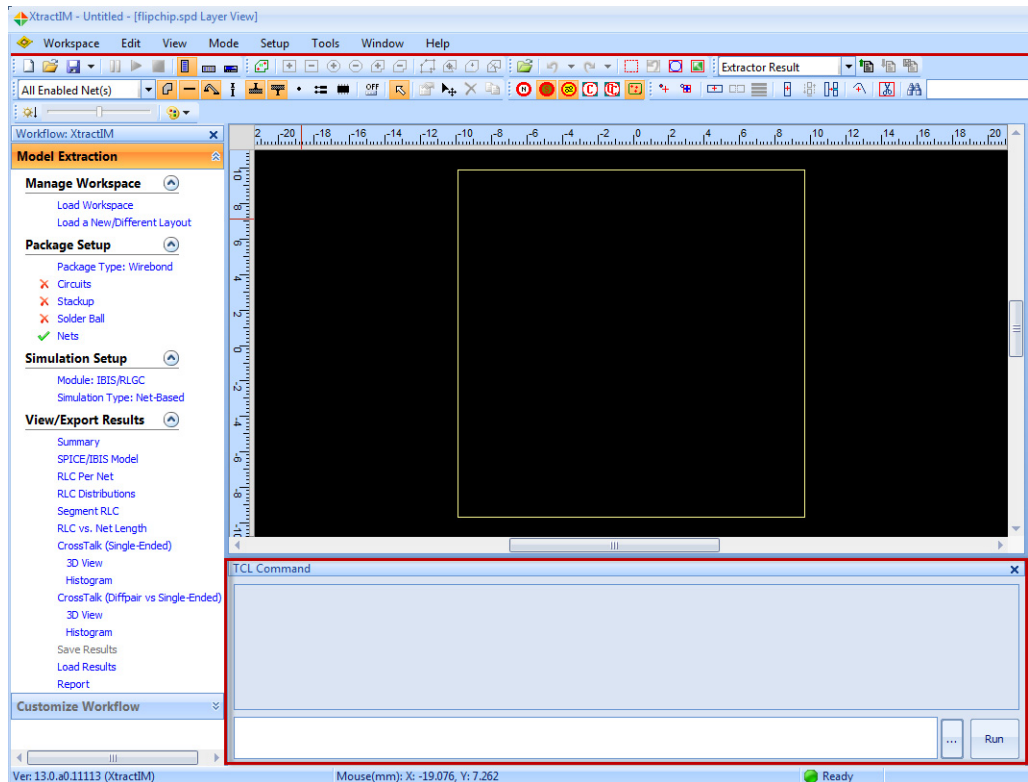
2. Remove the existing bump and solder ball layers if any before running TCL command.



A fresh example is like the following.



3. Choose View > Pane > TCL Command to open the TCL command input console.



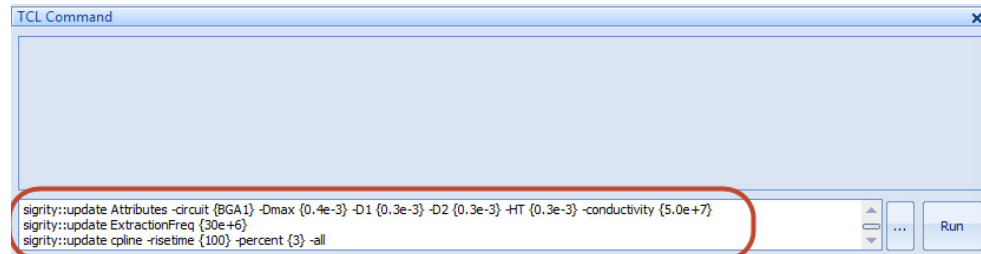
4. Copy the following TCL command to the **TCL Command** console.


```
sigity::update PackageType -dieType {0} -bgaType {0} -attachType {1}
sigity::update Circuits -dieCkts {U1} -boardCkts {BGA1}
sigity::add Layer {bump} -above {Signal$M1} -circuit {U1}
```

```

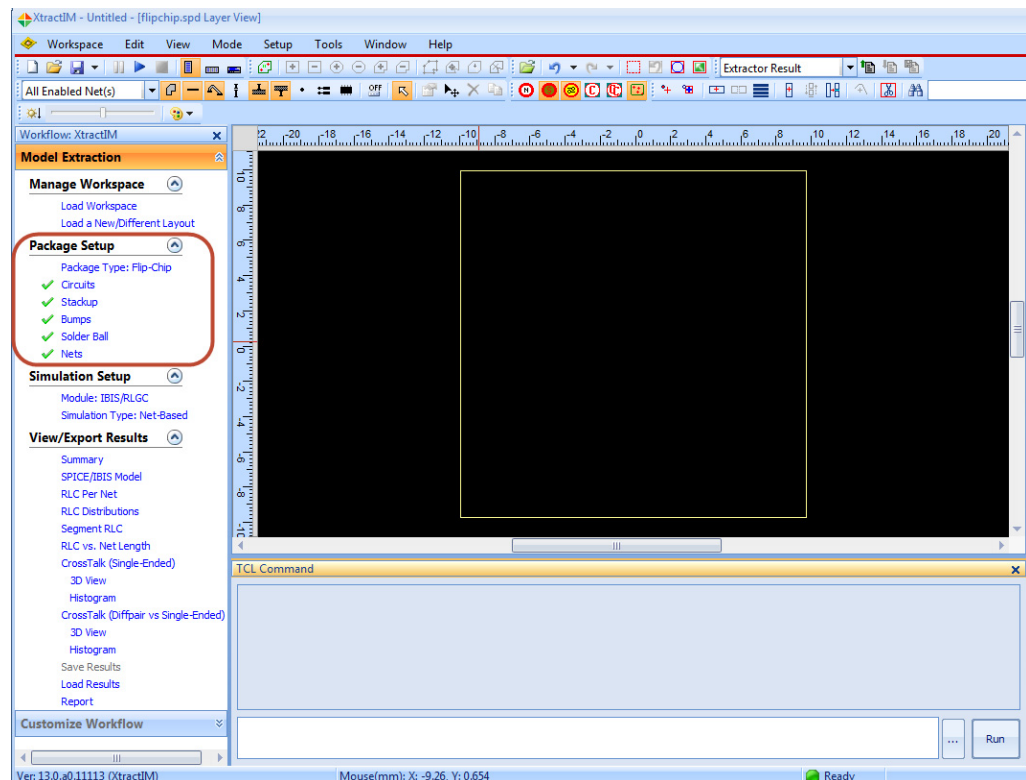
sigrity::add Layer {ball} -under {Signal$M4} -circuit {BGA1}
sigrity::update Attributes -circuit {U1} -Dmax {0.1e-3} -D1 {0.08e-3} -D2 {0.08e-3} -HT {0.1e-3} -conductivity {5.0e+7}
sigrity::update Attributes -circuit {BGA1} -Dmax {0.4e-3} -D1 {0.3e-3} -D2 {0.3e-3} -HT {0.3e-3} -conductivity {5.0e+7}
sigrity::update ExtractionFreq {30e+6}
sigrity::update cpline -risetime {100} -percent {3} -all

```



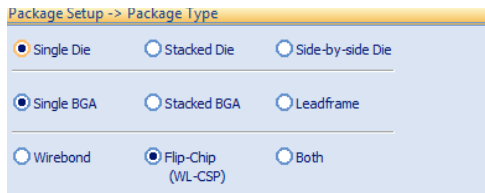
5. Click the **Run** button in the **TCL Command** console.

The **Package Setup** is automated.

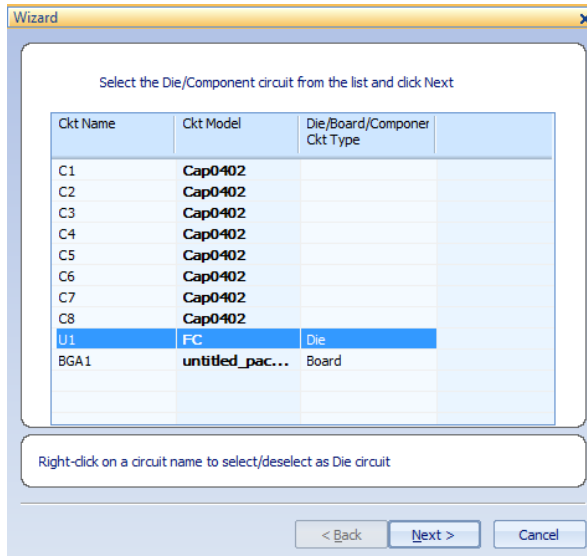


The relationship between individual TCL command and the corresponding Package Setup is described as follows.

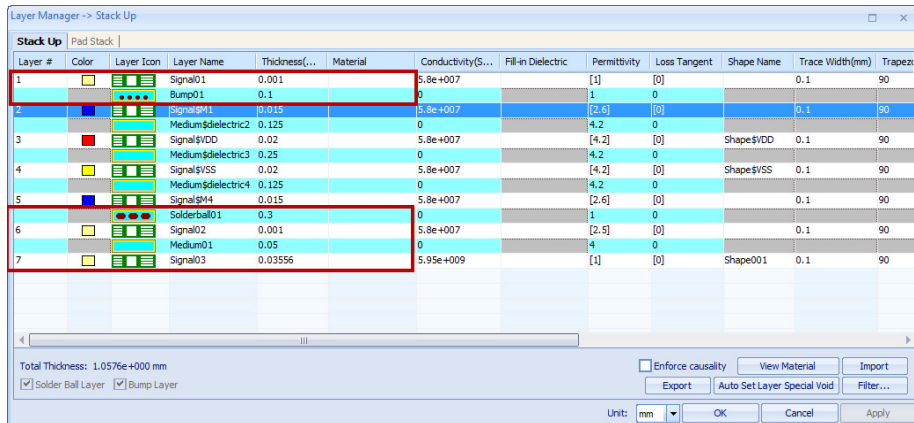
- sigrity::update PackageType -dieType {0} -bgaType {0} -attachType {1}



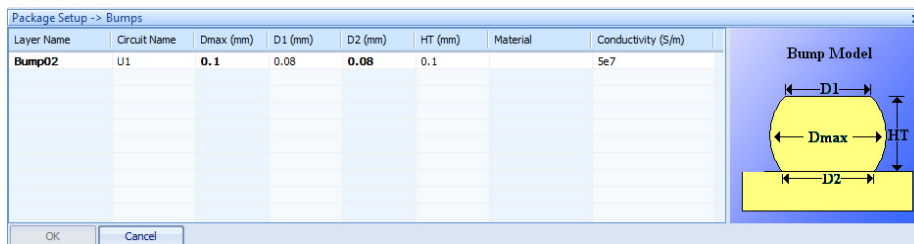
- sigrity::update Circuits -dieCkts {U1} -boardCkts {BGA1}



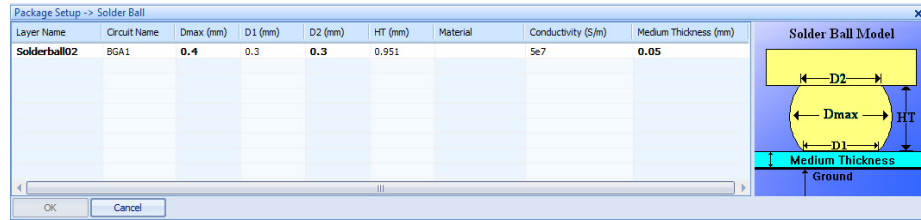
- sigrity::add Layer {bump} -above {Signal\$M1} -circuit {U1}
- sigrity::add Layer {ball} -under {Signal\$M4} -circuit {BGA1}



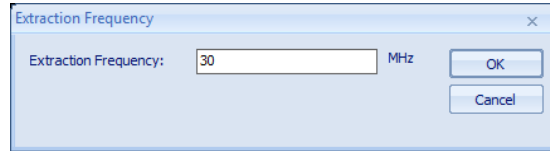
- sigrity::update Attributes -circuit {U1} -Dmax {0.1e-3} -D1 {0.08e-3} -D2 {0.08e-3} -HT {0.1e-3} -conductivity {5.0e+7}



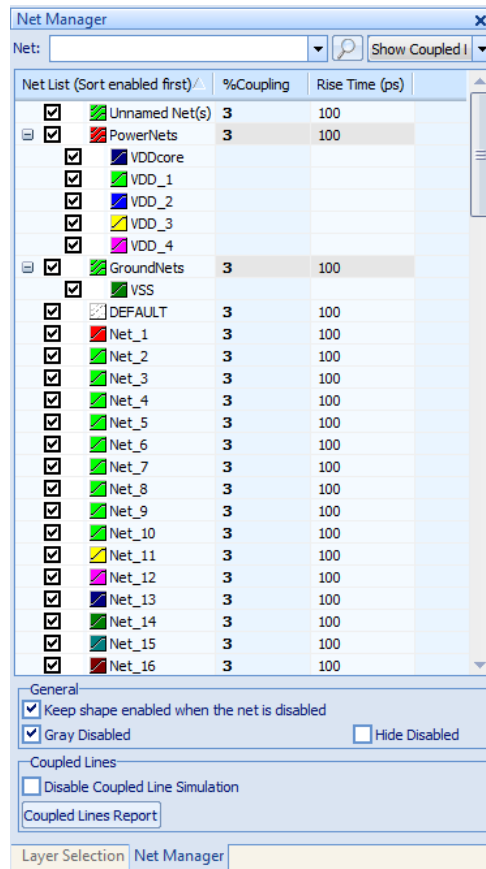
- `sigrity::add Layer {ball} -under {Signal$M4} -circuit {BGA1}`



- `sigrity::update ExtractionFreq {30e+6}`



- `sigrity::update cpline -risetime {100} -percent {3} -all`



6. The TCL command used above can also be prepared in a `.tcl` file.

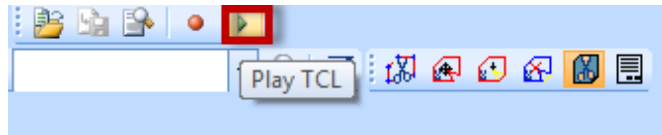
```

FlipChip.tcl - Notepad
File Edit Format View Help
sigrity::update Packagetype -dietype {0} -bgatype {0} -attachtype {1}
sigrity::update Circuits -dieckts {U1} -boardckts {BGA1}
sigrity::add Layer {bump} -above {signal$M1} -circuit {U1}
sigrity::add Layer {ball} -under {signal$M4} -circuit {BGA1}
sigrity::update Attributes -circuit {U1} -Dmax {0.1e-3} -D1 {0.08e-3} -D2 {0.08e-3} -HT {0.1e-3} -conductivity {5.0e+7}
sigrity::update Attributes -circuit {BGA1} -Dmax {0.4e-3} -D1 {0.3e-3} -D2 {0.3e-3} -HT {0.3e-3} -conductivity {5.0e+7}
sigrity::update ExtractionFreq {30e+6}
sigrity::update cpline -risetime {100} -percent {3} -all
    
```

7. Click the **Open a TCL file** icon to load in the prepared *.tcl file



8. Click the **Play TCL** icon to run the prepared TCL command.



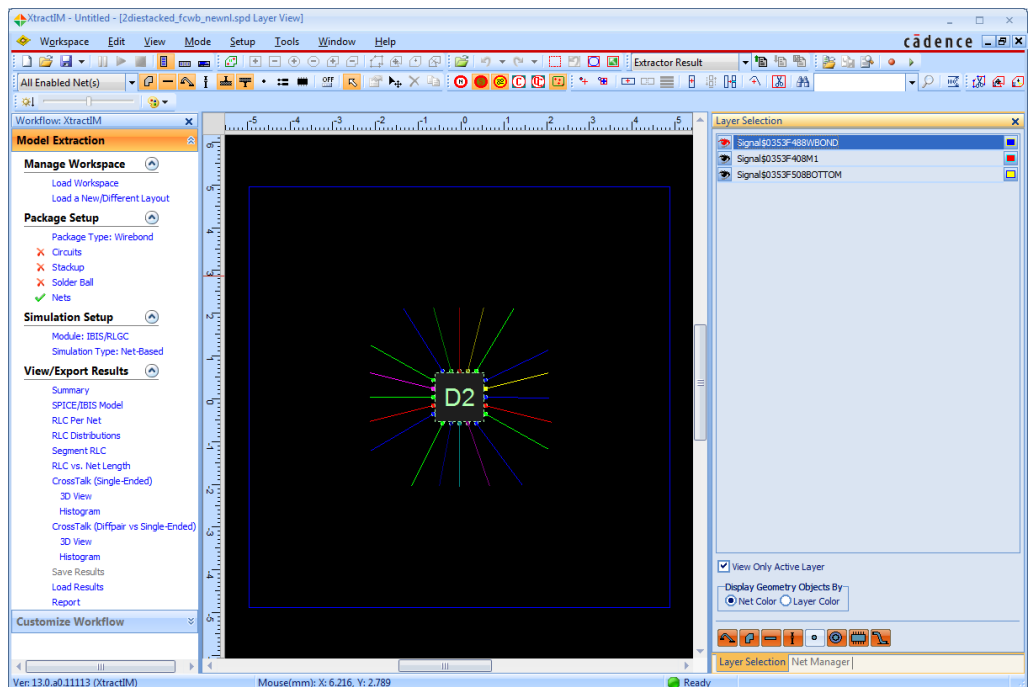
The same result will come out as in *Step 5*.

Multiple-Die BGA Package Sample

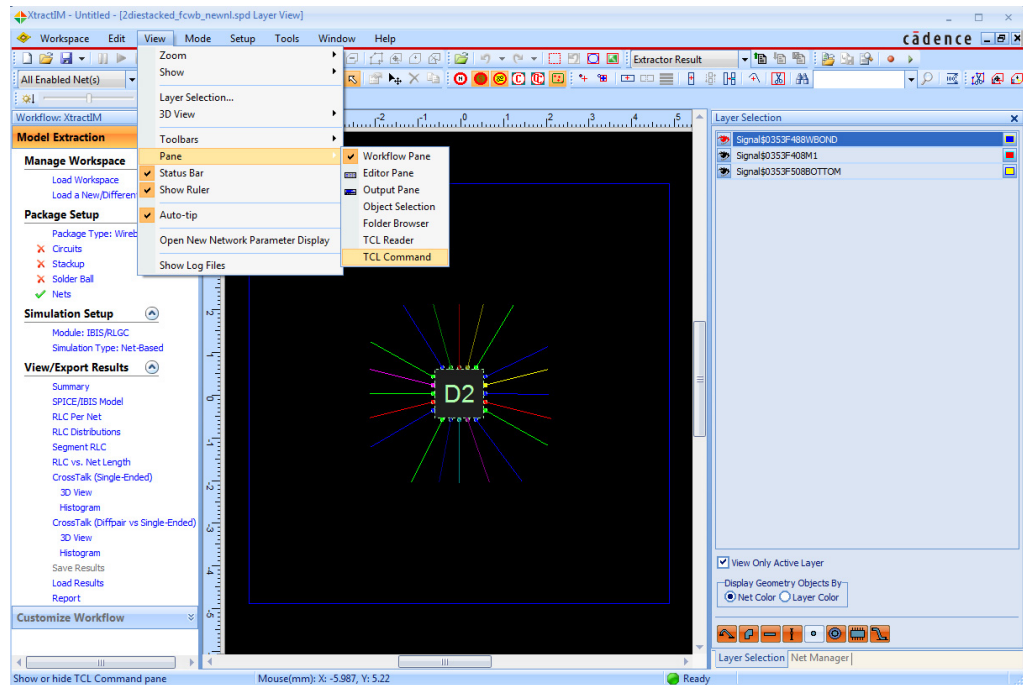
1. Load *2diestacked_fcwb_newnl.spd*.

It is typically located in <ASI_INSTALL_DIR>\Update3\SpeedXP\Samples\XtractIM\Single-Die_Sample_files\.

A wirebond die is placed above a flipchip die on a BGA package.

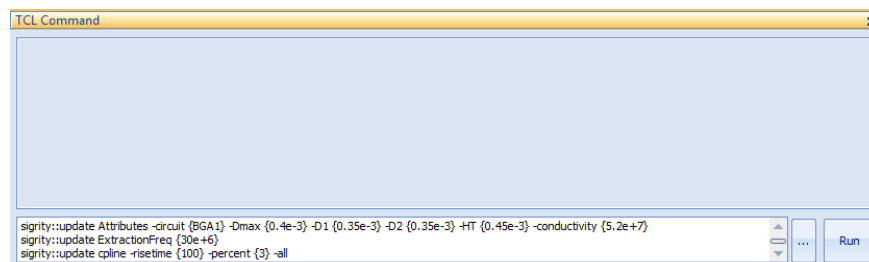


- Choose **View > Pane > TCL Command** to open the TCL command input console.

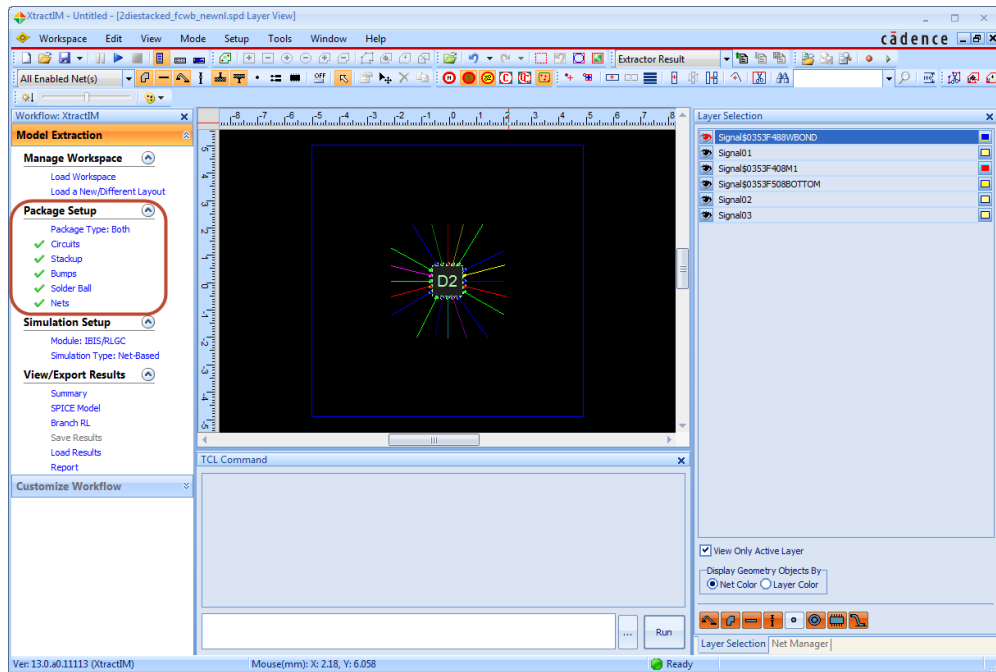


- Copy the following TCL command to the **TCL Command** console.

```
sigrity::update PackageType -dieType {1} -bgaType {0} -attachType {3}
sigrity::update Circuits -dieCkts {D1} -boardCkts {BGA1} -wbCkts {D2}
sigrity::add Layer {bump} -above {Signal$0353F408M1} -circuit {D1}
sigrity::add Layer {ball} -under {Signal$0353F508BOTTOM} -circuit {BGA1}
sigrity::update Attributes -circuit {D1} -Dmax {0.12e-3} -D1 {0.10e-3} -D2 {0.10e-3} -HT
{0.08e-3} -conductivity {5.0e+7}
sigrity::update Attributes -circuit {BGA1} -Dmax {0.4e-3} -D1 {0.35e-3} -D2 {0.35e-3} -
HT {0.45e-3} -conductivity {5.2e+7}
sigrity::update ExtractionFreq {30e+6}
sigrity::update cpline -risetime {100} -percent {3} -all
```

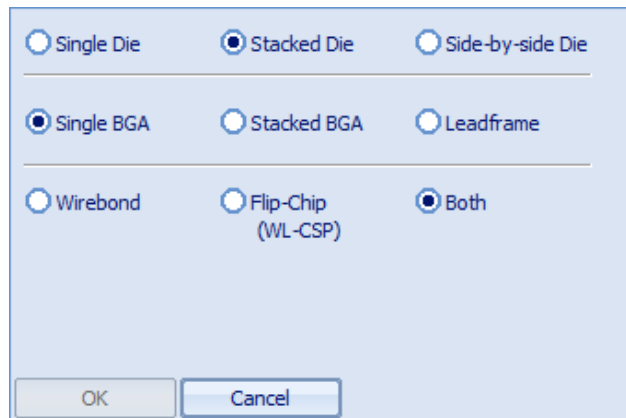


- Click the **Run** button in the **TCL Command** console.
The **Package Setup** is automated.

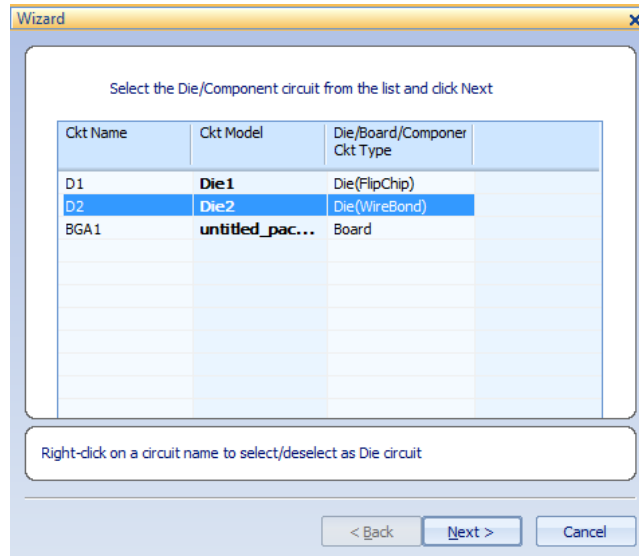


The relationship between individual TCL command and the corresponding Package Setup is described as follows.

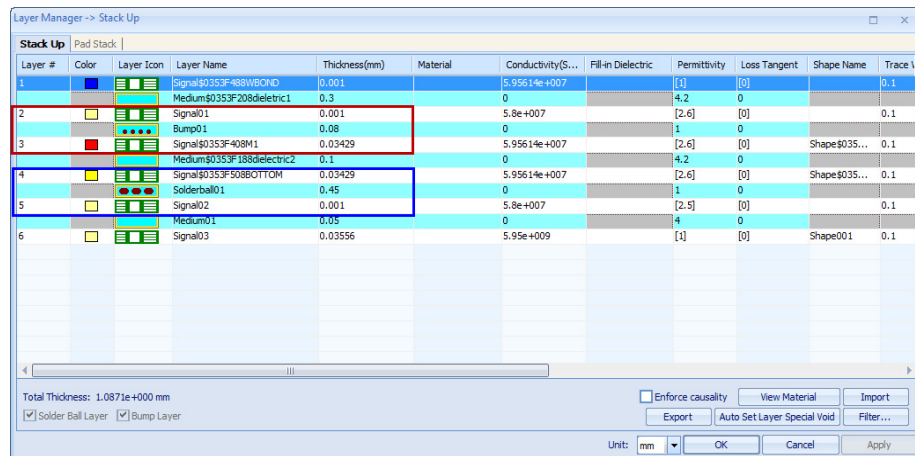
- `sigrity::update PackageType -dieType {1} -bgaType {0} -attachType {3}`



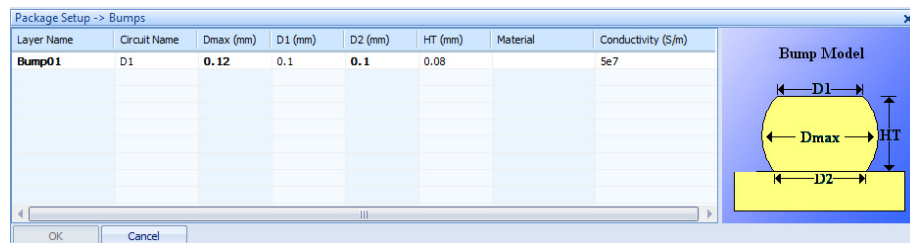
- `sigrity::update Circuits -dieCkts {D1} -boardCkts {BGA1} -wbCkts {D2}`



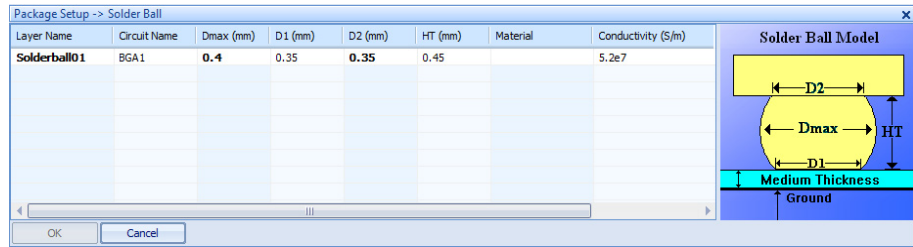
- sigrity::add Layer {bump} -above {Signal\$0353F408M1} -circuit {D1}
- sigrity::add Layer {ball} -under {Signal\$0353F508BOTTOM} -circuit {BGA1}



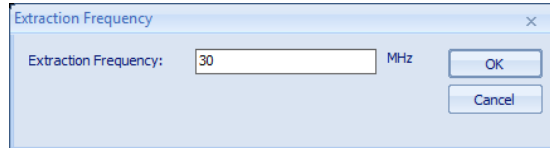
- sigrity::update Attributes -circuit {D1} -Dmax {0.12e-3} -D1 {0.10e-3} -D2 {0.10e-3} -HT {0.08e-3} -conductivity {5.0e+7}



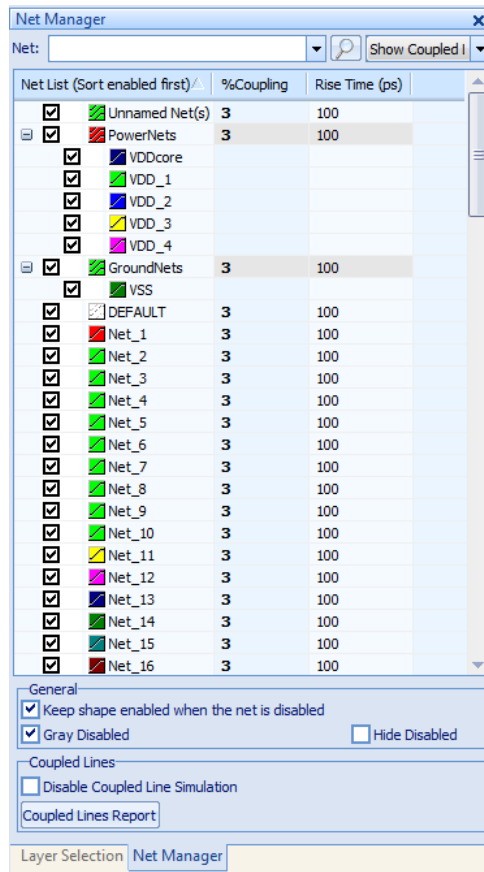
- sigrity::update Attributes -circuit {BGA1} -Dmax {0.4e-3} -D1 {0.35e-3} -D2 {0.35e-3} -HT {0.45e-3} -conductivity {5.2e+7}



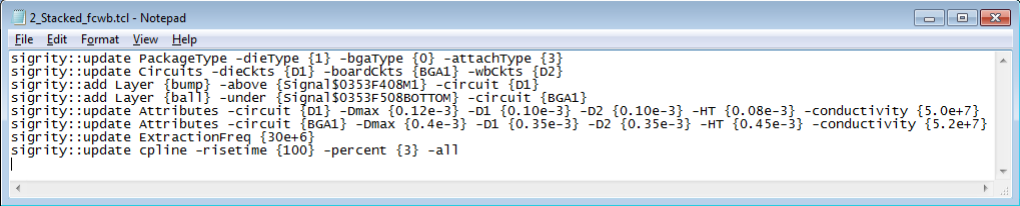
- `sigrity::update ExtractionFreq {30e+6}`



- `sigrity::update cpline -risetime {100} -percent {3} -all`



5. The TCL command used above can also be prepared in a `.tcl` file.



```

2_Stacked_fcwb.tcl - Notepad
File Edit Format View Help
sigrity::update PackageType -dietype {1} -bgatype {0} -attachtype {3}
sigrity::update Circuits -dieckts {D1} -boardckts {BGAI} -wbckts {D2}
sigrity::add Layer {bump} -above {Signal$0353F408M1} -circuit {D1}
sigrity::add Layer {ball} -under {Signal$0353F508BOTOM} -circuit {BGAI}
sigrity::update Attributes -circuit {D1} -dmax {0.12e-3} -D1 {0.10e-3} -D2 {0.10e-3} -HT {0.08e-3} -conductivity {5.0e+7}
sigrity::update ExtractionFreq {30e+6}
sigrity::update cpline -risetime {100} -percent {3} -all

```

- Click the **Open a TCL file** icon to load the prepared *.tcl file.



- Click the **Play TCL** icon to run the prepared TCL command.



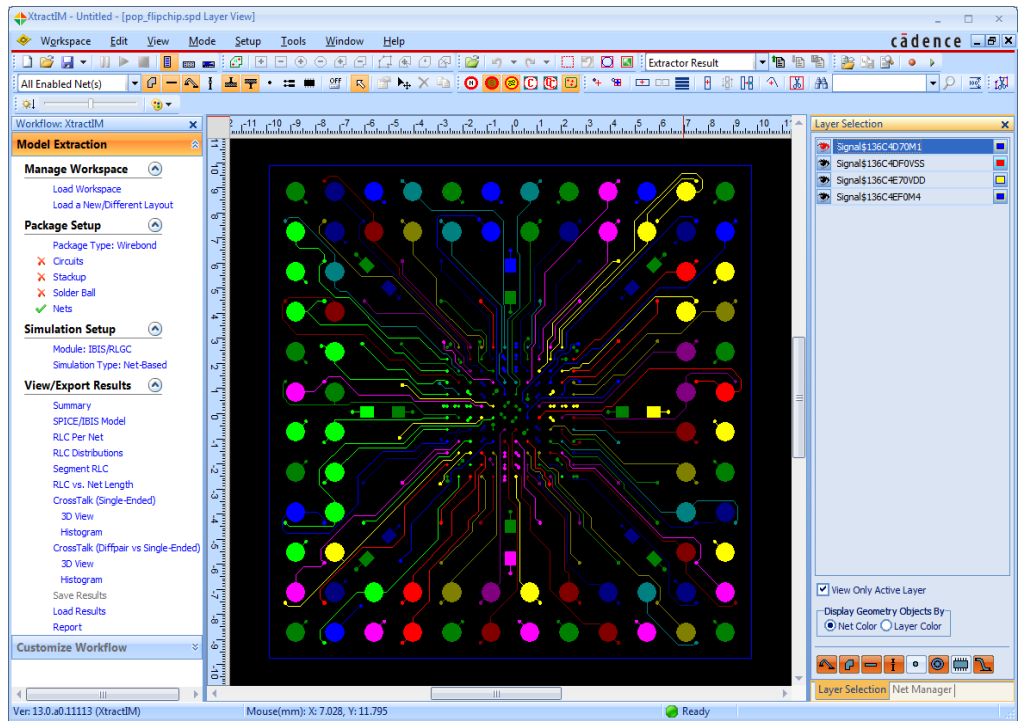
The same result will come out as in *Step 4*.

Stacked-BGA Package Sample

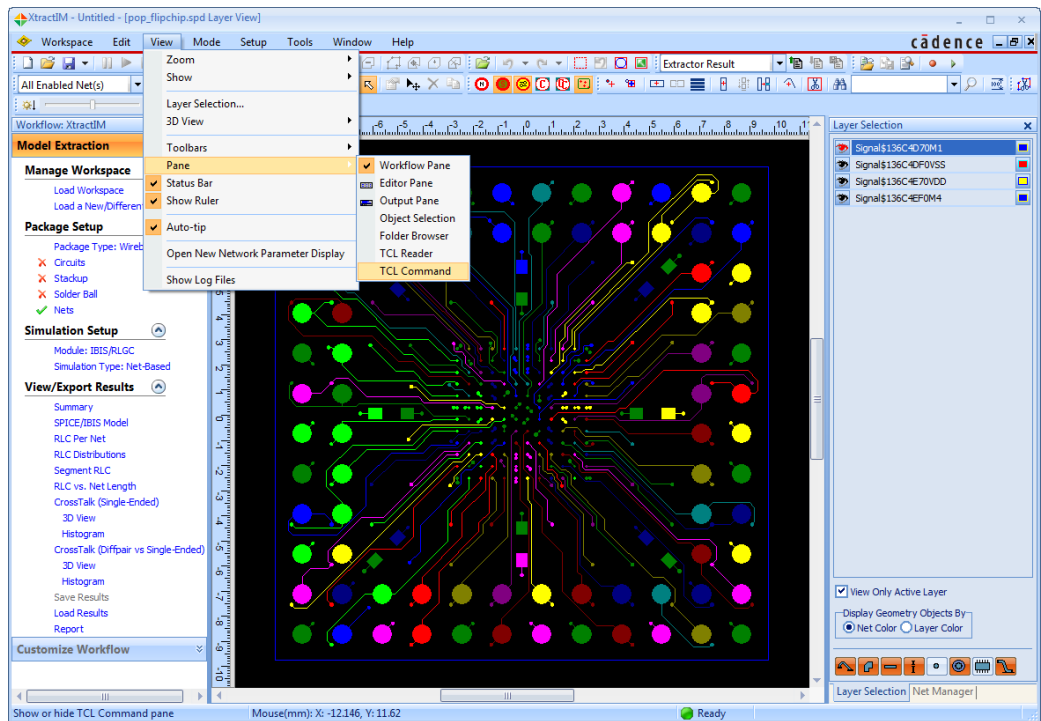
- Load *pop_flipchip.spd*.

It is typically located in <ASI_INSTALL_DIR>\Update3\SpeedXP\Samples\XtractIM\Single-Die_Sample_files\.

A flipchip BGA package is placed above a flipchip BGA package.



2. Choose View > Pane > TCL Command to open the TCL command input console.

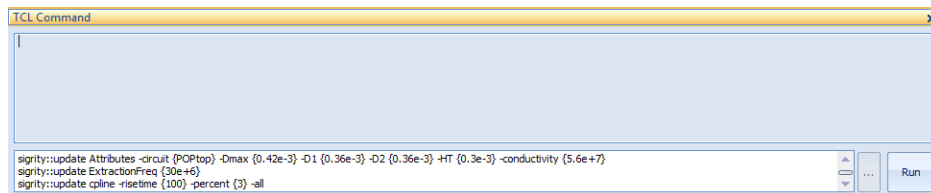


3. Copy the following TCL command to the **TCL Command** console.
`sigity::update PackageType -dieType {0} -bgaType {1} -attachType {1}`
`sigity::update Circuits -dieCkts {U1} -boardCkts {POPtop} -boardCkts {POPbottom}`

```

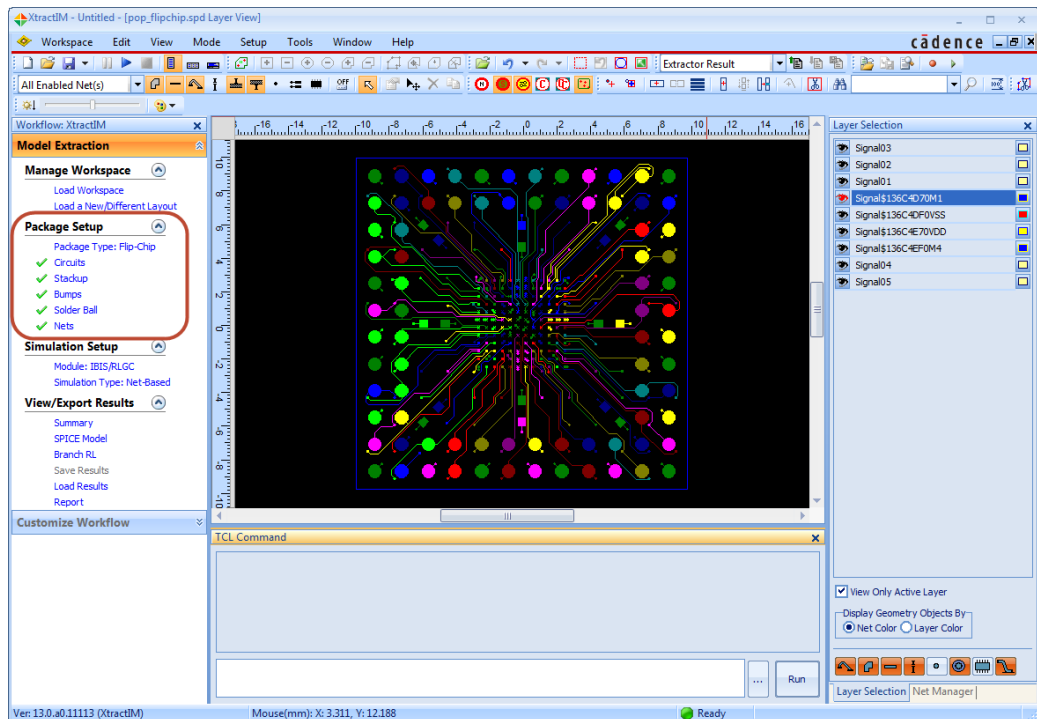
sigirty::add Layer {bump} -above {Signal$136C4D70M1} -circuit {U1}
sigirty::add Layer {ball} -above {Signal$136C4D70M1} -circuit {POPtop}
sigirty::add Layer {ball} -under {Signal$136C4EF0M4} -circuit {POPbottom}
sigirty::update Attributes -circuit {U1} -Dmax {0.12e-3} -D1 {0.10e-3} -D2 {0.10e-3} -HT
{0.08e-3} -conductivity {5.0e+7}
sigirty::update Attributes -circuit {POPbottom} -Dmax {0.4e-3} -D1 {0.35e-3} -D2 {0.35e-3}
-HT {0.45e-3} -conductivity {5.2e+7}
sigirty::update Attributes -circuit {POPtop} -Dmax {0.42e-3} -D1 {0.36e-3} -D2 {0.36e-3}
-HT {0.3e-3} -conductivity {5.6e+7}
sigirty::update ExtractionFreq {30e+6}
sigirty::update cpline -risetime {100} -percent {3} -all

```



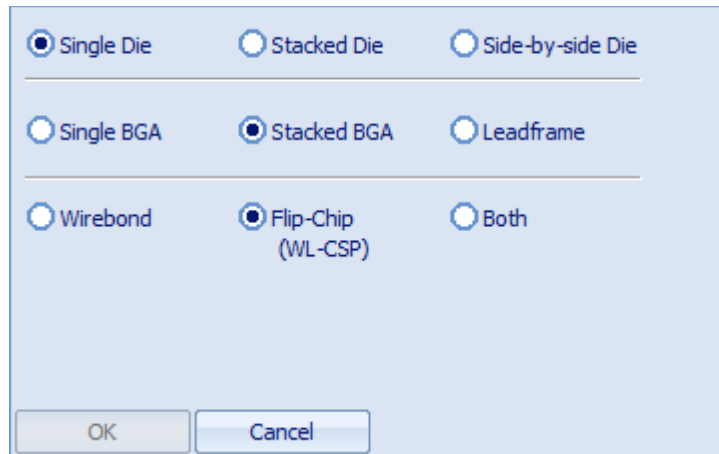
4. Click the **Run** button in the **TCL Command** console.

The **Package Setup** is automated.

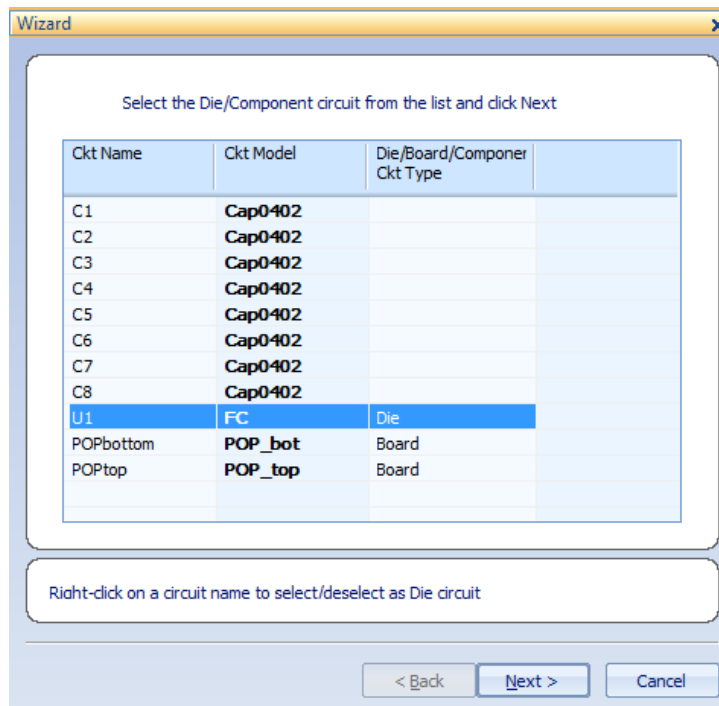


The relationship between individual TCL command and the corresponding Package Setup is described as follows.

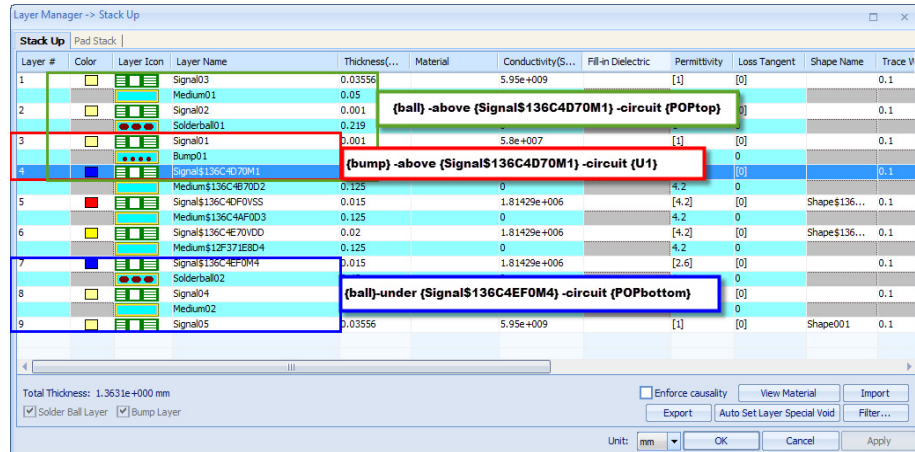
- sigirty::update PackageType -dieType {0} -bgaType {1} -attachType {1}



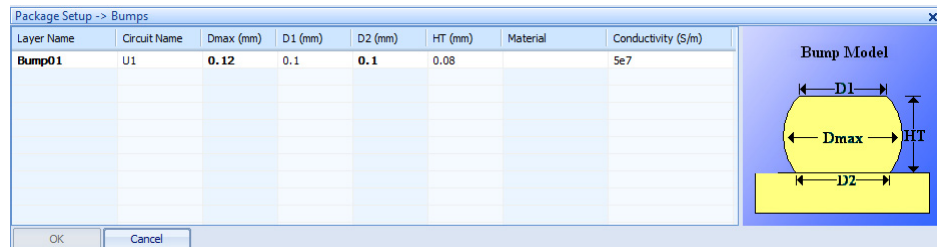
- `sigrity::update Circuits -dieCkts {U1} -boardCkts {POPtop} -boardCkts {POPbottom}`



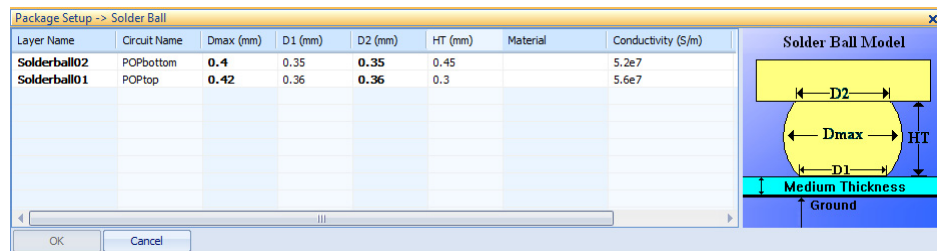
- `sigrity::add Layer {bump} -above {Signal$136C4D70M1} -circuit {U1}`
- `sigrity::add Layer {ball} -above {Signal$136C4D70M1} -circuit {POPtop}`
- `sigrity::add Layer {ball} -under {Signal$136C4EF0M4} -circuit {POPbottom}`



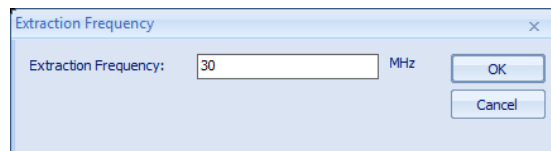
- sigrity::update Attributes -circuit {U1} -Dmax {0.12e-3} -D1 {0.10e-3} -D2 {0.10e-3} -HT {0.08e-3} -conductivity {5.0e+7}



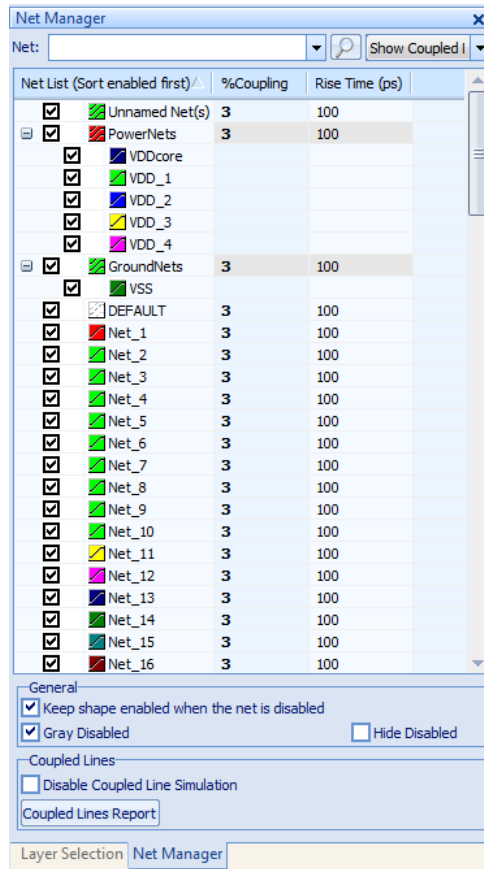
- sigrity::update Attributes -circuit {POPbottom} -Dmax {0.4e-3} -D1 {0.35e-3} -D2 {0.35e-3} -HT {0.45e-3} -conductivity {5.2e+7}
- sigrity::update Attributes -circuit {POPtop} -Dmax {0.42e-3} -D1 {0.36e-3} -D2 {0.36e-3} -HT {0.3e-3} -conductivity {5.6e+7}



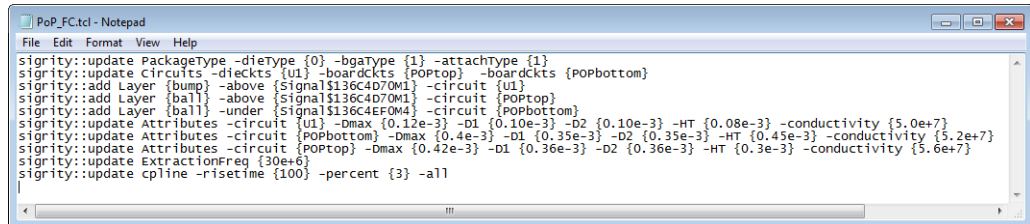
- sigrity::update ExtractionFreq {30e+6}



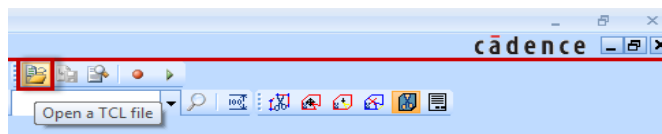
- sigrity::update cpline -risetime {100} -percent {3} -all



5. The TCL command used above can also be prepared as a .tcl file.



6. Click the **Open a TCL file** icon to load in the prepared *.tcl file.



7. Click the **Play TCL** icon to run the prepared TCL command.



This same result will come out as in *Step 4*.

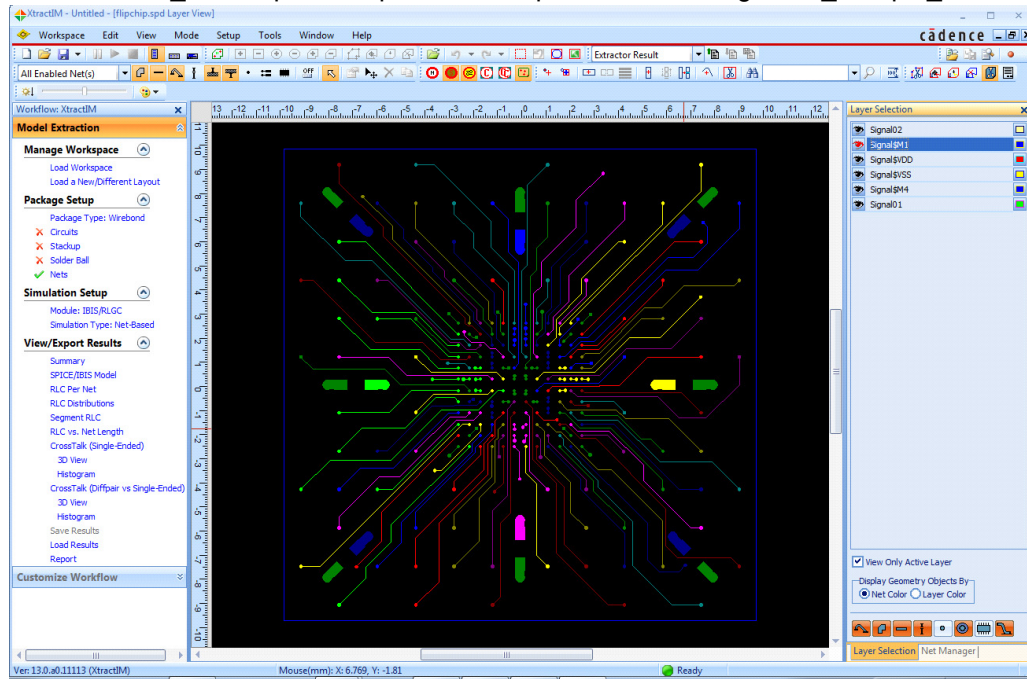
LESSON TWO: TCL COMMAND RECORDING SUPPORT FOR WORKSPACE SETUP

In this lesson, the TCL recording function for XtractIM workflow setup is introduced for preparing a reusable TCL file.

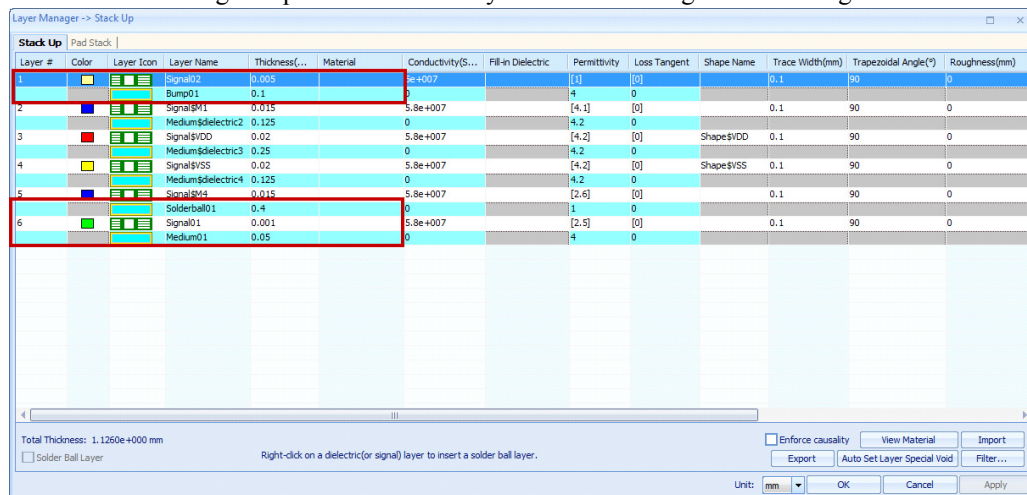
Load Design

1. Load a sample spd file.

flipchip.spd is used as sample case in this tutorial. It is by default located at `<INSTALL_DIR>\Update4\SpeedXP\Samples\XtractIM\Single-Die_Sample_files\`.

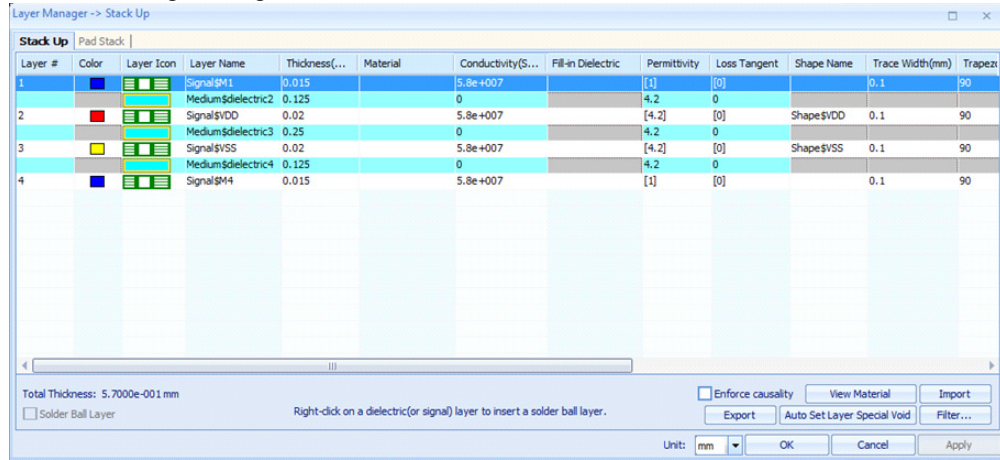


2. Remove existing bump and solder ball layers before running TCL recoding command.

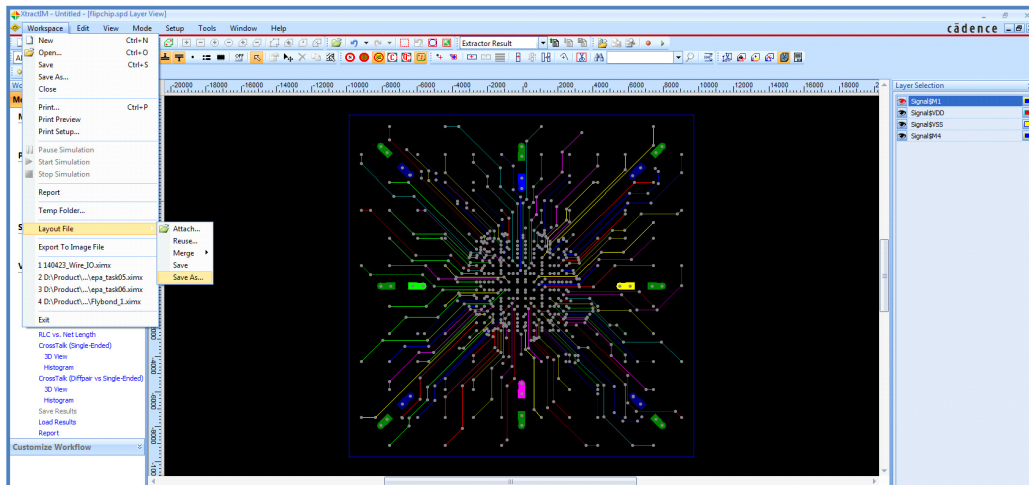


3. Click OK.

The Stackup is setup as below.

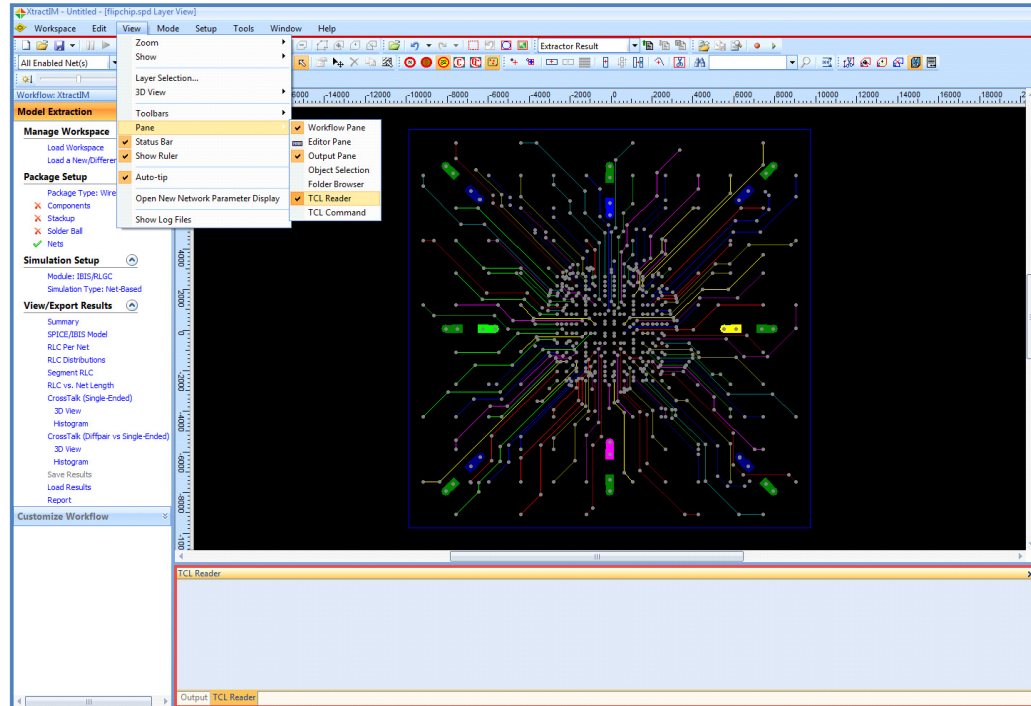


4. Save the clean spd file to the working directory.

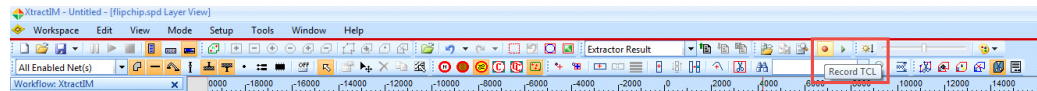


Record TCL Command for Workspace Setup

1. Choose View > Pane > TCL Reader.

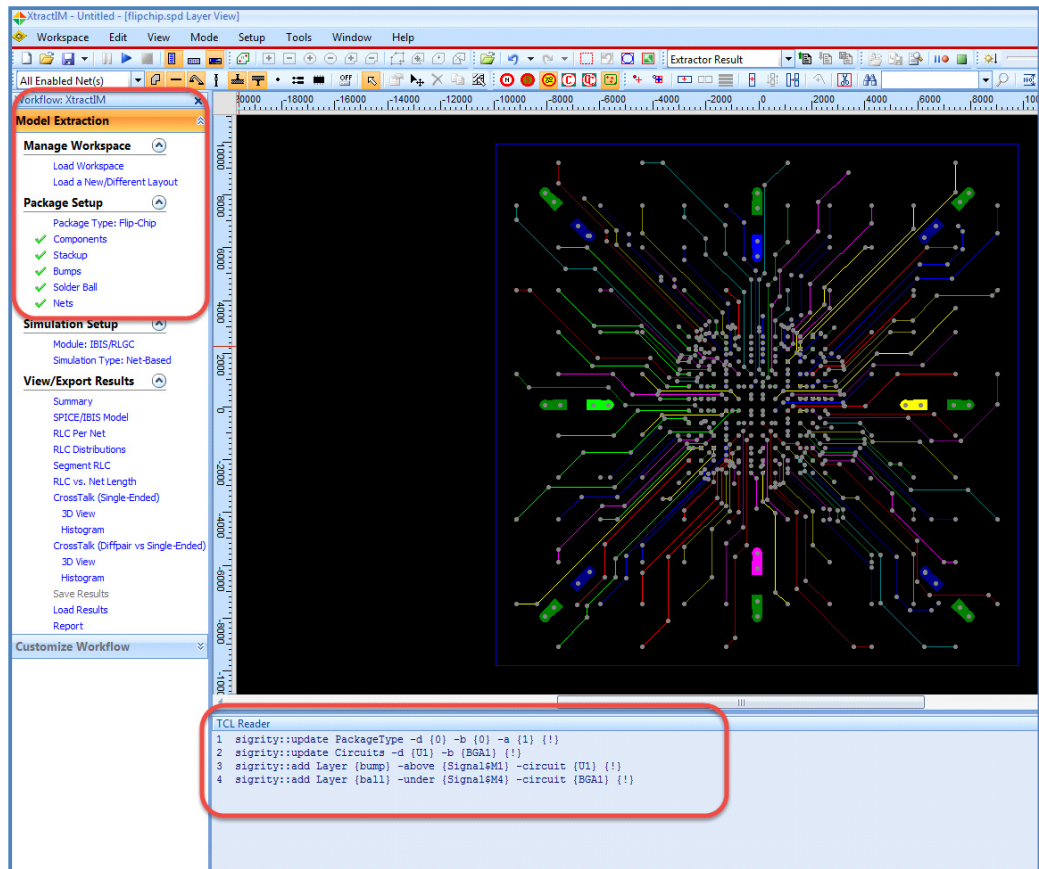


2. Click the **Record TCL** button.

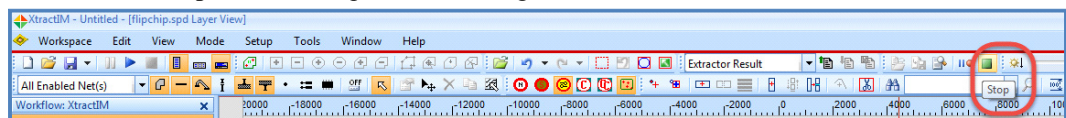


3. Set up the workflow as usual.

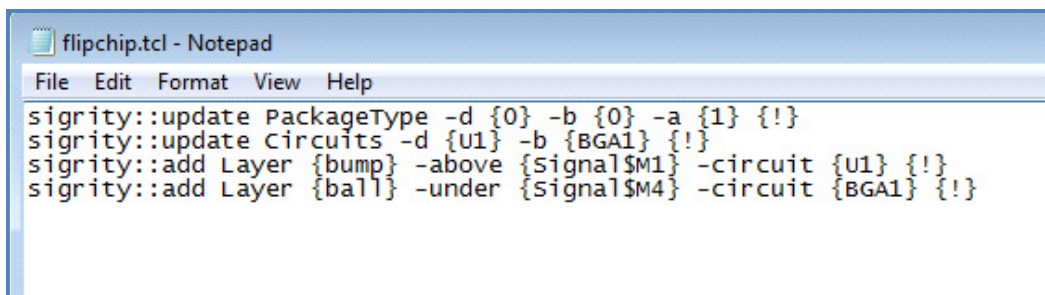
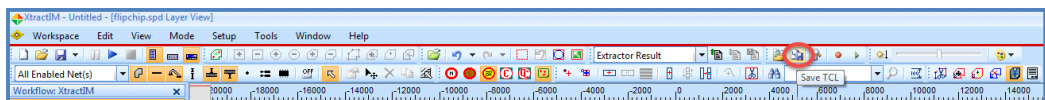
The used TCL command will be written in the TCL reader.



4. Click the **Stop** button to stop TCL recording.



5. Click the **Save TCL** button to save the TCL command to a file for reuse.



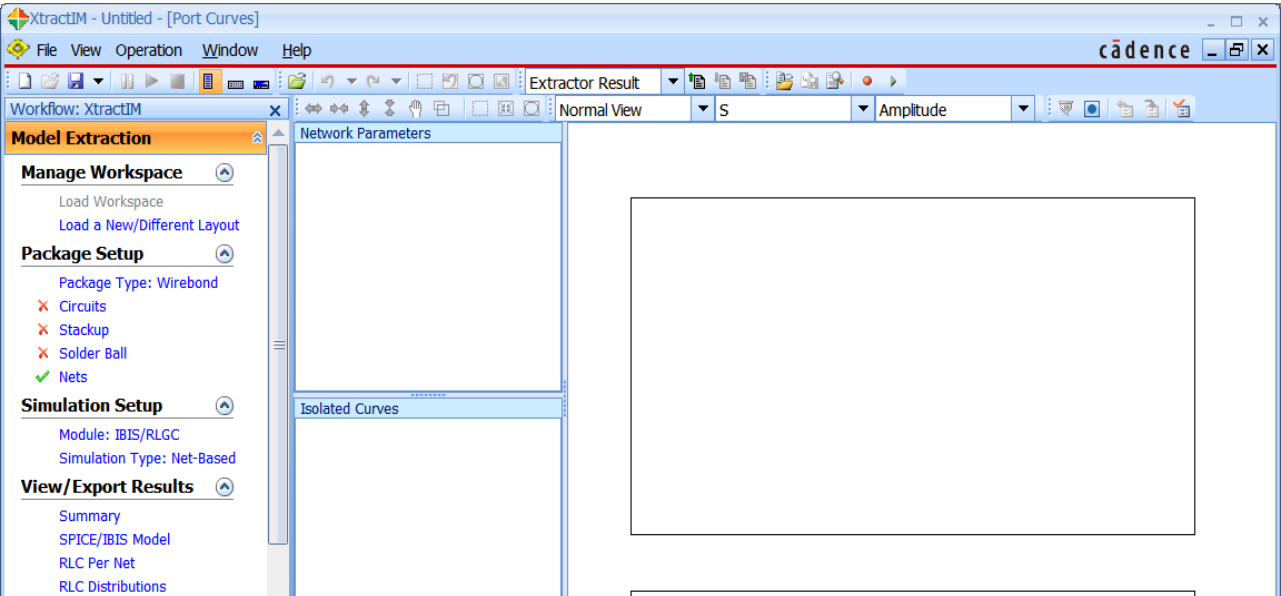
Network Parameter Viewer

This chapter takes you through the steps to use the XtractIM tool to view Network Parameter with both BNP and Touchstone files.

LOAD BNP / TOUCHSTONE FILES

1. Launch XtractIM.
2. Click the **New** button on the toolbar.
3. To open new Network Parameter Display, choose **View > Open New Network Parameter Display**.

The **Network Parameters** pane appears.





4. Choose
File > Open
or right-click in the upper left pane.
5. Select **Load** from the Context menu.
6. Select the network parameter files to be loaded.

Multiple BNP/ Touchstone files can be opened at the same time. Once a file is loaded successfully, there is a new entry of the Network Parameter Matrix added to the Matrix pane.

7. Click on the **Open** button.

By default the diagonal elements of the matrix are shown. The corresponding frequency curves are displayed in the Curve pane. A unique ID is assigned to the matrix and its elements, followed by a customizable display names.

The icon  denotes a matrix corresponding to a Touchstone file while the icon  denotes a matrix corresponding to a BNP file.

Select Matrix Elements


1. Select one or more parameter matrices.
2. Select
View > Select Matrix Elements
or right click on a selected matrix.
3. From the context menu select
Select Matrix Elements

The **Matrix Element Selection** dialog appears.

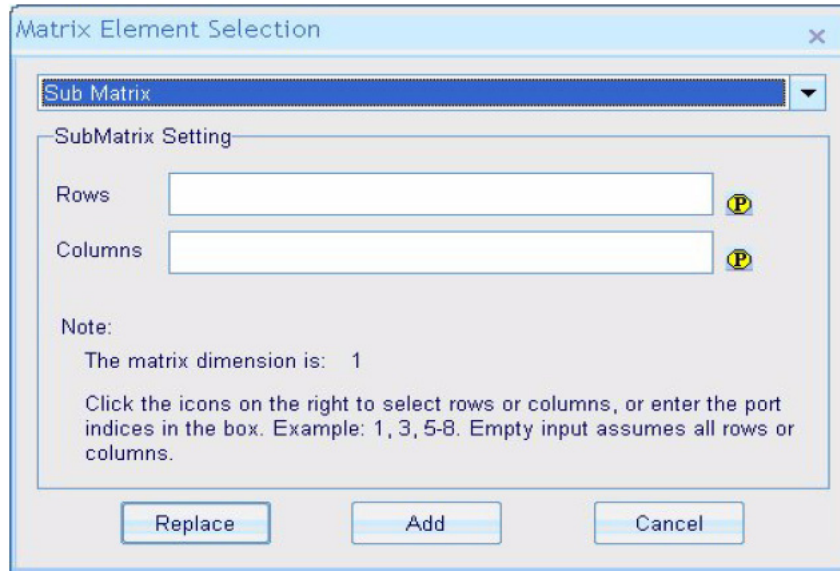
4. From the drop-down box choose from the pre-defined patterns.
 - Diagonal
 - Full Matrix
 - Lower Triangular Matrix
 - Sub Matrix
 - Upper Triangular Matrix

The **Sub Matrix** option is not available if more than one matrix is selected and the dimensions are different

5. If **Sub Matrix** is selected, enter the row and column numbers in the input boxes;

or click on the  icon and choose from the list of ports.

6. Click the **Replace** button to replace the existing displayed curves with the selections;
or click the **Add** button to add the selected curves to the existing list.



Hide / Show Matrix Elements

1. Single-click on the color icon in front of a matrix element to trigger the visibility; or select multiple matrices or matrix elements.
2. Select
View > Show/Hide Curves
or right-click on a selected matrix or curve.
3. Select
Show/Hide Curves
4. Choose from the available Visibility Control options.

Delete Matrix Elements

1. Select one or more matrix elements.
2. Select
View > Delete Selected Curves
or right-click on the selection.
3. Select
Delete Selected Curves
or press the **Delete** key.

Unload Networks

1. Select one or more matrices.
2. Select

File > Unload Network

or right-click on the selection.

3. To remove the selection from the Matrix pane select

Unload Network

4. To remove all the loaded networks select

Unload All Networks

The simulation result cannot be unloaded.

SAVE BNP / TOUCHSTONE FILES

Save a Modified Network

A network can be modified by editing the comments of the file, or by performing matrix operations such as re-normalization or frequency truncation, etc. When a network is modified, a star is added to the icon before the matrix entry. To save the modification follow these steps.

1. Select a matrix entry that has been modified.

2. Select

File > Save

or right-click on the selected matrix.

3. Select **Save** from the context menu.

The modified information is saved into the original file, over-writing its contents with the exact same settings of the file.

Save Network as Another File

1. Select a matrix.

2. Select

File > Save As

or right-click on the selection.

3. Select

Save As

In the **Save Curves** dialog, follow the same steps as in saving the simulation result

This feature allows you to convert between the BNP and Touchstone formats. Some of the information in the BNP file (such as AFS compression) is not supported by the Touchstone format.

If you save a BNP file with AFS compression into a Touchstone file, the matrices at discrete frequency samples is saved.

Export the Curves to Other Format

1. To save the screen shot of the curve window into a BMP file or PNG file select

File > Export to Image File

2. Select a matrix.
3. To save the displayed curves into a Excel .csv file select
File > Export To Excel

View Network Properties

1. Select a matrix entry.
2. Select
View > Property
or right-click on the selection.
3. Select **Properties** from the context menu.

The **Network Property** dialog allows you to view various information of the network. You can edit the comments in the dialog.

- Data Types
- Design Information
- Differential Pair Setup
- Port Setup
- Sampling Frequencies
- User Comments

CUSTOMIZE THE NETWORK AND ELEMENT DISPLAY NAME

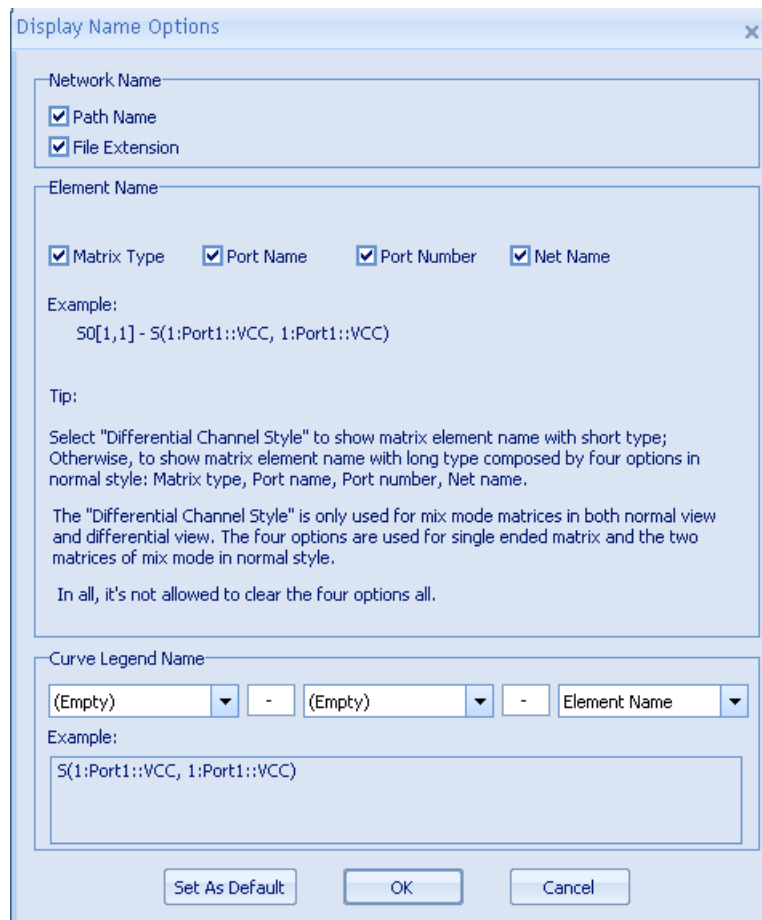
1. Select one or more matrix entries.
2. Select
View > Name Display > Customize
or right-click on the selection.
3. From the context menu select
Name Display > Customize
4. Check the appropriate fields you want to include in the network name, matrix element name and curve legend.
Examples of the element name and the curve legend are displayed as you change the settings.
5. Click **OK** to apply the setting to the selected matrices;
or, to apply the setting to all matrices, select
Save as Default
The default settings are saved into the registry and used for the networks loaded in the future.
6. In addition to the default names, the display names can also be modified. Select an entry.
7. Select
View > Name Display > Rename

or right-click on the selection.

8. From the context menu select
Name Display > Rename

You can then edit the name to any string. You can switch back to the default name.

9. From the View or Context menu, select
Name Display > Default Name



ADVANCED MATRIX OPERATIONS

Copy Network

1. Select one or more matrices.
2. Select
Operation > Copy
or right-click on the selection.

3. Select **Copy** from the context menu. When a network is copied, a new network is created. A matrix entry is added to the matrix pane.

The status of this network is set to **modified**. It is not saved to the hard drive until you manually save it.

Network Re-normalization

1. Select a network in the Matrix pane.

2. Select

Operation > Re-normalize

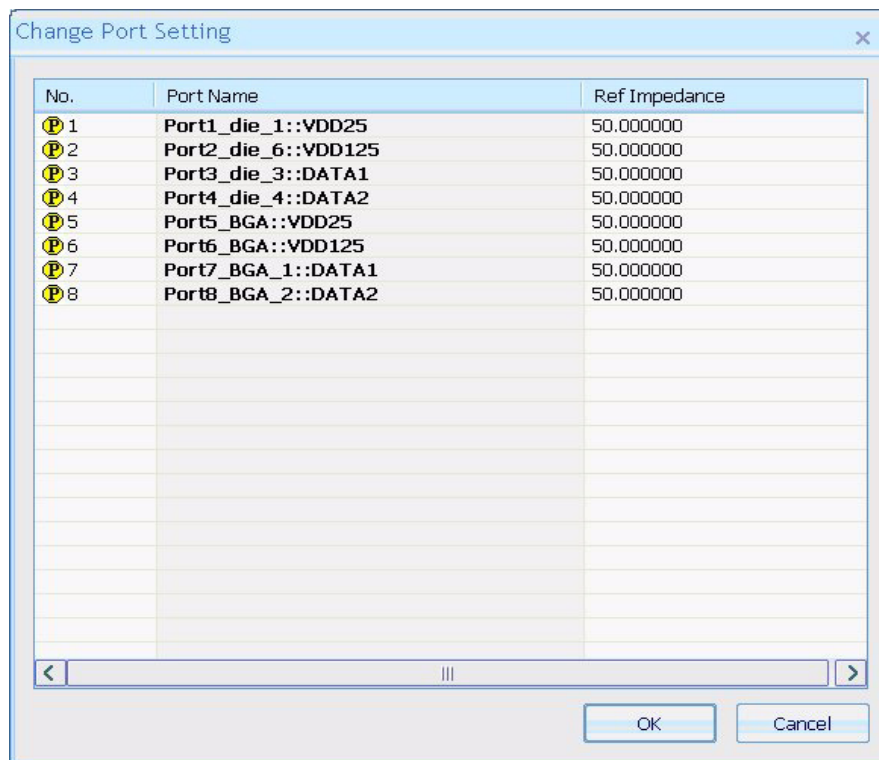
or right-click on the selection.

3. From the Context menu select

Matrix Operation > Re-normalize

The **Change Port Setting** dialog appears.

4. To edit the reference impedance of a single port select the line and click on the impedance value.
5. To change several ports at the same time, select multiple ports. A reference impedance input box appears.
6. Click **OK** to apply the changes. The **S** parameter curves are updated. The matrix is marked as modified.



Port Reduction

1. Select a network in the matrix pane.
2. Select
Operation > Reduction
or right-click on the selection.
3. From the context menu select
Matrix Operations > Reduction
The **Change Port Setting** dialog appears.
4. To change the status of a single port by select the line. Each port has 4 connection settings:
 - Match
 - Open
 - Remain as a Port
 - Short
5. Click on its connection status or select multiple ports.
6. Change their status together in the combo box at the bottom of the window.
7. Click **OK** to perform port reduction. The result is a new network added to the matrix pane. The network parameters are not saved to the hard drive until you manually perform a **Save**.

NOTE!

A BNP file with AFS compression cannot be reduced directly, since the AFS compression information in the original matrix is not necessarily valid for the reduced matrix. A warning message is shown. The matrix is converted into a discretely sampled format.

No.	Port Name	Port Connection Status
1	Port1_die_1::VDD25	Matched
2	Port2_die_6::VDD125	Matched
3	Port3_die_3::DATA1	Port
4	Port4_die_4::DATA2	Port
5	Port5_BGA::VDD25	Open
6	Port6_BGA::VDD125	Open
7	Port7_BGA_1::DATA1	Port
8	Port8_BGA_2::DATA2	Port

Passivity Enforcement

1. Select a network in the Matrix pane.

2. Select

Operation > Passivity Enforce

or right-click on the selection.

3. From the Context menu select

Matrix Operations > Passivity Enforce

A new network with passivity enforcement at each sampling frequency is generated.

NOTE!

Passivity enforcement is not available for BNP files with AFS compression.

Edit the Differential Pairs

A differential pair is defined with two nets. Pairs of differential ports can be defined under each differential pair. The differential pair and differential port information can be defined in PowerSI before the simulation and can be modified in the network parameter display.

1. Select a network in the matrix pane.

2. Select

Operation > Redefine Differential Port

or right-click on the selection.

3. From the context menu select

Matrix Operations > Redefine Differential Port

The **Define Differential Ports** dialog appears.

4. To remove an existing definition, select a pair of nets or a pair of ports.

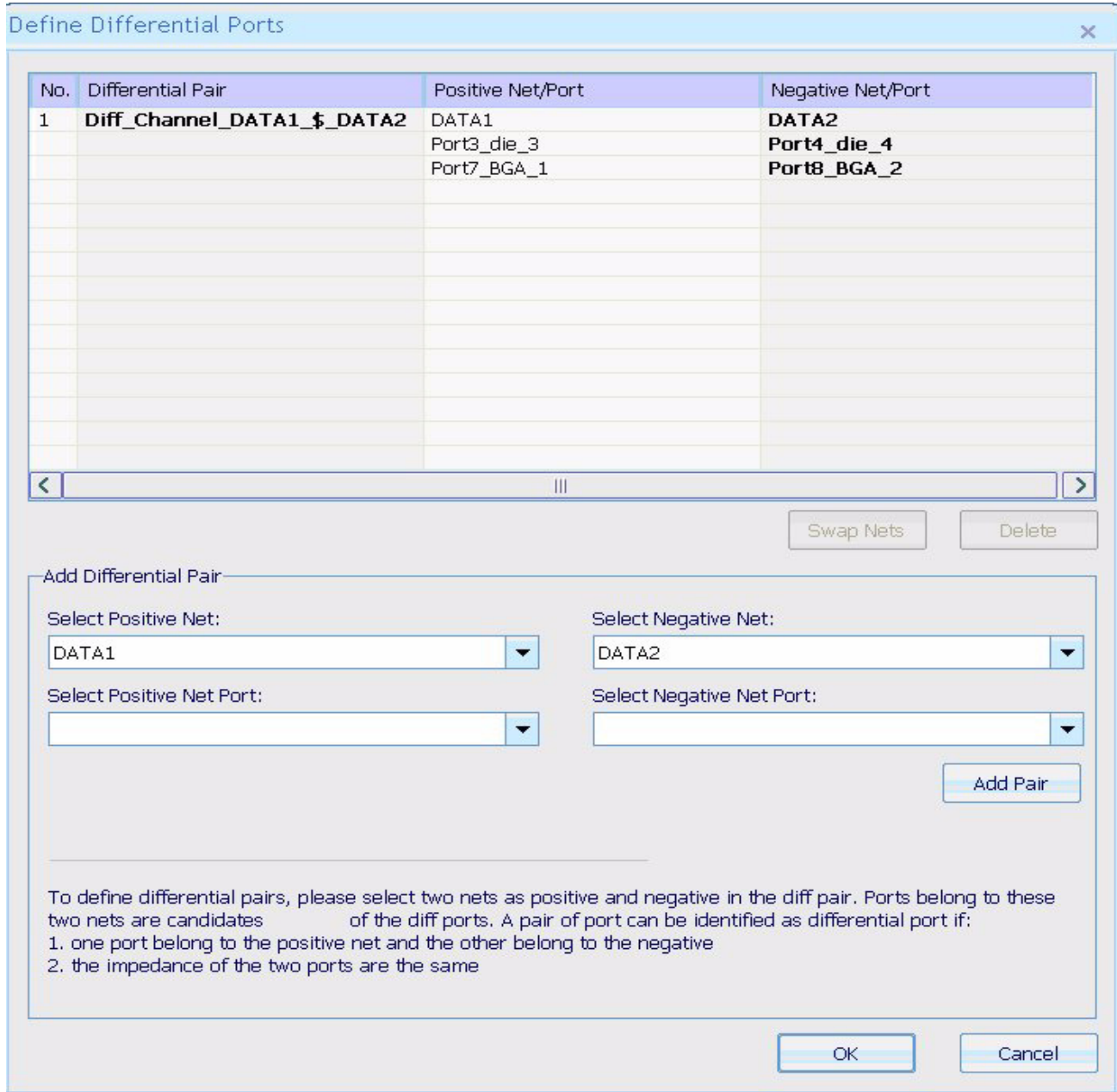
5. Click the **Delete** button.

6. To add a new pair, select a pair of nets from the net combo boxes.

7. Select a pair of ports from the port combo boxes.

8. Click **Add Pair** to create the differential ports.

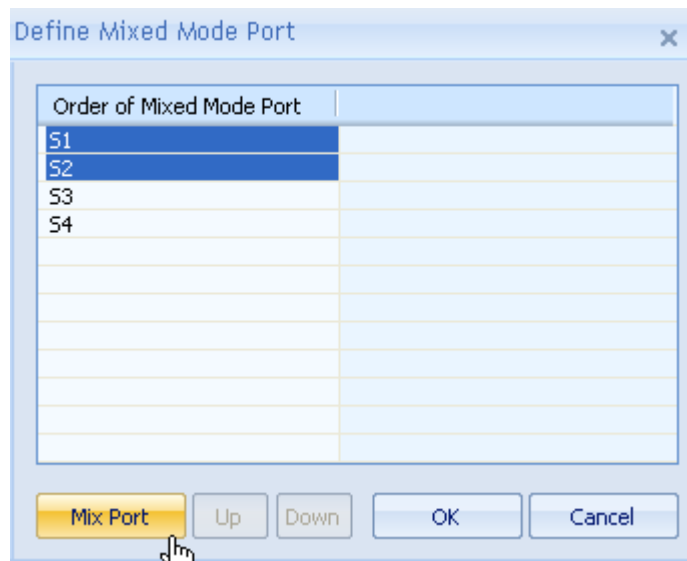
9. Click **OK** to apply the changes. The mixed-mode network parameters are updated.



Redefine Mixed Mode Port

1. Select a network in the matrix pane.
2. Select
Operation > Redefine Mixed Mode Port
or right-click on the selection.
3. From the context menu select
Matrix Operations > Redefine Mixed Mode Port

The **Define Mixed Mode Port** dialog appears.



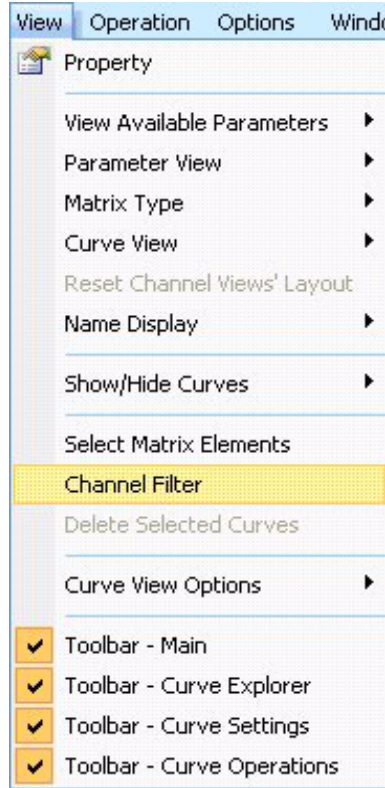
4. Hold down CTRL key and select two ports.
5. Click **Mix Port** to generate new mixed S-parameter.
6. Click **Ok** to apply changes.

The mixed-mode network parameters are updated.

SHOW NETWORK PARAMETERS VIA CHANNEL FILTER

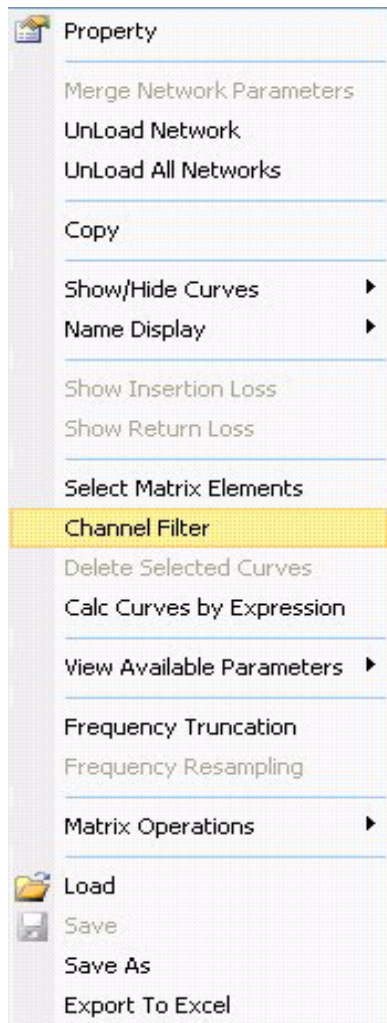
1. Select a matrix.
2. Click

View > Channel Filter



or select the pop-up menu

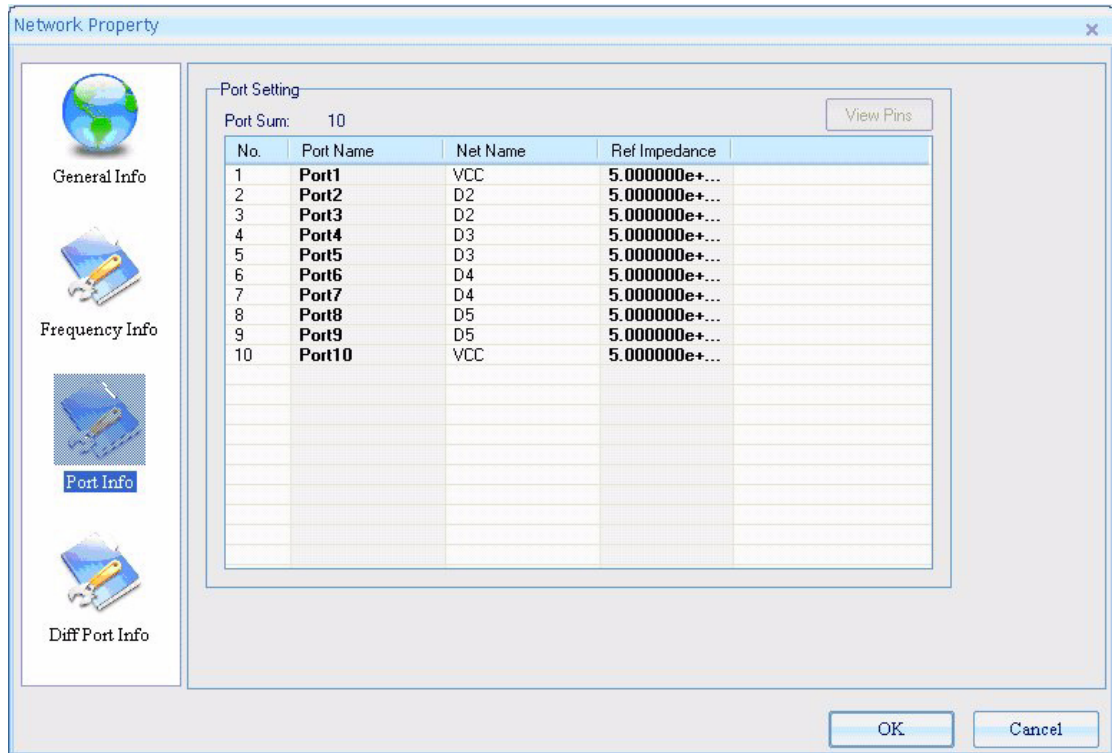
Channel Filter



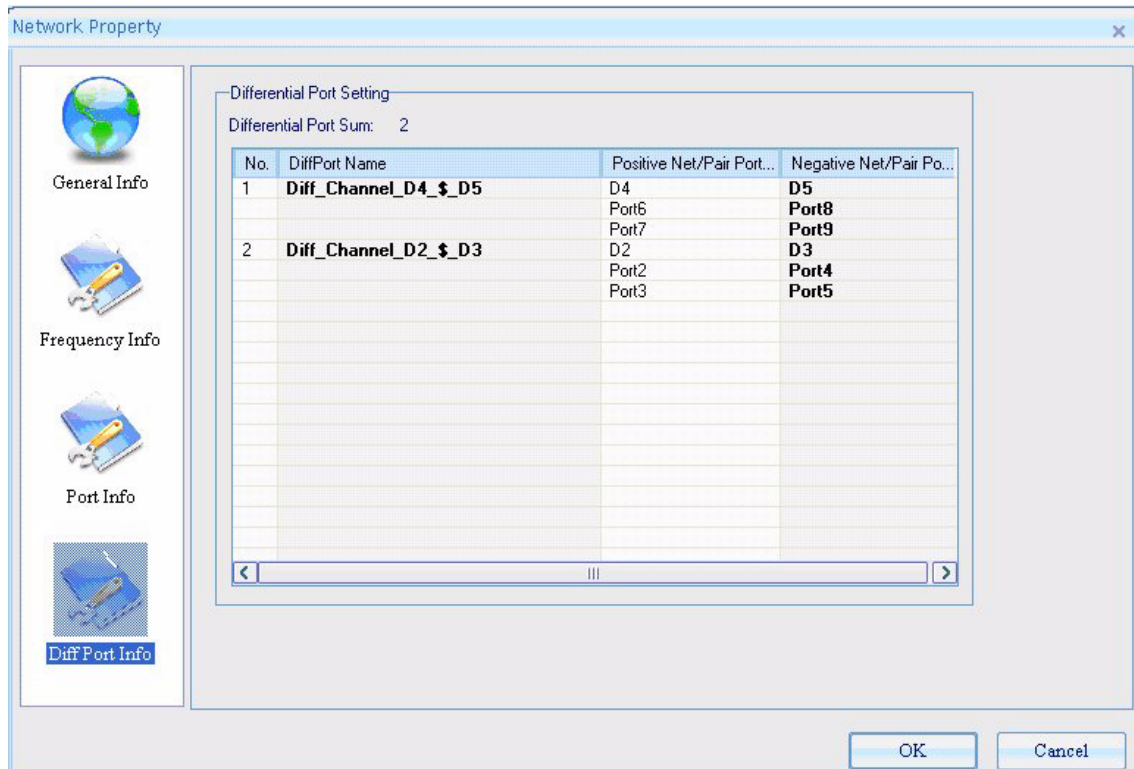
If no network matrix is selected, the **Channel Filter** menu or toolbar button appears **gray**.

3. A **Channel Filter** dialog appears.
 - For every network, there are 3 views of the matrices items.
 - It depends on the port setting and different channel setting.
 - If there is no different channel setting defined in a network, there is only one view of a single channel matrix.

Port Setting Example



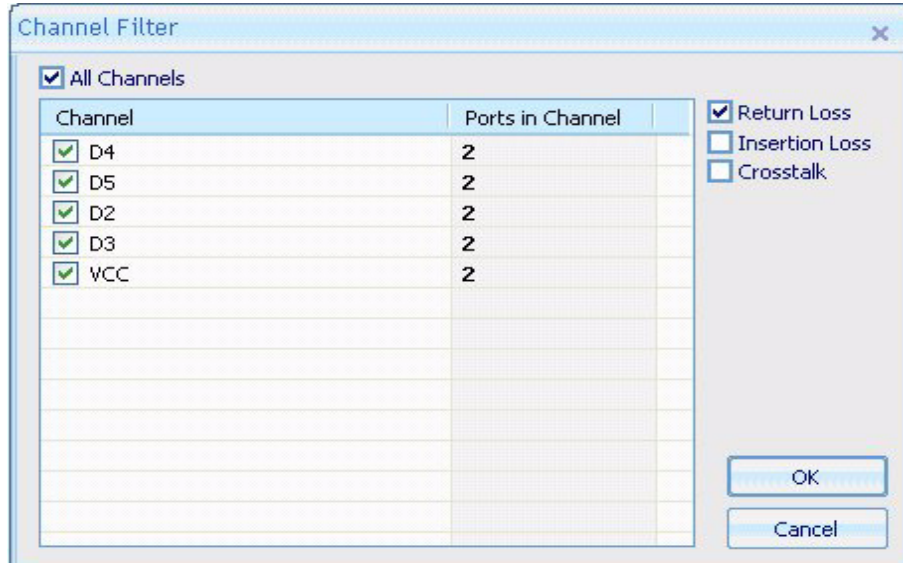
Differential Port Setting Dialog



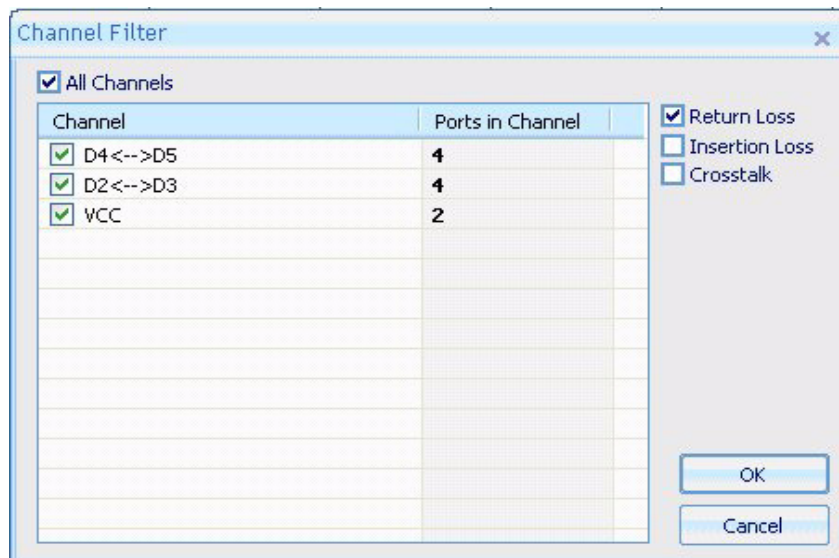
There are three Channel Filter dialogs.

- Mixed Mode Matrix in Differential Channel View.
- Mixed Mode Matrix in Normal View.
- Single Channel Matrix in Normal View.

Single Channel Matrix in Normal View



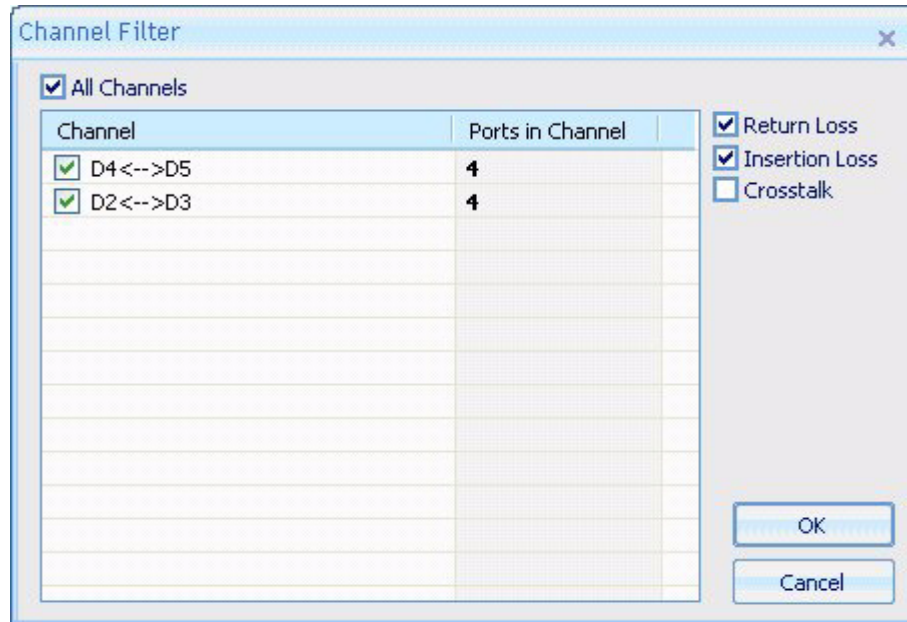
Mixed Mode Matrix in Normal View



Mixed Mode Matrix in Differential Channel View

The dialog below lists all the channels in current matrix. Users can select the channels in the list by a multiple-select method. To select all channels select

All Channels



- **Mixed Mode Network Parameters** — A channel is defined as all the port pairs in a differential net pair.
- **Single-ended Network Parameters** — A channel is defined as all the ports in a net.

Once a channel is selected, all ports under this channel are selected. The sub-matrix corresponding to all the selected ports are used for further selection. The elements in the selected sub-matrix are divided into three categories:

- **Crosstalk** – Rest of the elements.
- **Insertion Loss** – Off diagonal elements whose two ports are in the same channel.
- **Return Loss** – Diagonal elements.

The **Insertion Loss** and **Crosstalk** elements consider the elements in the lower triangular matrix. This dialog can remember last user's selection including:

- Channels
- Crosstalk
- Insertion Loss
- Return Loss

1. Select channels.
2. Check and uncheck the three options on the right side of the pane.
3. Click **OK**.

The displayed elements in the selected network should be replaced by the elements specified in the user selection.

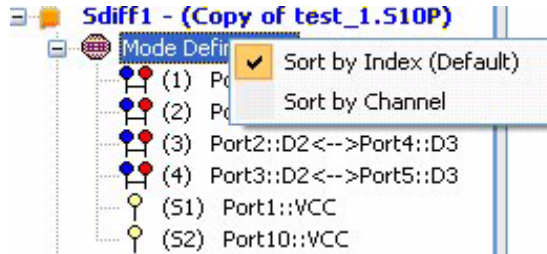
New Organization of Mixed Mode Network Parameters

Mode Definitions under the mixed mode network matrix lists all port pairs of differential channel setting and single channel ports. Single channel ports are only listed in normal view.

This tree item is collapsed by default.

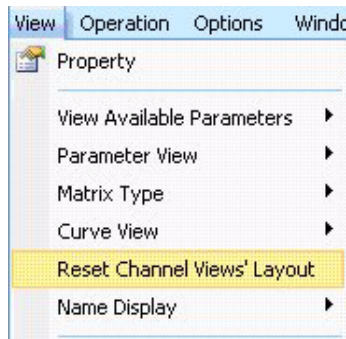
There are two pop-up menus. Use these menus to determine the sorting of the port pairs and single channel ports.

- Mode Definitions > Sort by Index (Default)
- Sort by Channel



Four curve views are available in the differential channel view pane.

1. Double-click in a curve view to maximize this curve view.
2. Double-click again to restore the size.
3. To restore the default layout of the four curve views click View -> Reset Channel Views' Layout
4. Double-click in the differential channel view to maximize and restore a curve window.



VIEW MIXED-MODE NETWORK PARAMETERS

The mixed mode parameters can be viewed in the normal view with the single-ended network parameters or in the differential channel view, which shows only the differential channels. The two views can be toggled by selecting

View > Parameter View > Normal View

or

View > Parameter View > Differential Channel View

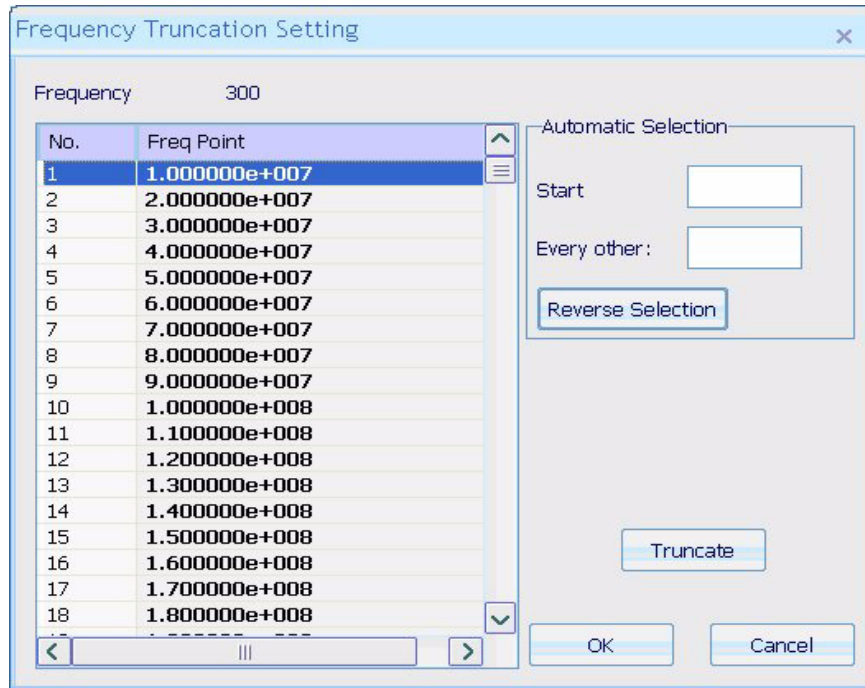
This can also be done with the combo box in the **Curve Settings** toolbar. If a loaded network contains differential pair definitions, but the mixed-mode network parameters are not displayed.

1. Select the matrix.
2. Select
View > View Available Parameters
or right-click on the selection.
3. From the context menu select
View Available Parameters
4. Choose the desired view.

Frequency Truncation

1. Select a network from the Matrix pane.
2. Select
Operation > Frequency Truncation
or right-click on the selection.
3. From the context menu, select
Frequency Truncation
4. Select the frequencies that you want to remove.
5. Click **Truncate** to remove these frequencies.

- Click **OK** to accept the final frequency sampling. The display is updated.



Frequency Re-sampling

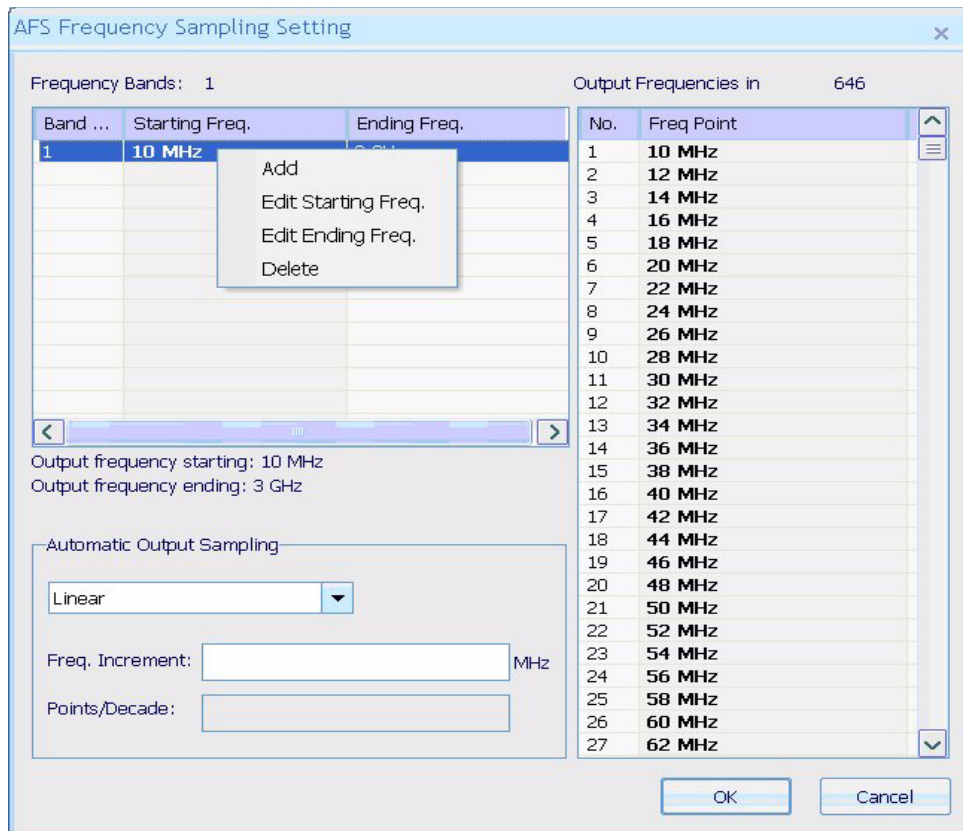
If the network parameters are saved in a BNP file with AFS compression, the sampling frequencies can be changed in the display.

- Select a network in the matrix pane.
- Select
Operation > Operation > Frequency Resampling
or right-click on the selection.
- In the Context menu, select
Frequency Resampling
- Right-click to select the frequency band. You can choose to:
 - Add a new band.
 - Delete the band.
 - Edit the ending frequency of the band.
 - Edit the starting frequency of the band.
- Select a **Sweeping Mode** from the **Automatic Output Sampling** combo box.
- Modify the sweeping information and click **Return**. The sampling with this band is updated.
- Select a frequency from the list on the right. Right-click.
- Edit the value or insert a frequency point above or below the selected frequency.
- You can select multiples of some frequencies. Right-click.
- Remove them from the list.

11. Click **OK** to accept the change. The display curves are updated.

NOTE!

The re-sampling is for display purpose. If you save the file in BNP format with AFS compression, the new sampling is not kept. To keep the new sampling, you can save the file in Touchstone format or discretely sampled BNP format.



VIEW TOTAL CROSSTALK OF NETWORK PARAMETER

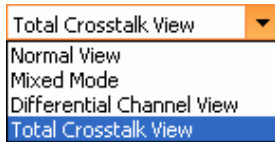
NOTE!

Total Crosstalk View is only available on reloaded result, not for current simulated result.

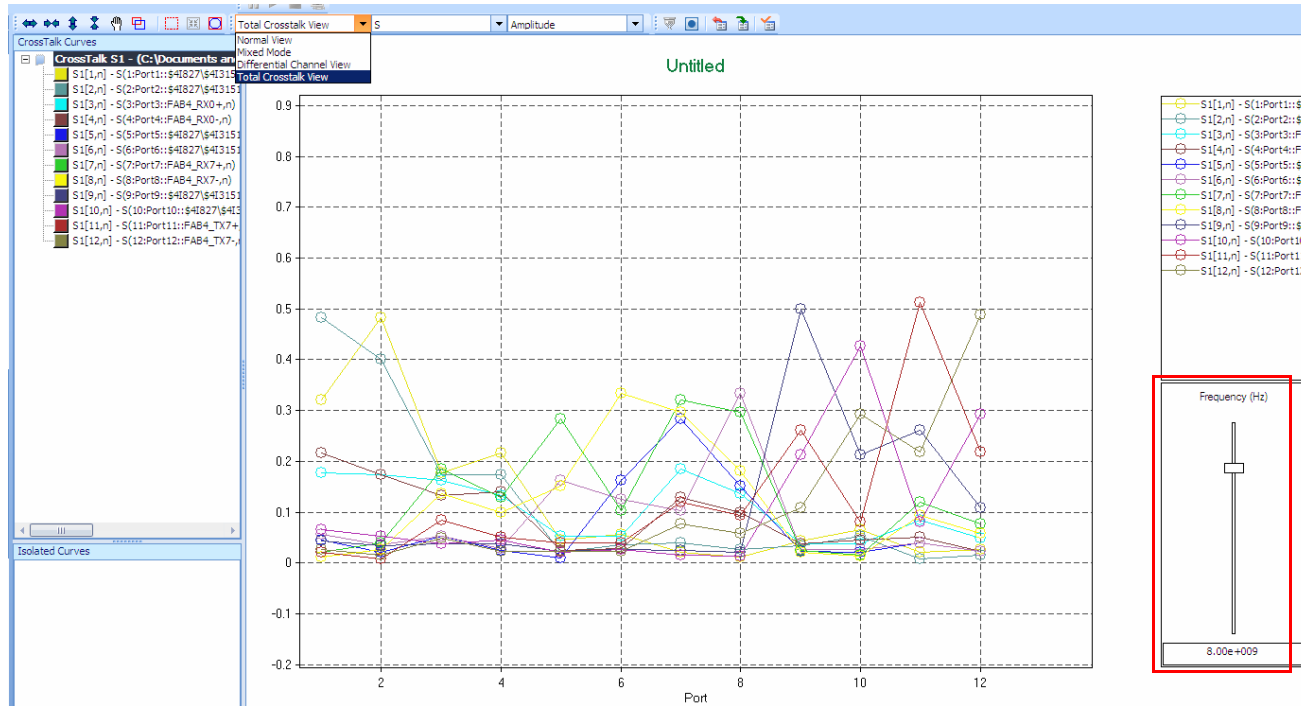
To view **Total Crosstalk View**, select

View > Parameter View > Total Crosstalk View.

Or select **Total Crosstalk View** from the toolbar.



The crosstalk result is displayed in the curve pane.



- Each curve shows the value of crosstalk from $S[i, 1]$ to $S[i, n]$.
- The X axis shows the port number from 1 to n.
- The Y axis represents the S/Y/Z Parameter.
- To view the crosstalk at desired frequency, you can use the scroll bar or enter specific number at the right-bottom corner.

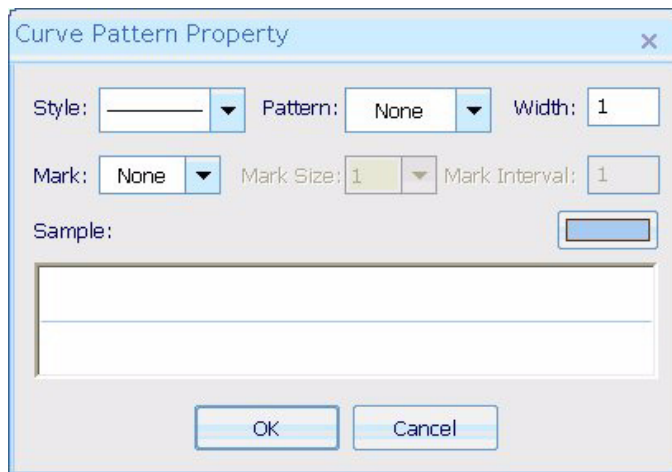
CURVE OPERATIONS

Load / Save Isolated Curves in PowerSI

1. Right-click in the **Isolated Curve** pane.
2. Select **Load** from the Context menu.
3. Select the curves in the **Isolated Curve** pane to save the curves.
4. Right-click on the selection.
5. Select **Save** from the context menu.

View and Set Curve Properties

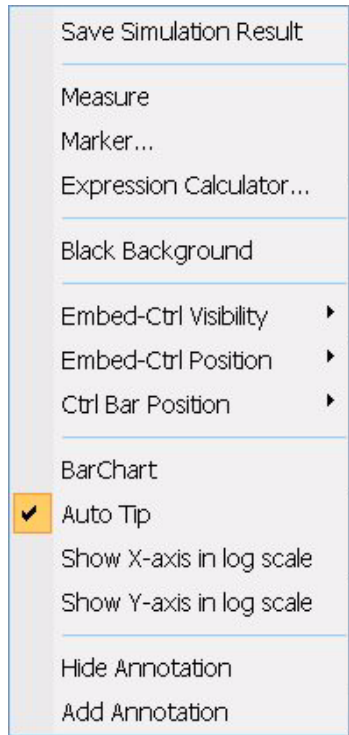
1. Select one or more matrix elements or one or more isolated curves.
2. Select
View > Property
or right-click on the selected curves.
3. Select **Property** from the context menu.



4. You can edit the following properties in the **Curve Property** dialog:
 - Curve Color
 - Line Pattern
 - Line Style
 - Line Width
 - Marker Size
 - Marker Type
5. Click **OK** to accept the changes. The selected curves are updated in the Curve window.

Curve Pane Context Menu

Right-click in the Curve window. A context menu appears.



You can perform the following operations in this menu.

- **Add Annotation** — Add a text string in the Curve window.
- **Auto Tip** — Show / Hide the tip of the objects in the Curve window when moving the mouse.
- **Bar Chart** — Toggle the plot style between a bar chart and a continuous line.
- **Black / White Background** — Set the background of the curve window to be black or white.
- **Ctrl Bar Position** – If a sub window is docked, change the position of the docking.
- **Embed-Ctrl Position** – Toggle the sub windows between floating or docking.
- **Embed-Ctrl Visibility** – Set the visibility of the sub windows (for example, the legend bar) in the display area.
- **Marker** — Toggle the horizontal and vertical marker lines.
- **Measure** — Toggle the horizontal and vertical measure lines.
- **Show X-axis in Log Scale** — Toggle the X axis between log scale and linear scale.
- **Show Y-axis in Log Scale** — Toggle the Y axis between log scale and linear scale, available only if the value type is set to Amplitude.

Copy Curve

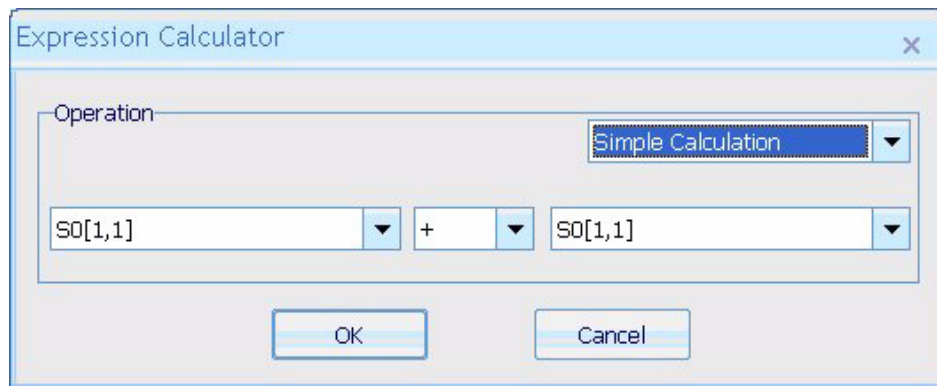
Curve Copy is a simple way to compare the network parameters of different types. The isolated curves are always the same regardless of the parameter matrix type.

1. Select one or more matrix elements, or one or more isolated curves.
2. Select
Operation > Copy
or right-click.
3. Select **Copy** from the context menu. The duplicates of the selected curves are added to the **Isolated Curve** pane.

Curve Calculation

1. Select
Operation > Expression Calculator
or right-click in the curve window.
2. In the context menu, select
Expression Calculator

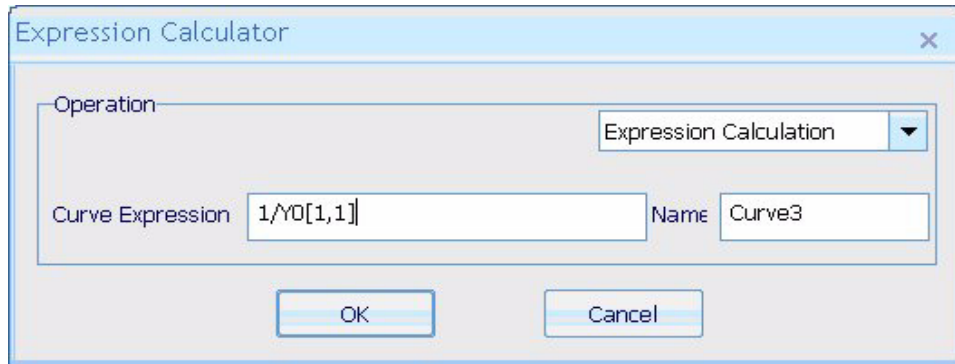
You can select the displayed curves or constants from the combo box and create a simple expression.



In the **Expression Calculation mode**, you can enter an expression with the matrix element unique ID or the isolated curve names.

A unique curve name is required for the new curve, and a default name is provided. The matrix elements can be anything that is available; it is not limited to the displayed elements.

3. Click **OK**. The calculation result is added as a new isolated curve.



Expression Customization

You can re-use an expression in future calculations.

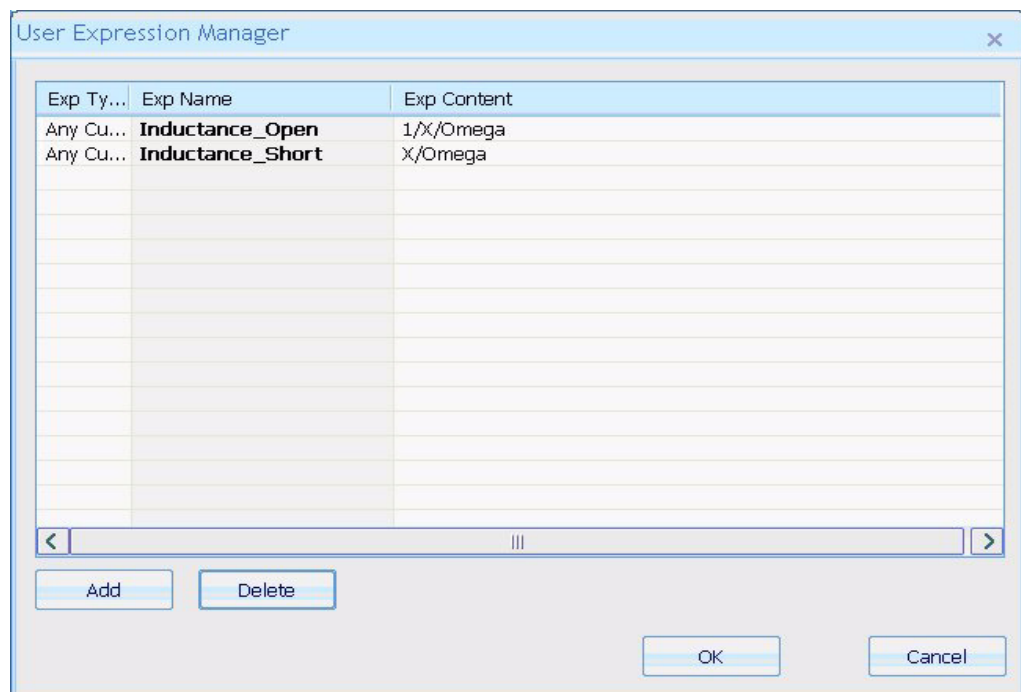
1. Create a curve using Expression Calculation.
2. Select the calculated curve.
3. Right-click on the selection.
4. In the context menu, select

Use Expression

The Expression Manager is displayed.

You can edit the name and contents of the expressions for later user. The symbol **X** represents the curve in the calculation.

5. Click **OK** to save the list of expressions.



Use a Saved Expression

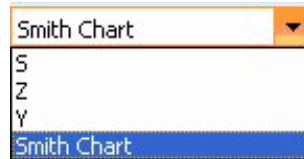
1. Select one or more matrix elements or one or more isolated curves.
2. Right-click on the selection.
3. From the context menu select
Calc Curves by Expression
4. In the Expression Manager select an expression.
5. Click **OK**. The expression is applied to all the selected curves. The calculation result is shown as new curves.

NOTE!

The validity of the expression depends on the parameter matrix and the port terminations.

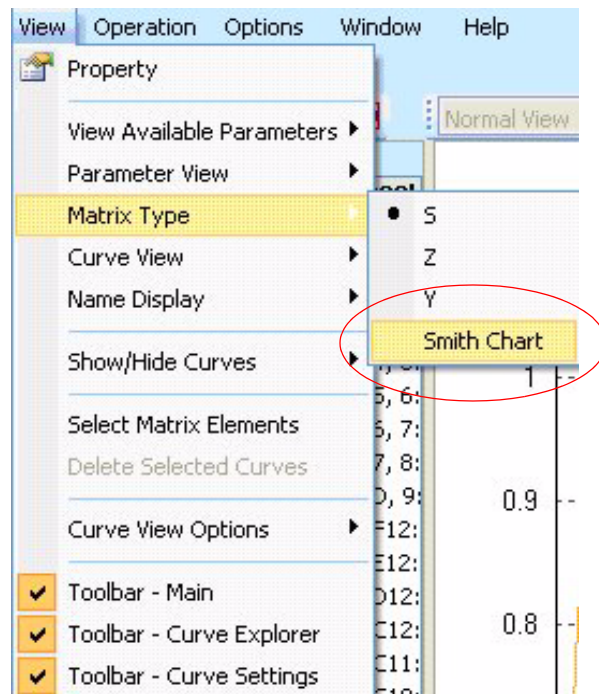
SMITH CHART VIEW OF THE S PARAMETER

Select **Smith Chart** from the Curve Source combo box;



or select Smith Chart from the menu

View > Matrix Type > Smith Chart



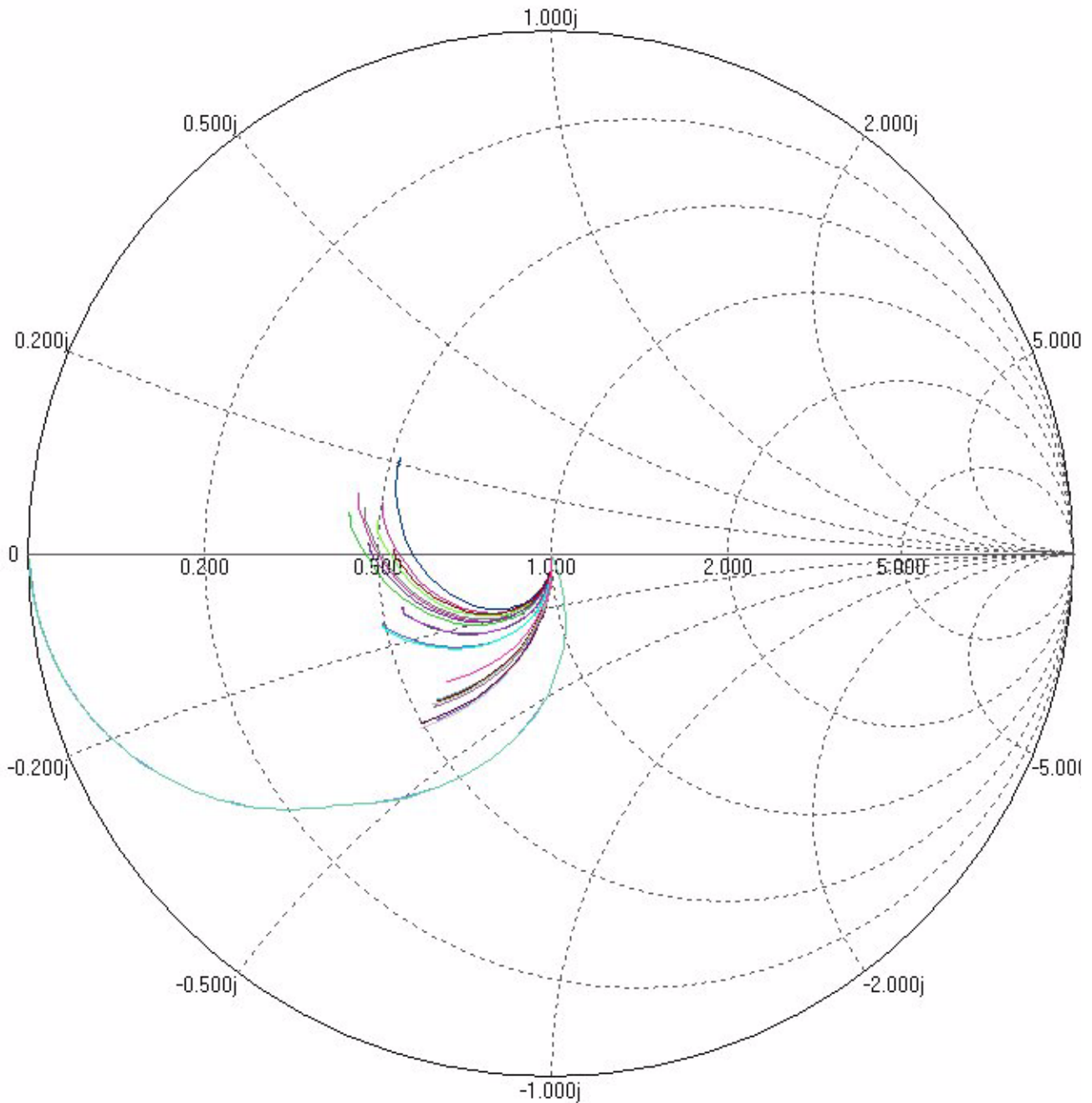
Overview

Use the toolbar to view the Smith Chart.

- Enlarge Reduce X / Y-scale buttons are disabled.
- Curve Method Selection combo box is disabled.



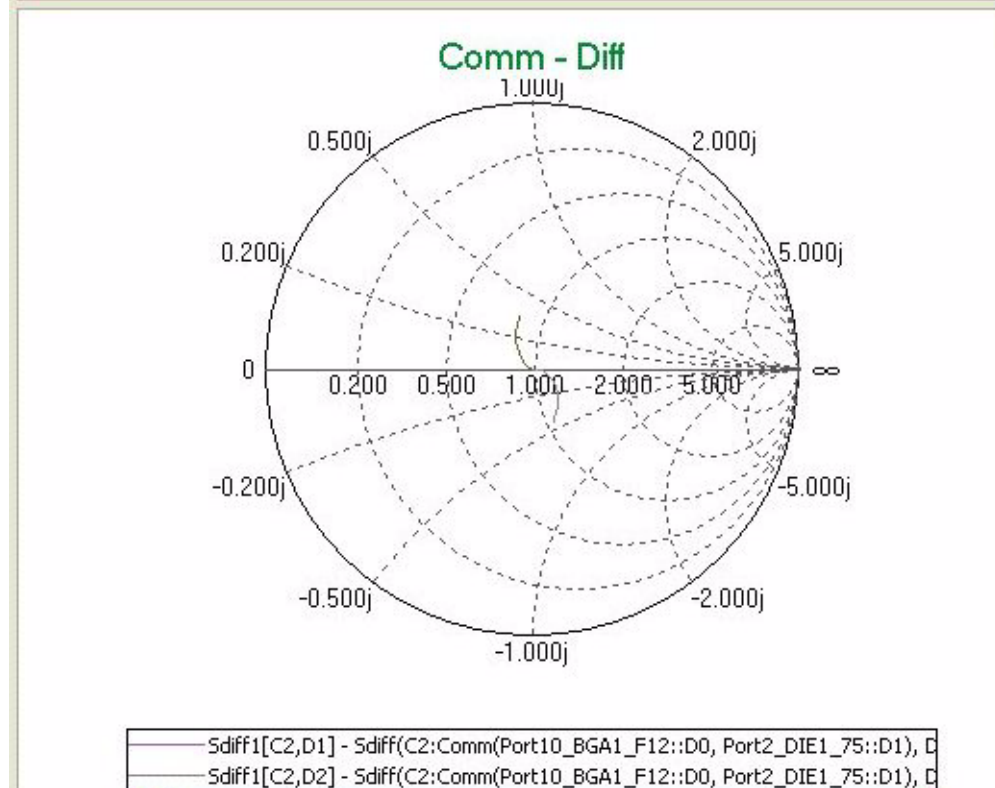
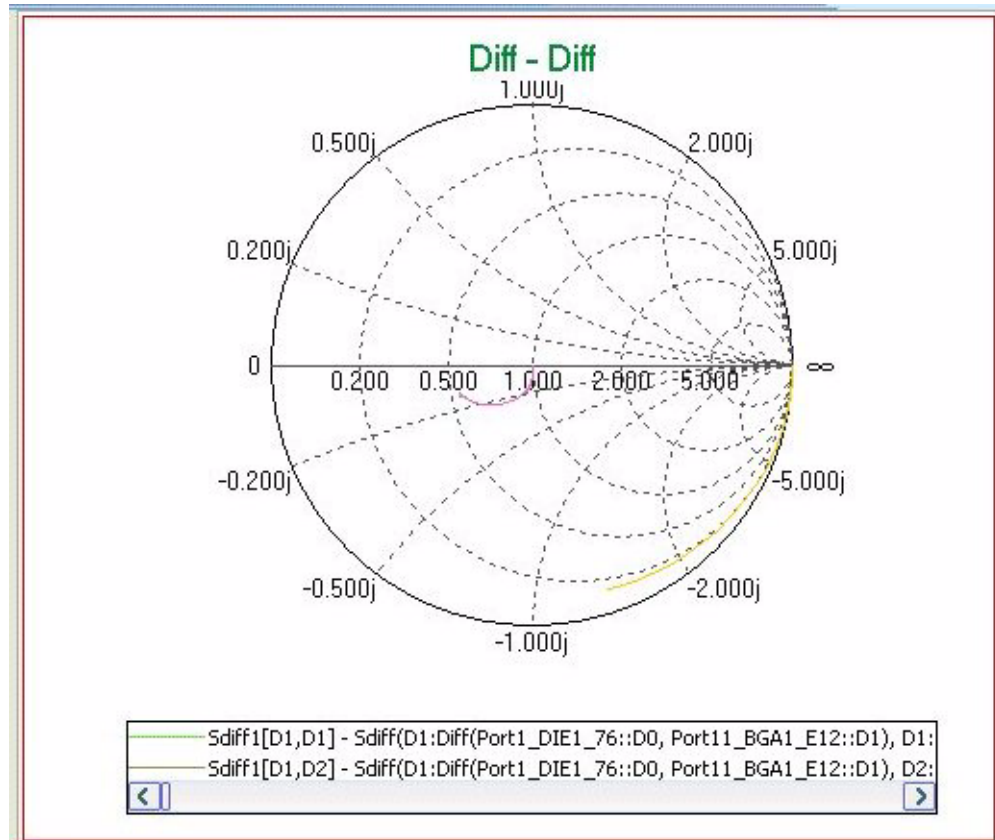
The Smith Chart in **Normal view** is shown in the following illustration.

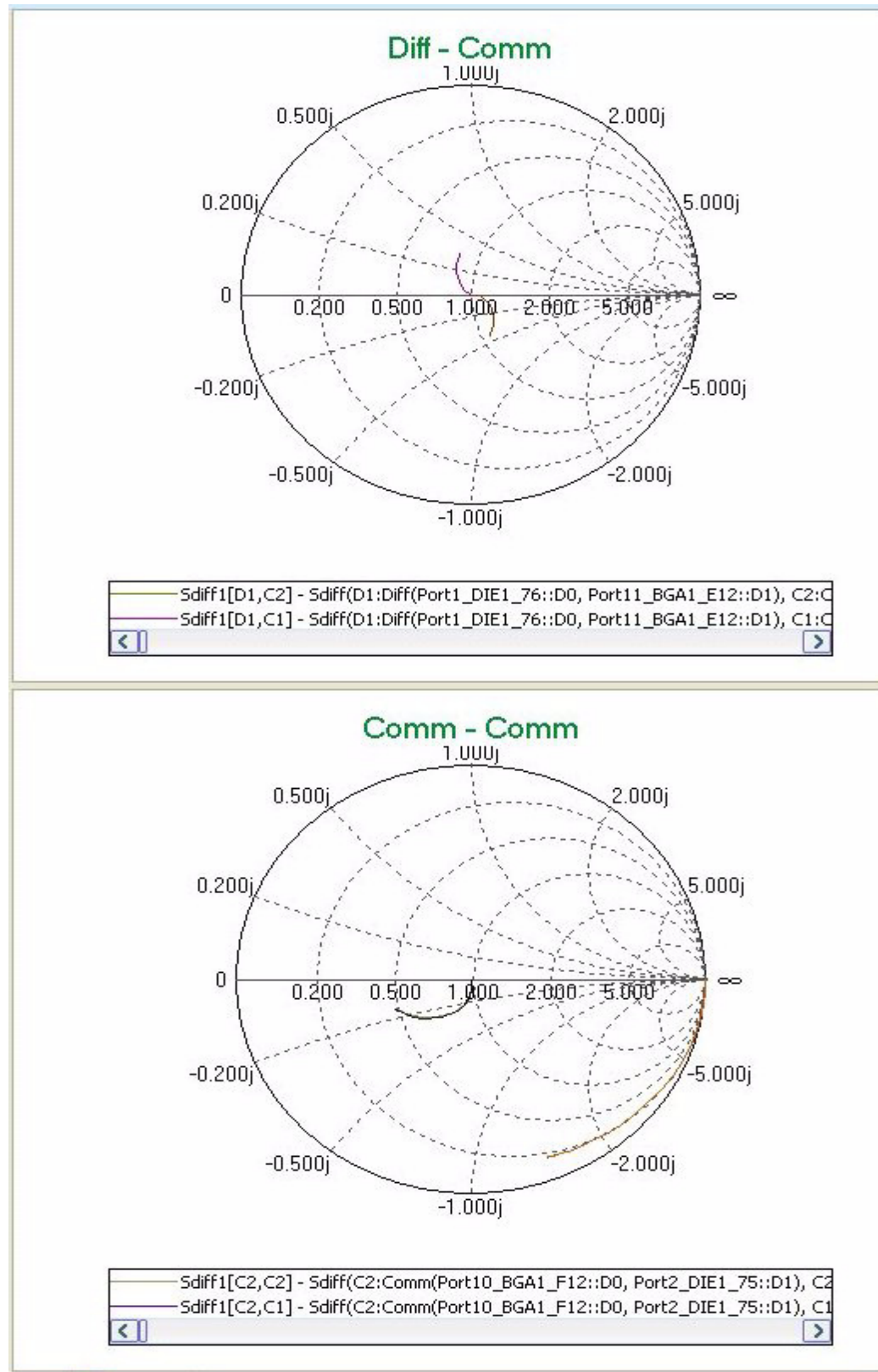


Differential Channel View

The Smith Chart plot in **Differential Channel View** is shown in the following illustrations.

- The first set shows **Diff-Diff** and **Comm-Diff**.
- The second set shows **Diff-Comm** and **Comm-Comm**.




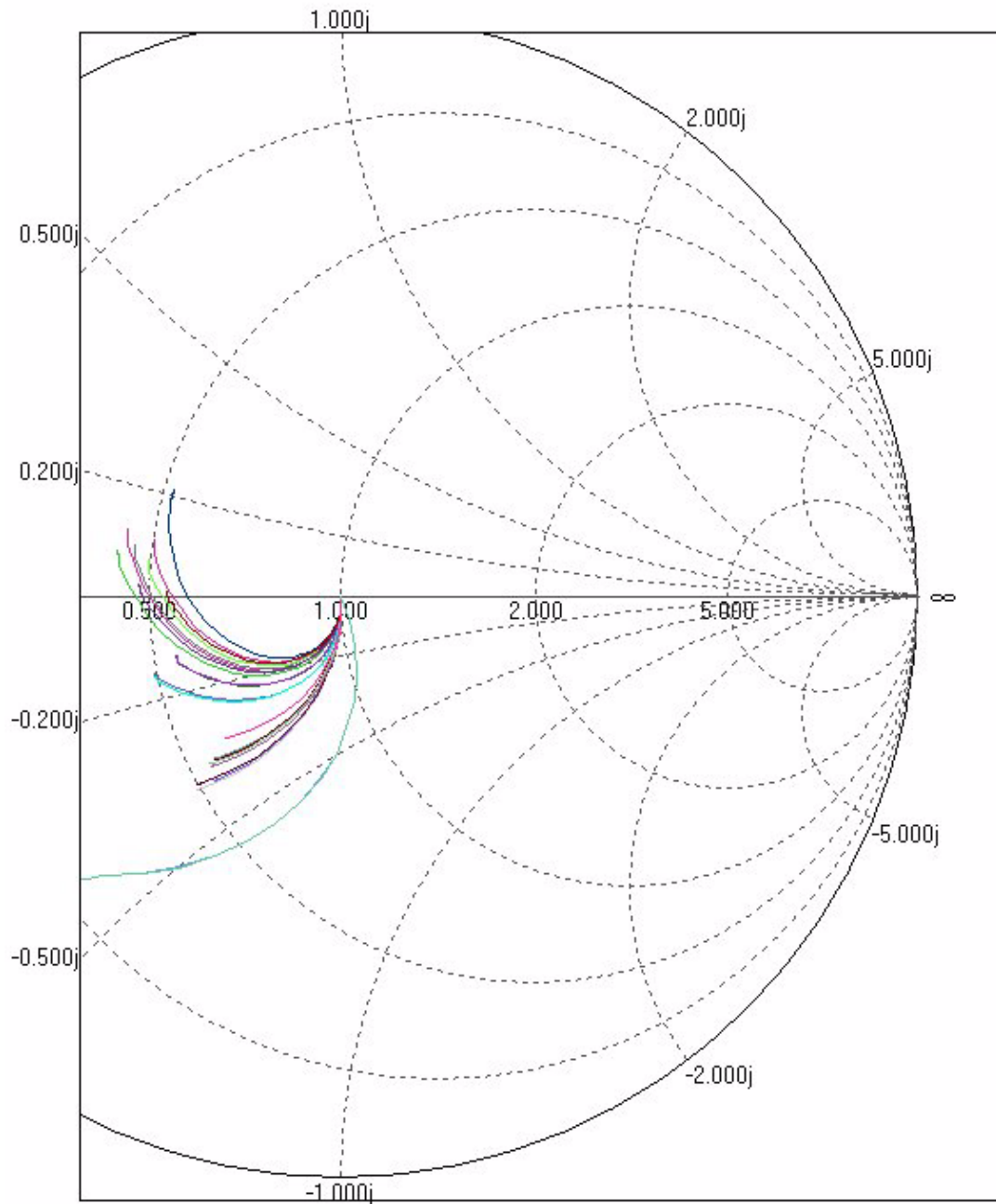


Manage the Curve View

The default plot display an unit circle, grid lines and curves. If the unit circle can be seen entirely, the square disappears; otherwise, it appears.

Move by Pan



1. Click the button  .
2. Press the plot.
3. Move to the desired position. Release the mouse button.




Zoom In and Out

Use the mouse wheel in a valid area to **Zoom** in and out of the plot to see the interested area. The grid line density of the Smith Chart automatically adjusts according to the Zoom status.

Area Select / Zoom Back

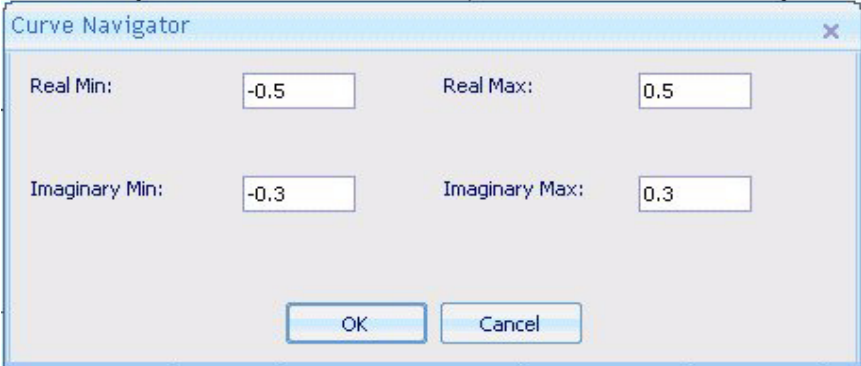
1. Click the button .
2. Select a rectangle in valid area to stand out the interested area.
3. The grid line density of the Smith Chart automatically adjusts according to the Zoom status.
4. Click the  button to **Zoom** back to the last area selected status.

Fit

Click the  button to bring the plot to the default setting.

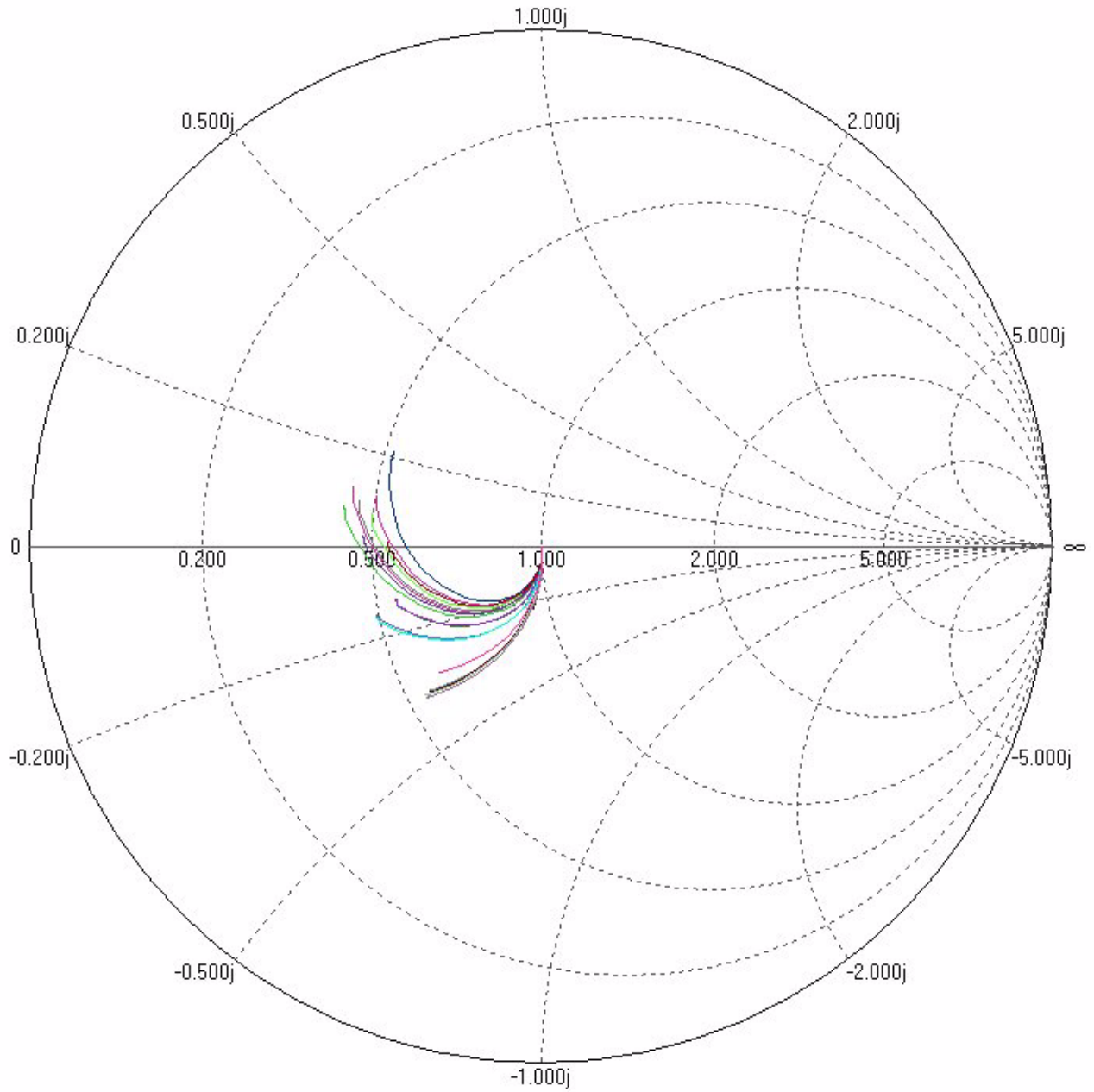
Navigator

1. Open a dialog.
2. Input the **Real Min** and **Real Max** values.
3. Click **OK**.



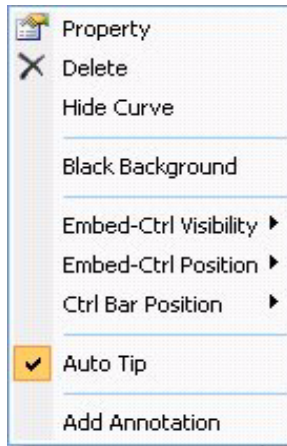
Parameter	Value
Real Min	-0.5
Real Max	0.5
Imaginary Min	-0.3
Imaginary Max	0.3

The plot is redrawn according to the new settings.



Menu Functionality

1. Move the mouse on a curve.
2. Right-click. The menu appears.



- **Add Annotation** — Click **Add Annotation** to switch the edit status to adding annotation.
- **Auto Tip** — Click **Auto Tip** to toggle the option of showing tip.
- **Black Background** — Click **Black Background** to toggle the background of the plot.
- **Delete** — Click **Delete** to delete the selected curve.
- **Embed-Ctrl Visibility / Position** — Float or resize the legend bar or rearrange the fixed position.
- **Hide Curve** — Click **Hide Curve** to hide the selected curve.
- **Property** — Click **Property** to set up the curve pattern of the selected curve.

Auto-tip

There are three sorts of tip in Smith Chart view:

- X-Axis
- Y-Axis
- Curve node

The autotip of the Curve node includes:

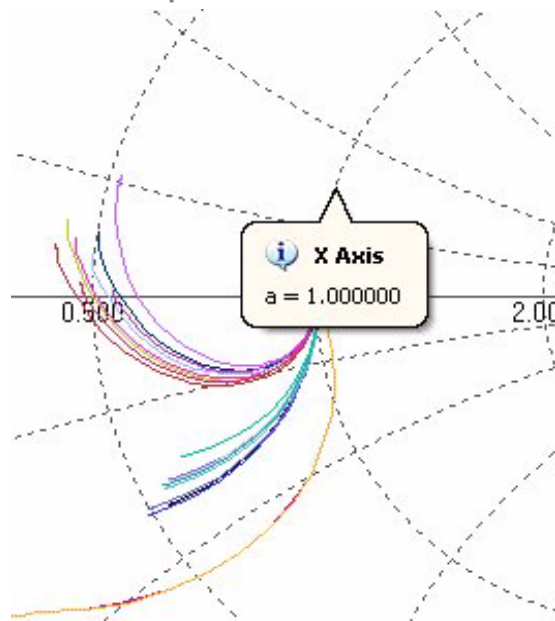
- Complex Value of the S Matrix Element at this Frequency.
- Frequency.
- Name of the S Matrix Element.
- Normalized Admittance Y.
- Normalized Impedance Z.
- VSWR.

Given the **S matrix** element value as s , the read-out is:

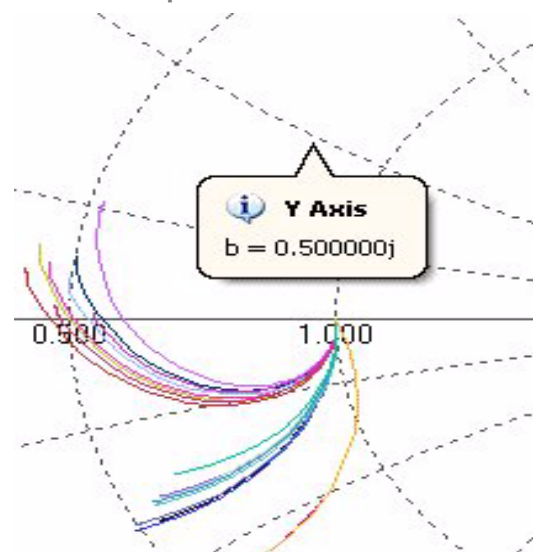
$$z = \frac{1+s}{1-s} \quad VSWR = \frac{1+|s|}{1-|s|}$$

$$y = \frac{1-s}{1+s}$$

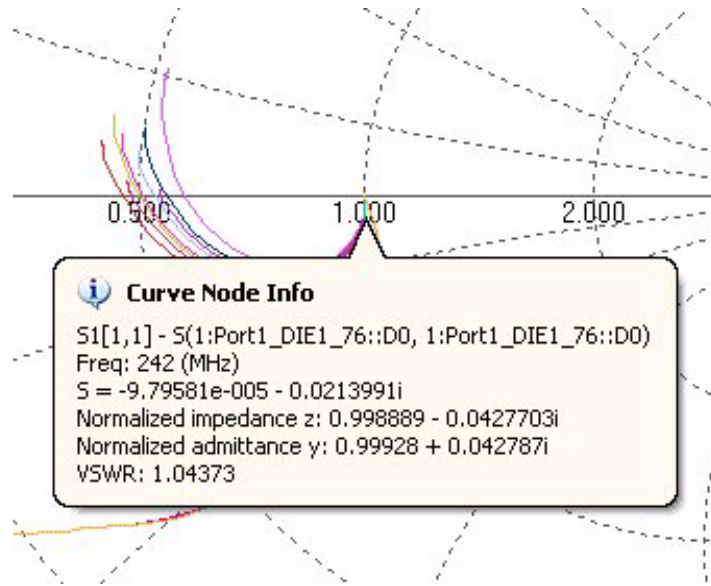
X-Axis Example



Y-Axis Example



Curve Node Info



Customize Workflow

This chapter introduces the customized workflow and takes you through customization process step-by-step.

LESSON ONE: UNDERSTANDING THE DEFAULT WORKFLOW

The default workflow now includes a customization option.

1. Click:

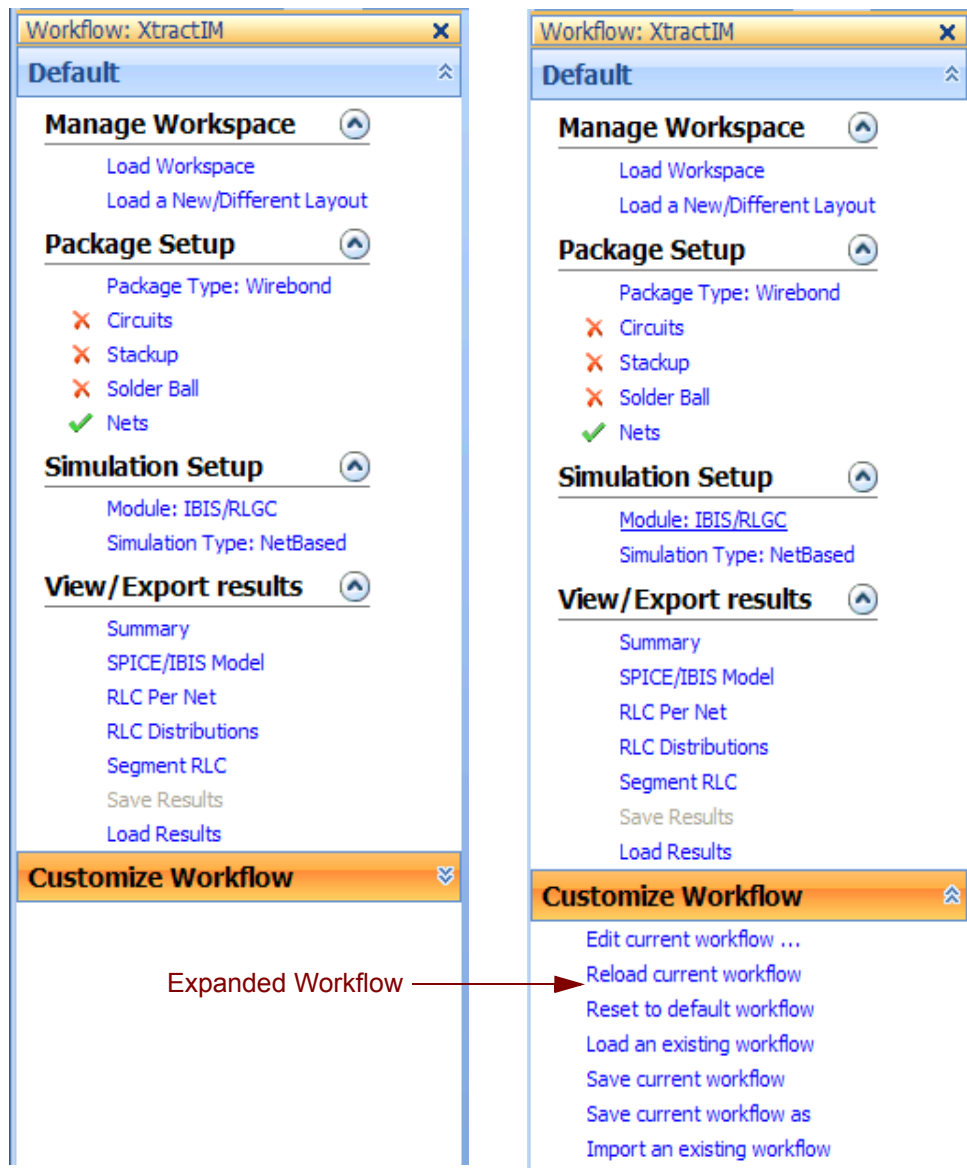
Customize Workflow

The Customize Workflow section in the Workflow expands and displays the customization options.

2. Click:

Edit current workflow

The Current workflow can be customized.

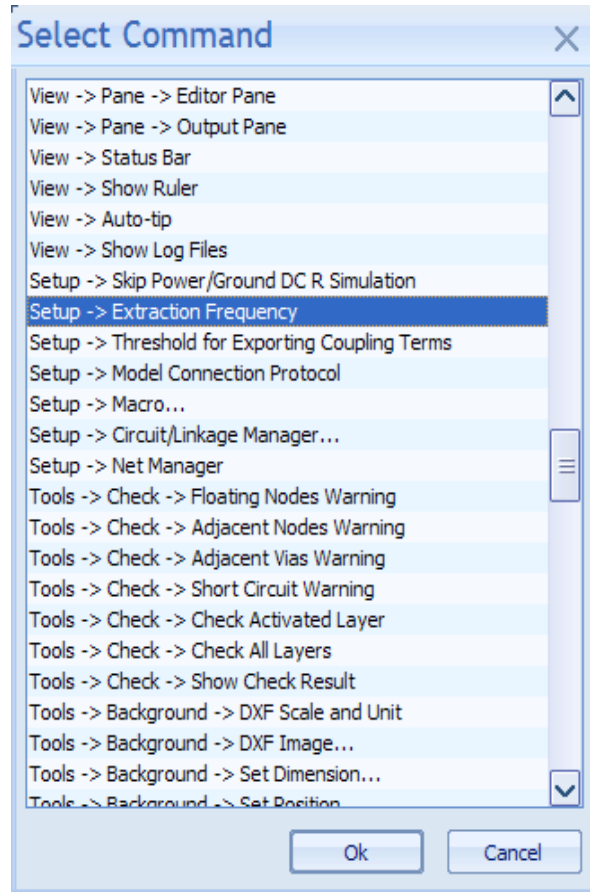
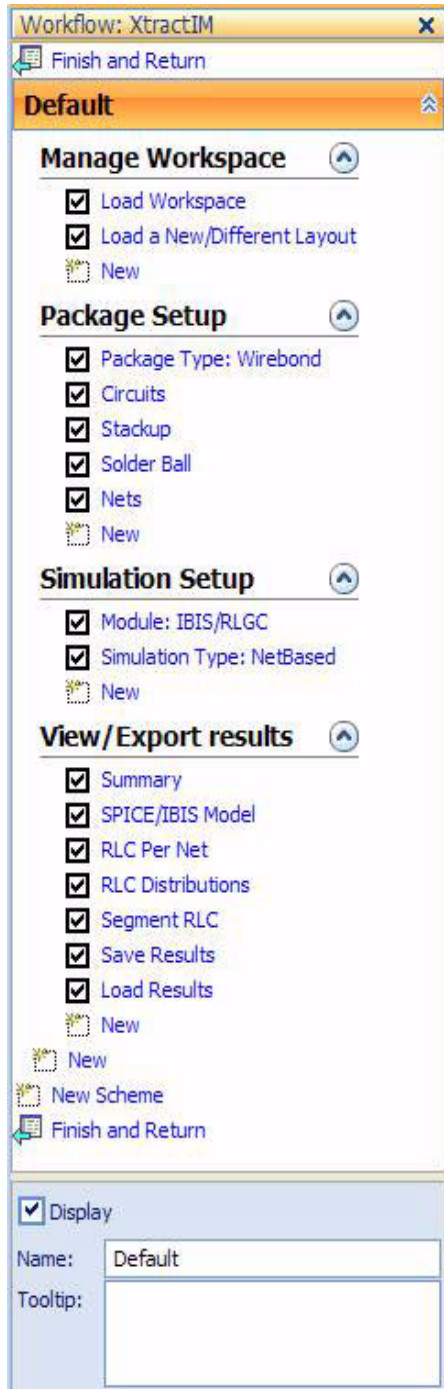


LESSON TWO: EDIT WORKFLOW

You can add, rename and change the sequence of the Workflow.

1. Click:
Simulation Setup > New
2. Click:
New Scheme
3. Change the name from **New Step** to **Extraction Frequency**.
4. Click **Set**.
5. Click:
Setup > Extraction Frequency
6. Click **OK**.
7. Click:
Package Type > Circuits
8. Change the name **Circuits** to a name your prefer (such as **Circuit Setup**).
9. In the Workflow pane, move **Nets** to:
Package Type > Wirebond

- 10. Click:
 - Finish and Return
- The new **Workflow** is updated.

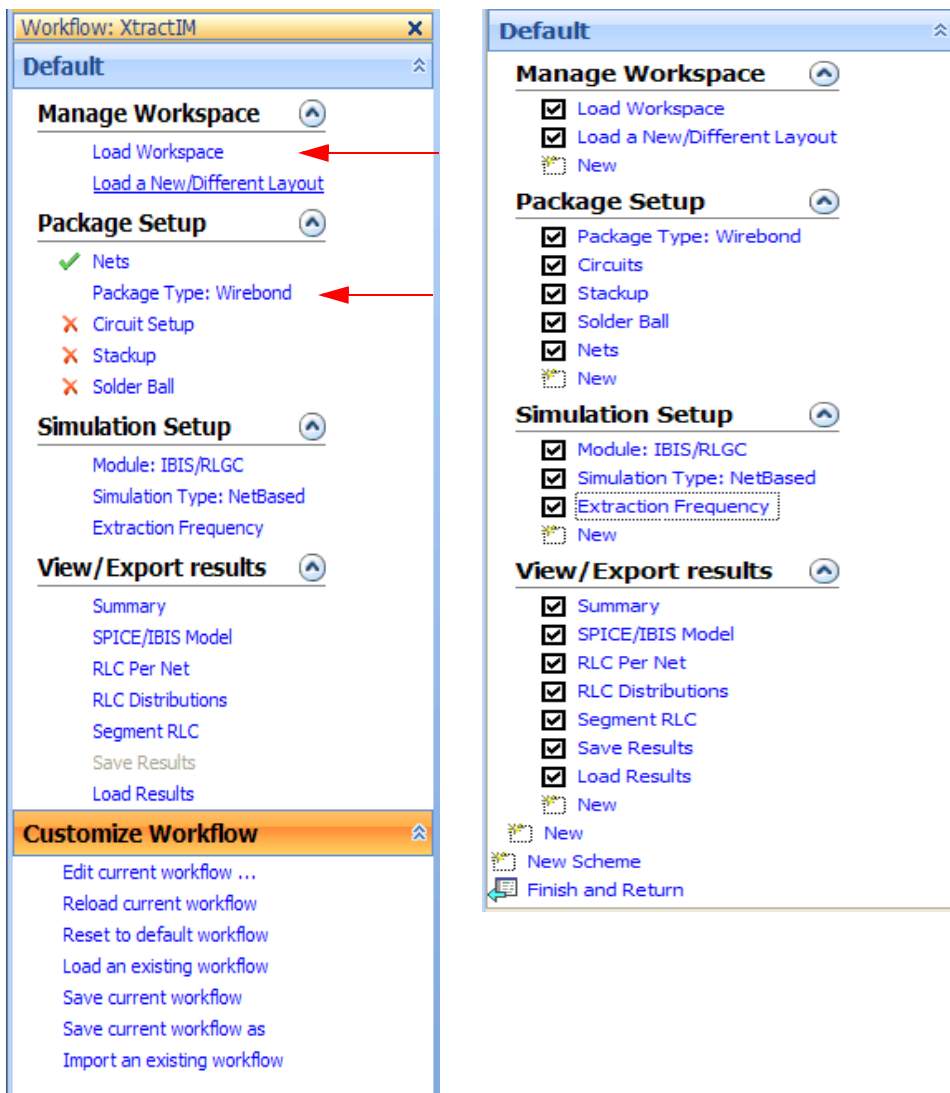


LESSON THREE: SAVE THE WORKFLOW

1. Click:
Customize Workflow > Save Current Workflow
An XtractIM.cfg file is saved in the same directory as XtractIM.exe.
2. Click:
Customize Workflow > Reset to default workflow
The workflow goes to **Default Workflow**.

Load Existing Workflow

1. After launching XtractIM, the saved XtractIM.cfg is automatically launched.
The customized workflow is loaded.
2. Select:
Customize Workflow > Reset to default workflow
The workflow goes to Default Workflow.
3. To substitute the current file, select:
Simulation Setup > Extraction Frequency
or select:
Import an existing workflow *.cfg file



Index

Symbols

. In these examples, review the relationship
25
.csv file 28, 29, 70, 71, 127, 205
.csv file names 85
.csv format 31, 127
.ibs format file 27, 127
.spd file 54, 72, 127, 132
.xml file 54, 72, 132
*_t.ckt 41
*.ckt 41, 70, 111
*.csv file 41
*.ibs file 41
*.pkg file 41
*.spd file 71
%Coupling Value 17

Numerics

2-die BGA package 64
30MHz 18, 124
3D display 4
3D view 15
3D view of the package 14

A

accurate mutual terms 16
action 79, 125
active layer 5
Actual number 146
actual value 171
add 239
Add a new band 219
Add a text string 223
Add Annotation 223, 234
Add button 202
Add Pair 209
added signal layer 12
AFS compression 204, 219
AFS format 77
Amplitude 223
analyze the electrical performance 131
apply the changes 207
appropriate fields 205
Attach DXF File 116
Attach Layout File 9
Auto Coupled Line 17
Auto Tip 223, 234

Automatic Output Sampling 219

B

background of the curve window 223
Bar 163, 164
Bar Chart 223
Batch Mode 47, 72
batch mode 129
Batch Mode Example 47, 72
batch mode simulation 47, 72, 129
before you begin the simulation 93
BGA 95
BGA circuit 94
BGA package 69
BGAs for multi-die stacked BGA packages 95
binary file 41, 70, 85, 128
bind 59
Black / White Background 223
Black Background 234
BMP file 204
BNP file 77, 202, 204, 219
board and package file formats 1
Board circuit 8, 11, 54, 56, 132
Board circuit 56
board side 63, 79
branch missing from net 68
branch R, L, and C 68
Branch RL file 70
BRD 3
Broadband Impedance 133, 139
Broadband Impedance 4
Broadband Insertion 5
Broadband module 114
Bump 7, 132
bump 60
Bump and Solderball diameters 53, 93
Bump data 54, 132
Bump Data setup 12
bump die package 59
bump layer 59
Bump Medium Layer 12
Bump/Solderball medium layer 54
Bumps 58
bumps 14
Bumps settings 12
Bump-to-BG DC Resistance 133

C

C of signal and power nets 4

C vs. Net Length 36
C(pF) 139
calculated curve 225
calculation result 225, 226
calculations 25, 80, 126
calculations for each net 64
Cancel the simulation 23, 63, 108, 125
Capacitance bar 34, 128
capacitance matrix 25
Capacitance plot 36
Capacitance values 34
capacitance/inductance 54
capacitance-to-ground 25, 126
captures all the coupling 18, 124
cell element 94
change 239
change extraction frequency 18, 107, 124
Change Port Setting 207, 208
Change Rise Time 162, 164
change several ports 207
Change the name 239
change the position of the docking 223
change the status of a single port 208
Change their status 208
Channel Filter dialogs 215
characteristic impedance 147
Check DC Current Density 133
check simulation results 5
choose the preferred view 144
circuit model 19, 124
Circuit Name Element 95
Circuit Section 75
Circuit Setup 239
circuit topology 114
Circuits 11, 56, 121
Circuits data 11, 56
circuits setup 11, 56
circuits to be extracted 90
circuit-to-circuit paths 4
color 157
color icon 203
Color Map 170
commands 5
Comm-Comm 228
Comm-Diff 228
compare the network parameters 224
complete the setup procedure 11
completing the simulation 47
Complex value 234
Component Name 154, 155, 158,

159
Conductance 25
conductance 31
conductance is very low 126
conductivity 7, 53
Conductivity of the outer leads 122
connection settings 208
connection status 208
Context menu 202, 207, 209
context menu 202
Continue 23, 63, 79, 108
Continue the simulation 23, 63, 108, 125
conventions 1
Convert 120
convert narrow shapes 120
Copy 207
coupled 17
Coupled lines 17
coupled lines 17, 18
Coupled Lines Edit pane 16
coupled trace 17
coupled transmission line sections 17
Coupling Coefficient Table 158
Coupling Coefficient 158, 159
Coupling Coefficient in Layout 159
Coupling Coefficient Plot (collapsed) 155
Coupling Coefficient Plot (expanded) 158
coupling elements 41
coupling neighbors 19, 124
couplings 160
Create a curve 225
create a package simulation 5
create a simple expression 224
Cross Probe Feature 153
Crosstalk 216
crosstalk 5, 17
Crosstalk among all Signal Nets 160
Ctrl Bar Position 223
Current Density 167
current value scale 170
Current workflow 238
Curve 157
Curve color 222
Curve Copy 224
curve legend 205
Curve Method Selection 227
Curve node 234
curve node 234
Curve Node Info 236
Curve pane 202

Curve Property dialog 222
Curve Settings toolbar 218
Curve Source combo box 226
curve views 217
curves 231
curves are updated 222
customizable 238
customization option 237
customization options 237
Customize Workflow 237, 241
Customize Workflow section 237

D

data 124
DC R of Each Path File 70
DC Resistance 29, 70, 128
DC_R 4
default name 224
default names 205
default percentage threshold 19, 124
default setting 76
default settings 205
default value 107
Default Workflow 241, 242
default workflow 237
defective design 23, 125
Define Differential Ports 209
Delay 66
Delay plot 36
Delay vs. Net Length 36
Delete 234
Delete button 209
Delete key 203
Delete the band 219
demonstration examples 1
design 3
Diagonal Element 25
diagonal element 25, 126
diagonal elements of the matrix 202
DIE 94, 95
DIE and BGA side 94
Die- and Board circuit 35
Die circuit 56
die circuit 59
Die Side 139
Die side 23, 63
Die to Board Circuit 150, 152
Die-Board mis-match 23, 63, 79, 108, 125
Die-circuit 8, 54, 132
Die-side 79
Die-toBGA1 67
Diff-Comm 228

Diff-Diff 228
different channel setting 213
different name 62
Differential Channel View 215, 228
differential channel view 217, 218
differential channel view pane 217
differential pair 209
differential pair definitions 218
differential port 209
Differential Port Setting Dialog 214
differential ports 209
directory 129
discrete frequency samples 204
display 146
display all results 139, 142
display area 223
display changes 172
display curves id 220
display names 205
Display Results 66
display results 166
displayed layers 5
docking 223
documentation 1
Drivers 3
DSN 3
DXF 115
DXF file 117
DXF format 118

E

Edit current workflow 237
Edit Pane 6
edit the name 225
edit the name to any string 206
edit the reference impedance 207
Edit the value 219
edit your layout 5
editing the comment 204
Editor Pane 5
electrical performance assessment 4
electrical performanc 3
Electrical Performance Assessment Workflow 131
electrical threshold parameter 17
element name 205
Embed-Ctrl Visibility / Position 234
empty signal layer 11
enabled cell 162, 164
Enbed-Ctrl Position 223
Enbed-Ctrl Visibility 223
End Component 155, 158
end of the solder ball 12

ending frequency 219
Enlarge Reduce X / Y-scale 228
equal voltage 136
errors 80
Examine what nets are mis-matched 23, 63, 108, 125, 133, 135
Excel .csv file 205
existing file 8
existing workspace file 73
export stage 124
Exporting Mutual Terms Example 19
Expression Calculation 225
Expression Calculation mode 224
Expression Manage 226
Expression Manager 225
extension .ckt 127
extension .pkg 127
extracted 88
extracted R, L, and C 68
extraction 16
Extraction Frequency 124, 239, 242
Extraction Frequency band 73
Extraction frequency points 114
extraction stage 18, 124

F

far-end crosstalk 39
Far-ended Crosstalk assuming the Rise Rime is 100 ps 161
FEXT 36, 39
File name window 70
Files of type field 87
final frequency sampling 219
Finish 11
Finish and Return 240
finish the setup 56
Flip-Chip 54, 55
Flip-Chip package 11, 12, 54, 56
Flip-chip package 132
floating 223
frequenc 82
Frequency 139, 234
frequency band 219
frequency curves 202
Frequency of Extraction 124
frequency point number 76
Frequency Range 75
frequency truncation 204
full matrix value 128
functionality 3

G

generate RLC models 16
green 62
grid line density 232
grid lines 231
Ground Net 16, 124, 139
Ground Net as the reference net 16
Ground Nets 16, 124
ground nets 27

H

heights 53, 59
Heights of the leads 122
Heights of the lower part 122
H-elements 107
Hide Curve 234
Histogram View 163, 164
horizontal and vertical marker lines 223
horizontal and vertical measure lines 223

I

IBIS / RLGC Module 7
IBIS Model 127
IBIS Model is saved 27
IBIS package 27
IBIS package model 127
IBIS package model files 41, 129
IBIS pin model files 41, 129
IC packages 3
ignoring mutual capacitance 19, 124
Impedance 154
Impedance in Layout 154
Impedance Plot (collapsed) 150
Impedance Plot (expanded) 152
Impedance Table 154
inductanc 19, 124
Inductance 146
inductance 35, 124
Inductance and Capacitance 139
inductance and capacitance 25
Inductance and Capacitance Matrix Example 25
Inductance bar 34, 128
inductance is 0.005 124
Inductance Matrix 25
Inductance plot 36
Inductance values 34
information of the network 205
Inner Lead Converter 119, 120
input boxes 202

input information 5
Insert a C4 Bump Medium Layer 12
insert a frequency point 219
insert a Leadframe layer 121
Insert a medium layer standing 122
Insert a signal layer 12
Insert Under 57, 121
Insertion and Loss 165
Insertion and Return 135
Insertion Loss 165, 216
interaction mode 94
Interactive Mode 132
Interconnects 3
isolated curve 225
isolated curve names 224
Isolated Curve pane 222, 224
isolated curves 224
isolated trace 17
Iteration Mode 113

L

L and C 41
L and C coupling elements 129
L vs. Net Length 36
L(nH) 139
last area selected status 232
Layer Name column 57
layer options 57
layers are inserted 12
LayerView window 80
Layout 159
Layout Area 5
layout error 6
layout error messages 6
layout file 8, 132
Layout files 54
Layout Selection Window 5
Layout Window 5
Layout window 146
Leadframe 122
leadframe 118
leadframe file 115
left-to-right 163, 164
length 53
Length of lower leads 122
Length of upper leads 122
Line pattern 222
Line style 222
Line width 222
linear scale 223
Load 88, 202
Load a New/Different Layout 9
Load an existing layout 116

Load Result window 174
Load Results 43, 129
load saved results 43, 71, 129
load the Package Structure 9
load the Package Structure 116
load the saved results 43
Load/Unload buttons 71
Loaded Curves 43, 129
loaded network 218
loaded networks 204
loaded results 43, 71, 129
loading capacitance 25, 126
log scale 223
lower frequency 75
lumped together 127

M

manual. 94
Manually convert selected shapes to traces 120
manually perform a Save 208
Marker 223
Marker size 222
Marker type 222
Match 208
matrices 25
matrix corresponding to a BNP file 202
matrix corresponding to a Touchstone file 202
matrix element name 205
Matrix Element Selection 202
matrix element unique ID 224
matrix elements 203, 224, 226
matrix entry 204, 207
matrix operations 204
matrix pane 218
matrix pane select 204
matrix value 33
Max 232
Maxwell Capacitance 127
Maxwell capacitance 25, 126
Maxwell Capacitance Matrix 25, 126
Maxwell capacitance matrix 25
MCM 3
Measure 223
medium layer 12
medium parameters 58
Menu Bar 5
menu bar 5
Mesh DIE 94
metal layer 41

metal layer. 33, 128
Min 232
minimum 124
minimum values 68
mis-matched nets 23, 63, 79, 109, 125
Mixed Mode Matrix 215
Mixed Mode Matrix in Differential Channel View 216
Mixed Mode Matrix in Normal View 215
mixed mode network parameters 216
mixed mode parameters 218
mixed-mode network parameters 209, 218
Mode Definitions 217
model files are saved 27, 127
modified in the network parameter display 209
modified information 204
modify a design 5
More Information 23, 63, 79, 108, 109, 125
More Information window 23, 63, 79, 109, 125
multi-conductor transmission lines 17
multi-die circuit 56
Multi-Die, Stacked-BGA package 4
Multiple BNP/Touchstone files 202
multiple rows 40
multi-sections circuit model 114
Mutual C 67
Mutual Capacitance 160
mutual capacitance 19, 124, 147
mutual capacitance / inductance 124
Mutual capacitance with other nets 25
mutual capacitance with positive values 25, 126
Mutual Inductance 31, 126, 160
mutual Inductance 25, 126
mutual inductance 27, 127, 147
Mutual Inductance and Capacitance 161
mutual inductance and capacitance 5
Mutual L 67
mutual L and C 4
Mutual loop inductance 25
Mutual Terms 31, 126
mutual terms 19, 124

N

NA2 3
narrow shapes 120
near-end coupling coefficient 147
Near-ended Crosstalk 146
Net as victim 163, 164
Net Coupling Summary 150
Net i 80
Net Impedance Summary 149
Net Length 66
net length 4, 28, 127
Net loop inductance 4
Net Manager window 16, 124
Net Name 168
net name 82
Net Name and Coupling Coefficient i 159
Netlist 156
Nets 124, 239
nets are mis-matched 79
nets for extraction 54
nets setup 16, 124
network 204, 209
network in the matrix pane 208
network name 205
network parameter files 202
Network Parameter Matrix 202
network parameters are not saved 208
network parameters are saved 219
Network Property dialog 205
new curve 224
New icon 9
new network 207
new network added 208
New Step 239
newly-added signal layer 58
NEXT 36, 39, 163, 164
No Outer Lead 118
no view for conductance 126
node as reference 94
Node Name 146
Normal View 215
Normal view 228
normal view 217, 218
Normalized admittance y 234
Normalized impedance z 234
number of elements 27

O

object display 5
Observation Ports 139

observe results 25, 64, 80, 126
off-diagonal elements 25, 126
One Pin Model in IBIS Fomat 41
One Summary Content in Excel
Format 41
Open 208
open 140
open a dialog 232
Open button 202
open circuit exits 94
Open Impedance 139
Open Layout File 62, 78, 108, 125
Optimized Broadband Module 73
optimized circuit 80
Option 1 94
Option 4 94
Options 2 & 3 94
Outer Lead only 121
output circuit 107
output data 41, 70
output files 41, 47, 71, 129
overlaid for each layer 171
overlaid on the Layout 159
overlaid on the layout 170
overlay features 174
overlay results 170

P

package model files 41, 129
Package name 26
Package Setup 88
package simulation setup 9, 54, 94
Package Type 9, 118, 239
package type 8, 132
parameter matrix type 224
Parital Outer Lead 118
Partial 3D View 15
Partial Outer Lead 118
passivity enforcement 209
Path File 70
path is from Die to Board 148
PCB medium layers 58
PCB medium thickness 122
physical layout 170
Pi-model 41, 90, 129
pin at the board side 23, 108, 125
pin at the Die side 23, 108, 125
Pin Groups 97
Pin Model
 Excel format 28, 127
Pin Node Name 145
pin nodes 98
Pin resistance and inductance 5

Pin-Based 95, 96
Pin-based extraction 94
Plane Current Density 172
Plane IR drop 5
Play button 63, 79, 108, 125, 138
PLC model 4
plot is redrawn 233
plot style 223
PNG file 204
POPbottom 57
port combo boxes 209
port pairs of differential channel setting and single channel ports 217
port reduction operation 208
port references 98
port setting 213
Port Setting Example 214
ports 202
Power Net 139
Power Nets 16
power nets 27, 28
Power to Ground Inductances and Capacitances 133
power/ground distribution systems for packages 3
PowerNets 124
pre-defined patterns 202
pre-saved result 86
Present Curves 43, 129
present results 43, 71, 129
Present Results window 170
proceed with the simulation 23, 79, 109, 125
project file 62, 78, 125
Properties 205
Property 222, 234

Q

Qualified nets 95

R

R and L elements 76
R, L, and C data 127
R(mOhm) or L(nH) 145
R/L/C full matrix 31, 127
Radius of lower arc 122
Radius of upper arc 122
Receivers 3
rectangle 232
reduce the size of the output circuit 18, 124
re-enter your settings 12, 13
Ref Ground Net 139
reference element 97
Reference Ground Net 139
reference ground net 16, 124
reference impedance input box 207
Reference Net 95, 98
Reference Net Node 96
Reference Nets 160, 165
registry 205
Remain as a port 208
remove these frequencies 218
rename 239
Reorder the list 26
Replace button 202
report results 5
Report Template 45
Reset to default workflow 241, 242
Resistance 25, 31, 126, 146
Resistance bar. 34, 128
Resistance using all Power and Ground Nets as Reference 161
Resistance values 34
result 85
result file 41, 70, 85
result output file 41, 70, 129
result_spd_file_name.eim 70, 128
result*.eim file 41, 70, 129
results 138
Results Overlay 170
results to be displayed 147
Return key 219
Return Loss 5, 166, 216
reverse crosstalk 17
Rise Time 17, 40
Rise Time Value 17
RLC 16, 33, 128
RLC curves 4
RLC Distributions 33, 128
RLC distributions 33, 128
RLC extraction 124
RLC Full Matrix 41, 129
RLC Full matrix 31, 127
RLC of each metal layer 129
RLC vs. NetLength 36
RLCG 23, 79, 108, 125
RLGC models 4
RLGC Module 4
RLGC Module Pin-based Extraction 113
RLGC SPICE model 90
RLGCcircuit extraction 94
Rotation icon 144
run a simulation 5
run simulation 23, 63, 79, 108, 125

S

- S chart 82
- S Imaginary 80
- S matrix element 234
- S matrix element value 235
- S parameter curves 207
- sampling frequency 209
- save a file 144
- Save as 78, 125
- Save as Default 205
- Save Curves dialog 204
- Save Extractor Result window 40, 70, 128
- Save Layout File 62, 125
- save layout file 21, 62, 78, 125
- save layout file under different name 62, 78, 125
- Save Result 85
- Save Results 173
- save results 25, 31, 40, 64, 70, 80, 126, 128
- save the workspace 137
- Save Workspace 62, 78, 125
- save workspace 62, 78, 125
- save workspace under different name 21
- save your entries 12, 13
- save your selection 9, 55
- saved file 27
- saved model 27, 127
- sections 80
- Segment RLC 33, 35, 41, 128
- Segment RLC values 34, 128
- Select a frequency 221
- select a pair of nets 209
- select a region 15
- Select as Board circuit 56
- select multiple matrices 203
- select multiple ports 207, 208
- select Package 121
- select shapes 120
- Select the circuits 75
- Select the nets 8
- select the next action 63, 108
- select the top cell 40
- selected nets of a package 3
- Self- and Total-loop Inductance 133
- Self C 66
- Self capacitance 25
- Self Inductance 25
- Self L 66
- Self loop inductance 25
- self R 4
- Self-C 28, 127
- self-C 41
- Self-capacitance 31, 126
- Self-inductance 31, 126
- self-inductance 147
- self-L 4, 41
- self-R 41
- set Solder Ball data 54
- Set the C4 Bump data 8
- Set the Solder Ball 8
- set up a simulation 5
- set up Rise Time and %Coupling 17
- Set With Default Parameters 17
- Setting Output Factors 63
- settings 12, 13, 122
- setup circuits 54
- Setup extraction frequency 9
- Setup Solder Ball 63
- setup stackup 54
- Setup the circuits 8
- Setup the Stackup 8
- Short 140, 208
- Show / Hide 223
- Show X-axis in Log Scale 223
- Show Y-axis in Log Scale 223
- signal net 16, 124, 128
- signal net length 41
- signal net length, self-R, self-L, self-C 129
- Signal net name 70
- Signal Nets 147, 165
- signal nets with single-pin 35
- signal velocity 147
- signal, power and ground nets 4
- Signal\$ layer 121
- Signal\$Bottom 57
- Signal\$Bottom layer 11, 57
- Signal\$Top 12
- Signal\$Top layer 12, 58
- simulation continues 23, 125
- simulation progress 5
- simulation result 204
- Simulation setup 54
- simulation setup 8, 54, 94
- simulation time 76
- Simulation Type 95, 96
- single BGA 54
- Single Channel Matrix 215
- single channel matrix 213
- Single Channel Matrix in Normal View 215
- Single Net 157
- Single net average error in S 82
- Single Net Coupling Coefficient 157
- single or stacked BGA packages 3
- single port 208
- single port select 207
- single section 80
- single transmission line algorithm 17
- Single\$1 layer 119
- Single-BGA 118
- single-BGA package 4, 7
- Single-Die 118
- Single-die Single-BGA package 148, 160
- Single-die Single-BGA packages 165
- single-ended network parameters 216, 218
- Sink Current 136
- Sink Side 136
- SIP 3
- smallest-to-largest 163, 164
- Smith Chart 226, 227, 232
- Smith Chart view 234
- Solder Ball 13
- Solder Ball data 54
- Solder Ball Data setup 13
- Solder Ball Medium Layer insert 11, 57
- Solder Ball Medium Layers 12
- Solder Ball settings 13
- solder balls 14
- solderball 58
- Solderball data 132
- Solderball Medium layer 132
- Sort 145
- S-parameter 76, 77, 88
- S-parameter element 80
- S-parameter error 80
- S-parameter Examples 81
- S-parameters 114
- S-parmeter 80
- S-parmter errors 80
- SPD file 174
- SPD format 7, 53, 93, 115, 118
- SPD formats 3
- special design 23, 125
- specialized panes 5
- SPICE capacitance 25, 126
- SPICE Capacitance Matrix 25, 126
- SPICE capacitance matrix 25
- SPICE circuit 41, 73
- SPICE circuit files 41, 70, 129
- SPICE Circuit model 84
- SPICE equivalent circuits 4

SPICE file 129
SPICE Model
 Circuit Topology 85
SPICE model 27
SPICE Model is saved 27
SPICE Model. 111
SPICE Mutual Capacitance 31, 126
SPICE sub-circuit 27, 127
SPICE/IBIS Model 28, 29, 127
SPICE/IBIS model 27, 127
spreadsheet 5
stacked BGA 54
Stackup 132
Stackup information 7, 53, 93
Stackup window 122
Standard Setup 122
Start Component 155, 158
start over 13, 124
start the extraction 23, 63, 79, 108, 125, 138
starting frequency 219
Status Bar 5, 6
step-by-step instructions 1
Stop 23, 63, 79, 108
strongest coupling coefficient 155
strongest coupling neighbors 124
strongest couplings 157
Sub Matrix 202
Sub Matrix option 202
Summary 26, 41, 68, 111
Summary of Extracted Results 68
Summary view file 86
Summary, extracted results 26, 127
Sweeping Mode 219
sweeping mode 76
system requirements 1
system-level analysis 3

T

T-circuit 27, 127
Thickness of the leads 122
Three Segment RLC in Excel Format 41
Threshold for Exporting Coupling Terms 124
time delay 41
T-model 41, 90, 114, 129
Toggle the plot style 216, 223
Toggle the sub windows 223
Toggle the X axis 223
Toggle the Y axis 223
tool bar 5
tools on the workspace 5

Total horizontal length 122
Total Near-ended Crosstalk of each Net as Victim 161
Total NEXT Histogram View 163, 164
Touchstone format 77, 204
trace 18
Trace and Wirebond Impedance 150
Trace coupling 146
Trace Coupling Threshold 16
trace coupling threshold 16
Trace nets 17
traces 120
traces are identified 17
traces belonging to several nets 17
tree item is collapsed 217
trigger the visibility 203
Truncate 218
Ts (ps) 162, 164
Type 88
Type column 88
Type Workflow 132
typical workflow 94

U

unique curve name 224
unique ID 202
unit circle 231
unload a loaded result 43, 129
Unload Extractor Result icon 43, 71, 129
UPD 3
upper frequency 75
Use a Saved Expression 226
Use As Reference Element 97
Use Reference Element 95, 97
Use Reference Net 95
Use Reference Node (auto) 95
Use Reference Node (manual) 95

V

valid area 232
value type 223
VDD 88
version 5
vertical marker lines 223
vertical measure lines 223
Via Counts 166
Via Counts Table 166
Via Current 168, 170
Via Current Histogram View 167
Via Current Table 167

Via resistance 35
Via starting layer 166
via starting layer 35
victim 146
view near-end 39
view the detailed results 158
view the results 174
View the Stackup 58
View/Export Results 128
View/Exports Results options 111
visibility control options 203
visibility of the sub windows 223
Voltage distribution 171
VSWR 234

W

Width of lower leads 122
Width of upper leads 122
Wirebond 54, 55
Wirebond Package 118
With Outer Lead 118
Workflow is updated 240
workflow pane 5, 6
workflow pane area descriptions 5
Workspace file 174
Workspace pane 108
Workspace toolbar 108
workspace toolbar 78
worst-case capacitive loading 25, 126

X

X-Axis 235
XML 174
XtractIM 131, 174
XtractIM.cfg 242
XtractIM.cfg file 241
XtractIM.exe 241
XtractIM.exe file 47, 72
X-Y coordinates 5, 146

Y

Y-Axis 235
yellow via 78

Z

Zoom 232
Zoom status 232
Z-parameter 139

