# **XtractIM Tutorial**

### Product Version 16.6 July 2014

Document Updated on: July 11, 2014

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# Chapter

# Introduction

Welcome to the XtractIM Tutorial. This manual is designed to give you a brief introduction to the XtractIM tool by providing real life examples and demonstrations so you can understand some of the basic concepts. The XtractIM tool is part of a complete suite of tools for package design.

#### SYSTEM REQUIREMENTS

Please refer to *Installation Guide* to check the system requirements.

#### How to Use This Guide

The XtractIM Tutorial provides demonstration examples and step-by-step instructions on how to get the desired results.

Go through the sections in each chapter in order. Perform all steps and study the examples.

#### **ADDITIONAL DOCUMENTATION**

In addition to this document, refer to the following documentation for additional information.

- XtractIM User's Guide describes in detail the features and functionality of XtractIM.
- *Translators User's Guide* describes translations from various types of board and package file formats to Sigrity's SPD format.

#### **CONVENTIONS USED IN THIS GUIDE**

CONVENTION	USE
Bold	GUI text, special names, terms (window names, buttons, menus, etc.)
Arial	Examples

CONVENTION	Use
>	Menu hierarchy

### HOW TO CONTACT TECHNICAL SUPPORT

We are committed to helping you in using XtractIM. If you have any questions, contact the <u>Cadence</u> <u>Online Support</u>.

# Chapter

## **Overview**

This chapter introduces the functionality of XtractIM.

#### **ABOUT XTRACTIM**

XtractIM extracts the most common electrical models of IC packages according to IBIS (I/O Buffer Information Specification) as well as SPICE netlist of electrical models. XtractIM also supports electrical performance assessment on signal and power/ground distribution systems for packages. This feature helps you analyze the quality of the design.

These models can be used for system-level analysis including:

- Assessing the electrical performance of IC packages
- Drivers
- Interconnects
- Receivers

XtractIM can handle lead-frame, flip-chip packages and wirebond packages with 3D bonding wire profiles. The package can be single- or multi-die, and single- or stacked-BGA packages.

It can extract models of full packages or selected nets of a package.

Its interface is compatible with data files in various formats, including UPD, MCM, .BRD, .SIP, NA2, DSN, and SPD formats.

XtractIM has two modules in extraction: IBIS/RLGC and Optimized Broadband. XtractIM supports both net-based and pin-based RLC extraction for single or multi-die and single or stacked BGA packages.

#### **MODEL EXTRACTION**

Model Extraction Mode includes

- RLC / IBIS Module
- Optimized Broadband Module

#### **RLGC / IBIS Module**

The RLGC / IBIS Module for single-die, single-BGA package provides with the capability to:

- Generate IBIS package pin RLC model
- Generate IBIS package RLC (Resistance, Inductance and Capacitance) matrix model with coupling between signal, power and ground nets
- Generate net length, DC\_R, delay of each signal net
- Generate SPICE equivalent circuits of package RLGC models of different topologies (Pi or T), including coupling among signal, power and ground nets
- 2D and 3D display of RLC curves and distributions, including coupling between nets

The RLGC Module for Multi-Die, Stacked-BGA package provides the capability to:

- Generate DC\_R of signal, power, and ground nets along each of circuit-to-circuit paths
- Generate self R, self-L, C of signal and power nets along each of circuit-to-circuit paths
- Generate mutual L and C of signal and power nets along each of the circuit-to-circuit paths
- Generate branch RL and total C of signal and power nets
- Generate SPICE equivalent circuits of package RLGC model including coupling among signal, power and ground nets

#### **Optimized Broadband Module**

The Optimized Broadband Module works for both single-die, single-BGA and multi-die stacked-BGA packages. It provides users with the following capabilities:

- Display of the original S-parameter and compact circuit model S-parameter
- Export the S-parameter model in Sigrity compact formats (BNP)
- Extract and display of S network parameters
- Optimized Broadband RLC circuit model extraction with options of selecting circuit models

#### **ELECTRICAL PERFORMANCE ASSESSMENT**

Electrical Performance Assessment includes two systems.

- Power / Ground Distribution System
- Signal Distribution System

#### **Power / Ground Distribution System**

- Net loop inductance of Power Nets referring to each of the Ground Nets
- Broadband Impedance of each Power Net referring to its best Ground Net

- · Plane IR drop, Plane current density and Via-current checking
- Per Pin resistance and inductance of power / ground net viewing from die-side

#### **Signal Distribution System**

- Trace layput checking: Impedance and strongest coupling of single-ended Net vs. section-bysection Net-length
- Net couplings: mutual inductance and capacitance, total near-ended crosstalk for each Net as a victim
- Broadband Insertion and Return Loss

#### THE XTRACTIM WINDOW

The new workspace is made up of two main areas.

- Layout Area Large area with a black background
- Workflow Pane Left side of the screen

Within these two main areas you'll find toolbars, menus, and smaller, specialized panes. You'll use all the tools on the workspace to create a package simulation.

- Editor Pane A spreadsheet. Users can easily input information into the pane for simulation setup or check simulation results in the pane
- Layout Selection Window Controls the active layer, displayed layers and the object display on or off
- Layout Window Where you edit your layout
- Menu Bar The pull-down menus provide the commands you need to modify a design, set up a simulation, run a simulation, check results and report results
- Status Bar Shows the version information, the current X-Y coordinates of the cursor and the simulation progress
- **Tool bar** Gives you quick access to common XtractIM commands
- Workflow Pane Lists all the workflow tasks. Tasks of the same type are sorted and listed together. When a task is clicked, details associated with that task appear in an Editor pane



**Using the Toolbar Icons** 

- **1.** Click on **Workflow Pane** . The Workflow pane pops out or hides.
- 2. Click on Edit Pane . The Status Bar pops up or hides.
- 3. Click on Layout Error Check . The layout error messages, if any, are shown or hidden.



# Chapter

# IBIS / RLGC Module: Net-Based Simulation Single-Die Single-BGA Packages

This chapter takes you through the steps to use the XtractIM tool IBIS / RLGC Module in the simulation of a single-die, single-BGA package.

#### **PREPARE FOR THE SIMULATION**

Collect this information before you begin the simulation.

- Have the Bump diameters, length, heights and conductivity ready
- Have the Stackup information ready
- Make sure your files have been translated into SPD format

#### **LESSON ONE: SIMULATION SETUP**

#### **Overview**

Follow these steps to perform a typical workflow in Interaction Mode.

Mode	Extraction
Man	age Workspace 🛛 🙆
	Load Workspace
	Load a New/Different Layout
Pack	age Setup 💿
	Package Type: Flip-Chip
<ul> <li>✓</li> </ul>	Components
<ul> <li>✓</li> </ul>	Stackup
<ul> <li>✓</li> </ul>	Bumps
<ul> <li>✓</li> </ul>	Solder Ball
<ul> <li>✓</li> </ul>	Nets
Simu	ulation Setup 🛛 🙆
	Module: IBIS/RLGC
	Simulation Type: Net-Based
View	ı/Export Results 🛛 🙆
	Summary
	SPICE/IBIS Model
	DLC Dev Net
	REC Per Net
	RLC Per Net RLC Distributions
	RLC Per Net RLC Distributions Segment RLC
	RLC Per Net RLC Distributions Segment RLC RLC vs. Net Length
	RLC Per Net RLC Distributions Segment RLC RLC vs. Net Length CrossTalk (Single-Ended)
	RLC Per Net RLC Distributions Segment RLC RLC vs. Net Length CrossTalk (Single-Ended) 3D View
	RLC Per Net RLC Distributions Segment RLC RLC vs. Net Length CrossTalk (Single-Ended) 3D View Histogram
	RLC Per Net RLC Distributions Segment RLC RLC vs. Net Length CrossTalk (Single-Ended) 3D View Histogram CrossTalk (Diffpair vs Single-Ende
	RLC Per Net RLC Distributions Segment RLC RLC vs. Net Length CrossTalk (Single-Ended) 3D View Histogram CrossTalk (Diffpair vs Single-Ende 3D View
	RLC Per Net RLC Distributions Segment RLC RLC vs. Net Length CrossTalk (Single-Ended) 3D View Histogram CrossTalk (Diffpair vs Single-Endi 3D View Histogram
	RLC Per Net RLC Distributions Segment RLC RLC vs. Net Length CrossTalk (Single-Ended) 3D View Histogram CrossTalk (Diffpair vs Single-Ende 3D View Histogram Save Results
	RLC Per Net RLC Distributions Segment RLC RLC vs. Net Length CrossTalk (Single-Ended) 3D View Histogram CrossTalk (Diffpair vs Single-Ende 3D View Histogram Save Results Load Results

- **1.** Load an existing workspace file (.xml file).
- **2.** Load a layout file (.spd file).
- **3.** Select a package type. Choose from:
  - Flip-chip
  - Single BGA (Board Grid Array)
  - Stacked BGA
  - Wirebond
- 4. Setup the components. You can select or deselect **Die component** and **Board component**.
- 5. Setup the Stackup.
- 6. Set parameters for the Bump or Solderball medium layer.
  - Set the Bump data if it is a flip-chip package.
  - Set the Solder Ball data.
- 7. Select the nets for extraction.

8. Setup extraction frequency and capacitance or inductance output control.

#### Load Workspace and Layout File

1. Launch XtractIM.

The XtractIM main window opens. Two icons are available:



2. Click the New icon to create a new workspace or select:

Workspace > New

- 3. Click Load Workspace in the Workflow pane and browse to load an existing workspace file.
- To load the Package Structure, click Load a New/Different Layout in the Workflow pane. The Attach Layout File window opens.

Attach Layout File	×
Apply current workspace setup	
Please choose the type of layout to load	
Load an existing SPD file	
O Load an existing DXF file	
OK Cancel	

Select Package Type

Click Package Type: Flip-Chip in the Workflow pane to select package type.
 The Package Setup -> Package Type pane appears at the bottom of the window.

Package Setup	-> Package Type	
• Single Die	O Stacked Die	O Side-by-side Die
Single BGA	O Stacked BGA	O Leadframe
O Wirebond	• Flip-Chip	OBoth
ОК	Cancel	

2. Click OK to save your selection.

The following example shows the workspace with the package type: Single Die, Single BGA, Flip-Chip.

#### Lesson One: Simulation Setup



#### **Setup Components**

**1.** Click **Components** in the **Workflow** pane to set up the Components data for a Flip-Chip package.

The Wizard pane opens.

	Model Name	Die/Board/Cap/Othe components Type
C1	Cap0402	
C2	Cap0402	
C3	Cap0402	
C4	Cap0402	
C5	Cap0402	
C6	Cap0402	
C7	Cap0402	
111		
BGA1	untitled pac	Select as Die
50/12	anddea_paen	Deselect as Die
		Select as Capacitor
		Deselect as Capacitor

- 2. Right-click the desired component and select Select as Die from the pop-up menu list.
- 3. Click Next.
- 4. Right-click the desired component and select it as a **Board** component.
- 5. Click Finish to complete the components setup.

#### Setup Stackup

1. Click Stackup in the Workflow pane.

The Layer Manager -> Stack Up window opens.

- 2. Right-click Signal\$Bottom layer.
- 3. Insert a Solder Ball Medium Layer.
- 4. Insert an empty Signal layer.

5. Insert a medium layer standing for a PCB medium layer. All layers are inserted under Signal\$Bottom.

The added Signal layer is located at the end of the solder ball.

#### Setup Bump Medium Layer

- 1. Right-click on the Signal\$Top layer.
- 2. Insert a Bump Medium Layer above Signal\$Top.
- **3.** Insert a **signal layer** above Signal\$Top. The added signal layer is the ending of the Bump. Both the Bump and Solder Ball Medium Layers are created.

#### **Setup Bumps**

 Click Bumps in the Workflow pane to set up the Bump data for a Flip-Chip package. The Package Setup -> Bumps pane appears at the bottom of the window.

Package Setup ->	Package Setup -> Bumps 🗙 🗙								
Layer Name	RefDes	Dmax (mm)	D1 (mm)	D2 (mm)	HT (mm)	Material	Conductivity (S/m)	Dama Madal	
Bump01	U1	0.1	0.1	0.1	0.1		5.8e7	Bump Model	
						aluminum			
						copper			
						silver		$\left( \leftarrow D_{\max} \rightarrow HT \right)$	
						Solder60 Solder63			
ОК	Cancel								

**2.** Input the settings for the Bumps.

Maximum Diameter: Dmax (mm)

D1 (mm)

D2 (mm)

Height: HT (mm)

Conductivity (S/m) (or click **Material** and choose material from the drop-down list, the conductivity will be automatically input.)

NOTE	XtractIM includes a material file in library (in the default intallation path:
NOTE:	<install_dir>\SpeedXP\Library\material\). It can be edited.</install_dir>

- 3. Click **OK** to save your entries.
- **4.** (Optional) Click **Cancel** if you do not want to save your changes, or if you want to start over and re-enter your settings.

**NOTE!** Perform the same steps to set up a wirebond package.

#### **Setup Solder Ball**

1. Click Solder Ball in the Workflow pane to setup the Solder Ball data for a Flip-Chip package. The Package Setup -> Solder Ball pane appears at the bottom of the window.

Package Setup -> Solder Ball 🗙 🗙								
Layer Name	RefDes	Dmax (mm)	D1 (mm)	D2 (mm)	HT (mm)	Material	Conductivity (S/m)	Solder Ball Model
Solderball01	BGA1	0.5	0.4	0.4	0.4	aluminum copper gold silver Solder60 Solder63	S.8e7	H → D2 → H
ОК	Cancel							

2. Input the settings for Solder Ball.

Maximum Diameter: Dmax (mm)

D1 (mm)

D2 (mm)

Height: HT (mm)

Conductivity (S/m) (or click Material and choose material from the drop-down list, the conductivity will be automatically input.)

- 3. Click OK to save your entries.
- 4. (Optional) Click Cancel if you do not want to save your changes, or if you want to start over and re-enter your settings.

#### **Viewing 3D Layout**

**Full 3D View** 

Select

View > 3D View > Full 3D View

+XtractIM - FlipChip.ximx	- [fli	pchip.spd Lay	er View]				
🧇 Workspace Edit	Vi	w Mode	Setup	Tools	Wind	ow	Help
🗋 📂 🔒 🚽 🔟 🕨		Zoom			•	9	🕶 🔛 🚰 👘 👻
Extractor Result		Show			•		
All Enabled Net(s)		Layer Selectio	in			R	📑 📭 🗙 🖻
* 18 📼 🚥 📕 🕈		3D View			×		Full 3D View
		Toolbars			•	_	Partial 3D View
Workflow: XtractIM		Pane			•	-2	0 2 4
Model Extraction	4	Status Bar					
Manage Workspace	4	Show Ruler					
Load Workspace		Auto-tip					
Load a New/Differen		Open New N	etwork Par	ameter Di:	splay		
Package Setup		Show Log File	25			$\mathbb{N}$	

The 3D view of the package is displayed showing the bumps and solder balls.



**Partial 3D View** 

1. Select

View > 3D View > Partial 3D View

2. Use the mouse to select a region (shown as a box outline in the following image).



The 3D view of the selected region is shown in the display.



#### Setup Nets

- 1. Click Nets in the Workflow pane to open Net Manager.
- Choose any desired nets for RLC (Resistance, Inductance and Capacitance)extraction.
   You can move the Signal Net into and out of Power Nets and Ground Nets if you wish.
- 3. Choose only the desired Ground Net as the reference net.

At least one Ground Net must be selected to act as a **Reference ground Net**.

- **4.** Set the Trace coupling threshold to a proper level to generate RLC models with accurate mutual terms.
- 5. Switch to Show Coupled Line. The Coupled Lines Edit pane opens.
- 6. Set the Trace Coupling Threshold to a proper level.



Laura Calastian Mat Mana

## NOTE!

The Coupled Lines tab controls only the coupling threshold between Traces.

Via coupling and wirebond coupling are always considered.

#### **Rise Time and %Coupling**

When Traces are identified as **coupled lines**, the crosstalk between these lines is calculated during the simulation. Based on electrical threshold parameters, Traces belonging to several nets are automatically identified and analyzed as coupled transmission line sections.

- Two Traces are said to be coupled if their reverse crosstalk exceeds the %Coupling
- Coupled lines can be selected after the relevant Traces have been placed. Coupled lines are treated as multi-conductor transmission lines
- An **isolated Trace** is modeled by the single transmission line algorithm

For a given **Rise Time**, the accumulated coupled section lengths between Trace nets should be long enough for forward crosstalk to exceed the %Coupling.

- **Rise Time Value** Must be greater than 0. Default value is 200 ps
- %Coupling Value Must be  $0 < value \le 100$ . Default value is 5%

**NOTE!** If the coupling parameters - %Coupling and Rise Time - are left blank, the trace-to-trace coupling is not calculated during simulation.

#### **Setup Rise Time and %Coupling**

- 1. Click on Coupled Line tab to set up *Setup Extraction Frequency* to identify a coupled trace.
- 2. Select the nets you wish to edit.
- **3.** Right-click to open the pop-menu.
- 4. Select:

Set With Default Parameters



5. Select Show Coupled Lines in the Net Manager.

The Trace identified as coupled lines is displayed in the **Layout View** pane, as shown in the following screen.



#### **Setup Extraction Frequency**

**1.** To change the Extraction Frequency, select

Setup > Extraction Frequency

The Extraction Frequency window opens.

Extraction Frequency			×
Extraction Frequency:	30	MHz	ОК
			Cancel

2. Input the value of extraction frequency in the field.

The default value is 30MHz.

3. Click OK.

#### **Setup Threshold for Exporting Mutual Terms**

XtractIM provides an option to reduce the size of the output circuit during the export stage. Besides, XtractIM captures all the coupling during the extraction stage.

1. Select

Setup > Threshold for Exporting Coupling Terms

The Threshold for Exporting Coupling Terms window opens.

Threshold for Exporting Coupling Terms	×
Number of strongest neighbors to export 10	
In addition,	
Ignore mutual C if the ratio of mutual over self terms is less than 0.005	
Ignore mutual L if the ratio of mutual over self terms is less than 0.005	

2. Input the number of strongest coupling neighbors to be kept in the circuit model.

The default number of strongest coupling neighbors is 10; which means outputting the 10 strongest neighbors (including self).

**3.** Ignore mutual capacitance or inductance if the ratio of mutual terms over self term is less than a percentage.

The default percentage threshold for ignoring mutual capacitance and inductance is 0.005.

#### **Exporting Mutual Terms Example**

If the mutual capacitance or inductance is less than the 0.5% of the minimum of the two self-capacitances and inductances,

then

XtractIM does not output the mutual capacitance or inductance

NOTE	Threshold for Exporting Coupling Terms is used to:
NOTE!	<ul> <li>Ignore mutual capacitance or inductance less than a specified net-to- net coupling threshold.</li> </ul>

**Output RLC Matrix in .csv Format** 

1. To output RLC matrix in .csv format, select

Tools > Options > Edit Options...

The **Options** window opens.

Options	×	2
Options          File <ul> <li>General</li> <li>File Manager</li> <li>Save Options</li> <li>Hotkeys</li> </ul> Layout <ul> <li>Grid and Unit</li> <li>View</li> <li>Processing</li> <li>Trace</li> <li>Error Checking</li> <li>Translator</li> <li>3D Layout View</li> <li>Display</li> <li>Quality</li> <li>Simulation (Basic)</li> <li>General</li> <li>Net and Coupling</li> </ul>	Change the 'Output SPICE Circuit' options in XtractIM   Output SPICE Circuit     Power-Ground net has partial inductance (Single-Die Single-BGA Net-based no Decap)     Net Name Included in Circuit Node Name   Keep All Coupling Terms to Power Nets   Export RLC Matrices   Output IBIS .pkg file for Multi-die Stacked-BGA Package   (Each .pkg model represents one-die to one-board path assuming other dies and board to be open/floating )	
General Net and Coupling Special Void Output SPICE Circuit Report Simulation (Advanced) Electric Models Mesh Nets and Shapes Field Solver Engine	<ul> <li>Do not Output T- and Pi-topology SPICE Model</li> <li>Include Decaps in SPICE circuit         <ul> <li>(If a circuit is selected as decap during workspace-&gt;circuit setup,</li></ul></li></ul>	
	Default Apply OK Cancel	

- 2. Click Output SPICE Circuit under Simulation (Basic).
- 3. Select the Export LC Matrices option.
- 4. (Optional) Select the **Do not Output T- and Pi-topology SPICE Model** option if you do not want these two SPICE models.
- 5. Click OK.

#### LESSON TWO: SAVE WORK AREAS

#### **Tool Bar**

There are four icons related with work areas saving.



ICON	DESCRIPTION
<b>2</b>	Open Workspace File
	Save all
•	Save Workspace File Save Layout File
<b>2</b>	Attach a layout file

NOTE	Saving the workspace automatically saves the .spd file.
	Saving the layout file does not automatically save the workspace.

#### **Workspace File**

To save the workspace under a different name, select

Workspace > Save As...

٨	W	orkspace	Edit	View	Mode
: 🗋		New			Ctrl+N
12	2	Open			Ctrl+O
•+		Save			Ctrl+S
Wor		Save As			
Мо		Close			
м		Print			Ctrl+P
		Print Prev	view		
		Print Setu	ıp		
Pa		Pause Sir	nulation		

#### **Layout File**

To save the layout file under a different name, select Workspace > Layout File > Save As...



#### **LESSON THREE: RUN THE SIMULATION**

#### **Start Simulation**

1. Click the Start Simulation icon <a>> on toolbar to start the extraction (simulation).</a>

XtractIM only extracts RLCG for a net which has at least one pin at the Die side and at least one pin at the board side.

At the beginning of the simulation, if some nets have Die-Board mis-match, a pop-up window appears.

Die and	d Board pins do	o not matcl	h X
	The pins of the die circuit Click More Information to	do not correspond see the list of misn	to the board circuit pins. natched pins.
	Enabled nets	: 19	
	Nets in ground group	: 1	
	Nets with pin-mismatch	: 1	
	Nets to be extracted	: 18	
	You may Continue or Sto	op the simulation.	
	Continue	Stop	More Information

- **2.** Select the next action.
  - **Continue** Continue the simulation
  - More Information Examine what nets are mis-matched
  - **Stop** Cancel the simulation

#### **Investigate Mis-matched Nets**

- 1. The More Information window lists all the mis-matched nets.
- 2. Investigate the mis-matched nets to see whether there is a special design or a defective design.
- 3. Decide whether or not to proceed with the simulation.
- 4. Choose Continue, Stop or More Information.

If 30 seconds pass and the user has not made a choice; then, by default, the simulation continues.

Die and	d Board pins do not match $ imes$					
The pins of the die circuit do not correspond to the board circuit pins. Click More Information to see the list of mismatched pins.						
	Enabled nets : 19					
	Nets in ground group : 1					
	Nets with pin-mismatch : 1					
	Nets to be extracted : 18					
	You may Continue or Stop the simulation.					
	Continue Stop More Information					
Enabled Nets in g Nets wit Nets to b	nets : 19 round group : 1 h pin-mismatch : 1 be extracted : 18					
Enabled Nets in g Nets with Nets to I Unmatch The form (1) Die c (2) Die c (3) Die c (4) Die c (1) Boar (2) Boar (3) Boar (4) Boar	nets : 19 round group : 1 h pin-mismatch : 1 be extracted : 18 med pins are listed below. hat of the list is [cktName, pinName, net_name]: ircuit (D1), D1-A4, vdd ircuit (D1), D1-A4, vdd ircuit (D2), D2-A2, vdd ircuit (D2), D2-A2, vdd d circuit (BGA1), BGA1-10, vdd d circuit (BGA1), BGA1-15, vdd d circuit (BGA1), BGA1-20, vdd d circuit (BGA1), BGA1-5, vdd					

# NOTE!

A file named Xtracted\_PinNode\_Info.log is saved on hard disk. This file records the total extracted node number of each circuit and, if available, the mis-matched information.

#### LESSON FOUR: OBSERVE AND SAVE SIMULATION RESULTS

XtractIM performs calculations for each net. The calculations include:

- Conductance
- Mutual capacitance with other net
- Mutual loop inductance
- Resistance
- Self capacitance
- Self loop inductance

The inductance and capacitance are matrices. In the Inductance Matrix, the Diagonal Element is the Self Inductance of each net. The off-diagonal elements are mutual Inductance.

There are two concepts of capacitance matrix:

- Maxwell capacitance matrix
- SPICE capacitance matrix
- Maxwell Capacitance Matrix Each diagonal element is the loading capacitance; for example, capacitance-to-ground when other nets are grounded. This represents the worst-case capacitive loading. Off-diagonal elements are mutual capacitance with negative values
- SPICE Capacitance Matrix Each diagonal element is capacitance-to-ground. Off-diagonal elements are mutual capacitance with positive values

In the examples, review the relationship between Maxwell capacitance and SPICE capacitance matrix.

#### Inductance and Capacitance Matrix Example

A simple group of four nets has the following inductance and capacitance matrix.

$\begin{bmatrix} L_{11} & L_{12} & L_{13} & L_{14} \end{bmatrix}$	$\begin{bmatrix} C_{11} & C_{12} & C_{13} & C_{14} \end{bmatrix}$
$L_{21}$ $L_{22}$ $L_{23}$ $L_{24}$	$C_{21}$ $C_{22}$ $C_{23}$ $C_{24}$
$\begin{bmatrix} L_{31} & L_{32} & L_{33} & L_{34} \end{bmatrix}$	$C_{31}$ $C_{32}$ $C_{33}$ $C_{34}$
$\begin{bmatrix} L_{41} & L_{42} & L_{43} & L_{44} \end{bmatrix}$	$\begin{bmatrix} C_{41} & C_{42} & C_{43} & C_{44} \end{bmatrix}$

**Capacitance Example** 

$$\begin{split} C_{ij} \left( SPICE \right) &= -C_{ij} \left( Maxwell \right) \\ C_{ii} \left( Maxwell \right) &= \sum_{j} C_{ij} \left( SPICE \right) \\ C_{ii} \left( SPICE \right) &= \sum_{j} C_{ij} \left( Maxwell \right) \end{split}$$

#### **Summary of the Extracted Results**

- 1. Click Summary in the Workflow pane.
- **2.** View the data for R, L and C.
  - Extraction Frequency
  - Full RLC Matrix
  - Maximum / minimum R, L, C
  - Nets Extracted
  - Package Name
- **3.** Reorder the list, if desired.

	Extractor Result		) 🔐 🔛 🕒 🖉				
Extractor Result							
[Version]	12.1.b1.02041						
[Date]	0.6						
[Package Name]	C:	I\Update1\Sp	peedXP\Samples\Xtract				
[Description]	C:	I\Update1\Sp	peedXP\Samples\Xtrac1 =				
[Nets Extracted]	10						
[Frequency of Extra	action] 30	MHz					
[Max R(mOhm)]	31	.2.934					
[Min R(mOhm)]	4.	54504					
[Max self-inductand	ce L(nH)] 8.	76833					
◀	111						
Net 🔺 Net	R(mOhm)	L(nH)	C(pF)				
	12.9943	1.02645	18.0999				
VDD_2 VDD_2	0	0	0				
VDD_2 VDD_3	0	0	0				
VDD_3 VDD_4	0	0	0				
VDD_4 VDDcore	0	0	0				
VDDcore Net_1	0	0	0				
Net_1 Net_2	0	0	0				
Net 2 Net_3	0	0.184293	0.406076				
Net 3	0	0.393493	0.438503				
Output	^	0.700440	0 503630		~		
* Processing natch02 Patc	h¢\/DD				~		
* Processing patch02 Patch	h\$VSS						
* Processing Patch\$VDD P	atch\$VSS						
* Processing Patch\$VSS Pi Connecting Circuits To Patches	atch01						
Handling Floating Circuits	-						
Modeling Pads							
Solving Package and Circuits							
Sindiction is in progress.					•		
Miscellaneous Mesh - Errors	s VariablesCheck						

#### **Save SPICE/IBIS Model Files**

Upon completing the simulation, both model files are saved in the same directory as the .spd file.

#### Save SPICE Model Files

The total number of elements in the circuit is displayed at the bottom of the window.

R, L, M, C and G where M is the mutual inductance

The SPICE Model is saved as a SPICE sub-circuit with the extension .ckt.

The SPICE model is a T-circuit.



#### **Save IBIS Model Files**

The IBIS Model is saved as an IBIS package model. The saved model has the extension .pkg.

An .ibs format file is saved. The saved file includes each single net's R, L, C.

All power nets and ground nets are lumped together.



#### **Load Pin Model in Excel Format**

- 1. Click Pin Model: Excel format in the SPICE / IBIS Model window.
- 2. A .csv file is loaded. The .csv file includes information for each signal net.
  - Net Length
  - Net Name
  - Pin Name
  - Self-R
  - Self-L
  - Self-C
  - Time Delay

Self-C is the Maxwell Capacitance. The information for power nets does not include net length.
actor Result							
View Model Select	ion						
SPICE T-model							
SPICE Pi-model			-^^^~	000			
					11111		
C Ibio pky model							
Pin model: IBIS f	ormat				1111		
-				ter de la terreta de la ter	1111		
Pin model: Excel	format				1100		
				and a deal of the			
O DC Nesistance							
PinName	NetName	NetLength(mm)	SelfR(Ohm)	SelfL(nH)	SelfC(pF)	Delay(pS)	
BGA1-G1: BGA1-	VDD 1		0.0156075	1.16316	19.0766	148.96	
BGA1-A10: BGA	VDD 2		0.0148735	1.04337	20,1058	144.837	
BGA1-G12: BGA	VDD 3		0.0149638	1.09652	19.914	147.771	
BGA1-M7: BGA1	VDD 4		0.0152309	1.05723	20.4667	147.099	
BGA1-K3: BGA1	VDDcore		0.00717351	0.370523	42.6992	125,782	
BGA1-L2	Net 1	9.88884	0.239083	6.94694	1,13387	88,7519	
BGA1-M2	Net 10	11.4717	0.284798	8.33932	1,28413	103,483	
BGA1-B11	Net 100	11.1565	0.273255	7.94035	1.24412	99.3918	-
BGA1-L1	Net 11	12.1041	0.300393	8.34175	1.39613	107.918	
BGA1-H4	Net 12	5.54869	0.12016	3.50787	0.838864	54.246	
BGA1-G5	Net 13	2.67495	0.0436108	1.68291	0.591901	31.5613	
BGA1-F1	Net 14	10.2331	0.247378	6.90269	1,1993	90,9857	
BGA1-F5	Net 15	3,73966	0.0699779	2.1132	0.646634	36,9657	
BGA1-D1	Net 16	11.0788	0.269966	7.57057	1.25417	97,4414	
BGA1-D3	Net 17	8.22157	0.192791	5.08606	1.10179	74.8585	
BGA1-B2	Net 18	10.1306	0.244018	7.37262	1.14468	91.8658	
BGA1-J5	Net_19	4.9028	0.103388	3.26669	0.754613	49.6497	
BGA1-J3	Net_2	7.13797	0.163051	4.63538	0.986172	67.6113	
BGA1-L3	Net_20	9.87792	0.235877	5.20066	1.16056	84.8308	
BGA1-H5	Net_21	5.68593	0.127314	3.31686	0.845386	52.9531	
BGA1-K2	Net_22	10.7874	0.262896	7.27888	1.23451	94.7936	
BGA1-H3	Net_23	7.79617	0.182037	6.16109	0.964408	77.0831	
BGA1-E4	Net_24	6.00798	0.132958	3.7231	0.870797	56.9391	
BGA1-B1	Net_25	12.4208	0.308913	8.46425	1.42993	110.015	
BGA1-A2	Net_26	12.2451	0.306041	8.7622	1.36485	109.358	
BGA1-C4	Net_27	7.1569	0.163887	4.68482	0.937359	66.2673	
BGA1-K5	Net_28	6.69234	0.15299	4.86343	0.897985	66.0855	
		0.41000	0.000040	C 10010	1 1227	300.00	

NOTE!

Net-length is reported only for single nets. If a single net has multi-pins in either die side or BGA side, its' net -length will NOT be reported.

#### **View DC Resistance**

- 1. Click **DC Resistance** in the SPICE / IBIS Model window.
- 2. View the .csv file. DC Resistance is given for each of the power, ground and signal nets. A .csv file is saved on the hard disk.

💼 🔛 🖉 - (° -	🗌 🔠 🖸 🕴 Extractor Result 🛛 🖌 📳 🖺	
Extractor Result		
View Model Selection SPICE T-model SPICE Pi-model IBIS .pkg model Pin model: IBIS format Pin model: Excel format O C Resistance	-~~~-~~~ 	
NatNama	P/Ohma)	
Net Name         DL           VDD_1         0.00           VDD_2         0.00           VDD_3         0.00           VDD_4         0.00           VDD_core         0.00           Net_10         0.22           Net_11         0.22           Net_11         0.22           Net_11         0.22           Net_11         0.22           Net_13         0.00           Net_14         0.22           Net_15         0.09           Net_16         0.22           Net_17         0.11           Net_18         0.22           Net_19         0.00           Net_20         0.13           Net_21         0.14           Net_22         0.22           Net_23         0.14           Net_24         0.11           Net_25         0.22           Net_26         0.22           Net_27         0.13           Net_28         0.13           Net_29         0.14	Note       Note         1766212       173         17728748       1734888         1731403       1389387         1389387       6745         132246       128         132246       128         132247       128         132248       129         132247       129         132723       127         14774       129         14214       128         1222723       127         1362       126         14214       128         1531       10191         1222371       13362         16608       13159         17516       148         18752       17665         17566       1026         134056       123376         13598       123376	

#### **View RLC Per Net**

- 1. View **Resistance** for each net.
- 2. View Self-inductance for each net.
- 3. View Self-capacitance for each net.
- 4. View Mutual Terms.
- 5. View Mutual Inductance.
- 6. View SPICE Mutual Capacitance.

Usually conductance is very low, so there is no view for conductance.



#### Save R / L / C Full Matrix

- 1. Click on R/L/C full matrix.
- 2. The matrix is saved on hard disk in .csv format.

<b>Z</b> /	Nicroso	ft Exce	l - pkg_	flipchip	o_6_Tal	bleCont	🔳		
Ð	<u>F</u> ile <u>E</u> dit	t <u>V</u> iew j	<u>I</u> nsert F <u>o</u> r	mat <u>T</u> ool	s <u>D</u> ata	<u>W</u> indow	<u>H</u> elp	_ 8 ×	
1	📂 🛃 🔒	) (3) (4)	. 👗 🛍 -	10 - (1	-   Σ - <u>A</u> Z	↓ X↓   🛍	ad 🕐 🚆	i 💩 - 🚆	
: 🖢	🔄 🔄 🖄 🕢 🖏 🖄 👘 🕅 🖓 🦓 🛍 🕅 🕅 Reply with Changes End Review								
	A1	•	<i>f</i> ∡ Net i	-					
	Α	В	С	D	E	F	G	F	
1	Net i	Net j	Rij (mOhm	Lij (nH)	Cij (pF)				
2	VDD_1	VDD_1	16.6984	1.14717	17.8014				
3	VDD_1	Net_5		0.882293	0.398692				
4	VDD_1	Net_14		0.845834	0.51895				
5	VDD_1	Net_32		0.830443	0.397358				
6	VDD_1	Net_6		0.706866	0.410717				
7	VDD_1	Net_41		0.660616	0.204631				
8	VDD_1	Net_16		0.501037	0.509205				
9	VDD_1	Net_31		0.447115	0.060698				
10	VDD_1	Net_4		0.41579	0.32842				
11	VDD_1	Net_23		0.28861	0.126366				
12	VDD_1	Net_15		0.280537	0.0241				
13	VDD_2	VDD_2	15.9463	1.02801	18.649				
14	VDD_2	Net_35		0.754558	0.606863				
15	VDD_2	Net_50		0.728148	0.398461				
16	VDD_2	Net_55		0.721226	0.494188				
17	VDD_2	Net_54		0.702859	0.4037				
18	VDD_2	Net_45		0.698387	0.457406				
19	VDD_2	Net_62		0.692691	0.533048				
20	VDD_2	Net_49		0.566389	0.1798				
21	VDD_2	Net_65		0.563293	0.178132				
22	VDD_2	Net_43		0.459691	0.290527				
23	VDD_2	Net_63		0.402483	0.374004				
24	VDD_2	Net_72		0.274983	0.329165				
25	VDD_3	VDD_3	15.9821	1.07951	18.4838			~	
N.	· · · ·	kg_flipchi	p_6_Table	Content/	<b>(</b> )			>	
Dr	aw + 🗟   A	A <u>u</u> toShapes	- / * [		4 3 8	🗟   🆄 -	<u>⊿</u> • <u>A</u>	• = 🔋	
Read	dy					1	NUM		

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#### **View RLC Distributions**

- 1. Click **RLC Distributions** in the Workflow pane.
- 2. View the full matrix value of R, L and C.

RLC Distributions offers eight kinds of views.



**3.** View the **RLC distributions**.



#### **View Segment RLC**

1. Click Segment RLC in the Workflow pane.

For each Signal Net, XtractIM outputs the RLC segment of each Metal layer.

Extractor Result           PinName         SignalNetNa         Signal\$VI(0         Signal\$VDD(         Signal\$VSS(         Signal\$M4(0           L2         Net_1         0.180109         0.0111254         0.00946193         0.0119557           J3         Net_2         0.11236         0.010766         0.00949058         0.0119557           J1         Net_3         0.255368         0.010766         0.00949058         0.0119557           G2         Net_4         0.148074         0.0107667         0.00949058         0.0119557           G2         Net_5         0.13487         0.0107667         0.00949058         0.0119557           E3         Net_7         0.100455         0.0107647         0.00949058         0.0119574           D2         Net_8         0.15182         0.0107647         0.00948935         0.0119541           C2         Net_9         0.16308         0.0107647         0.00948935         0.0119541           M2         Net_10         0.20419         0.0107647         0.00948935         0.0119541           L1         Net_11         0.26482         0.0107647         0.00948935         0.0119541           H4         Net_12         0.073506         0.
PinName         Signal%H1(Q         Signal%VDD(         Signal%VSS(         Signal%M4(Q           L2         Net_1         0.180109         0.0111254         0.00946193         0.0119557           J3         Net_2         0.11236         0.010766         0.00949058         0.0119557           J1         Net_3         0.255368         0.010766         0.00949058         0.0119557           H2         Net_4         0.148074         0.010766         0.00949058         0.0119557           G2         Net_5         0.133487         0.0107667         0.00949935         0.0119557           E3         Net_7         0.100455         0.0107667         0.00949935         0.0119574           D2         Net_8         0.151882         0.0107647         0.00948935         0.0119541           C2         Net_9         0.163308         0.0107647         0.00948935         0.0119541           M2         Net_10         0.220419         0.0107673         0.00948935         0.0119541           L1         Net_12         0.073506         0.010766         0.0949058         0.0119574           H4         Net_12         0.073506         0.010766         0.0949058         0.0119557 <tr< th=""></tr<>
PinName         SignalNetNa         SignalsM1(0         SignalsVDD(         SignalsVSS(         SignalsM4(0           L2         Net_1         0.180109         0.0111254         0.00946193         0.0119557           J3         Net_2         0.11236         0.010766         0.00949058         0.0119557           J1         Net_3         0.255368         0.010766         0.00949058         0.0119557           H2         Net_4         0.148074         0.010766         0.00949058         0.0119557           G2         Net_5         0.133487         0.010766         0.00949058         0.0119557           E3         Net_7         0.100455         0.0106971         0.00949058         0.0119574           D2         Net_8         0.151882         0.0107647         0.00948035         0.0119541           C2         Net_9         0.163308         0.0107647         0.00948035         0.0119541           M2         Net_10         0.20419         0.0107647         0.00948035         0.0119541           L1         Net_11         0.236482         0.0107663         0.00949058         0.0119541           L1         Net_12         0.073506         0.0107666         0.00949058 <t< th=""></t<>
L2       Net_1       0.180109       0.0111254       0.00946193       0.0119557         J3       Net_2       0.11236       0.010766       0.00949058       0.0119557         J1       Net_3       0.255368       0.010766       0.00949058       0.0119557         H2       Net_4       0.148074       0.010766       0.00949058       0.0119557         G2       Net_5       0.133487       0.010766       0.00949058       0.0119557         E2       Net_6       0.144806       0.010766       0.00949058       0.0119574         E2       Net_7       0.100455       0.0106971       0.00948935       0.0119574         D2       Net_8       0.151882       0.0107647       0.00948935       0.0119541         C2       Net_9       0.163308       0.0107647       0.00948935       0.0119541         M2       Net_10       0.220419       0.0107673       0.0094918       0.0119574         H4       Net_12       0.073506       0.010766       0.00949058       0.0119574         H4       Net_12       0.073506       0.00759813       0.0124565         F1       Net_14       0.18993       0.010766       0.00949058       0.0119557
J3       Net_2       0.11236       0.010766       0.00949058       0.0119557         J1       Net_3       0.255368       0.010766       0.00949058       0.0119557         H2       Net_4       0.148074       0.010766       0.00949058       0.0119557         G2       Net_5       0.133487       0.0107667       0.00948935       0.0119541         E2       Net_6       0.144806       0.010766       0.00949058       0.0119577         E3       Net_7       0.100455       0.0106971       0.00948935       0.0119574         D2       Net_8       0.151882       0.0107647       0.00948935       0.0119541         C2       Net_9       0.163308       0.0107647       0.00948935       0.0119541         M2       Net_10       0.220419       0.0107647       0.00948935       0.0119541         L1       Net_11       0.236482       0.0107673       0.00949058       0.0119574         H4       Net_12       0.073506       0.0107666       0.00949058       0.0119557         G5       Net_13       0.00569206       0.003949058       0.0119557         F5       Net_16       0.2101       0.010766       0.00949058       0.0119557      <
J1         Net_3         0.255368         0.010766         0.00949058         0.0119557           H2         Net_4         0.148074         0.010766         0.00949058         0.0119557           G2         Net_5         0.133487         0.0107647         0.00948935         0.0119541           E2         Net_6         0.144806         0.010766         0.00949058         0.0119557           E3         Net_7         0.100455         0.0106971         0.0094918         0.0119574           D2         Net_8         0.151882         0.0107647         0.00948935         0.0119541           C2         Net_9         0.163308         0.0107647         0.00948935         0.0119541           M2         Net_10         0.220419         0.0107647         0.00948935         0.0119541           L1         Net_11         0.236482         0.0107673         0.0094918         0.0119574           H4         Net_12         0.073506         0.010766         0.00949058         0.0119557           G5         Net_13         0.00569206         0.00895375         0.00759813         0.0124565           F1         Net_14         0.18993         0.010766         0.00949058         0.0119557
H2       Net_4       0.148074       0.010766       0.00949058       0.0119557         G2       Net_5       0.133487       0.0107647       0.00948935       0.0119541         E2       Net_6       0.144806       0.010766       0.00949058       0.0119557         E3       Net_7       0.100455       0.0106971       0.0094918       0.0119574         D2       Net_8       0.151882       0.0107647       0.00948935       0.0119541         C2       Net_9       0.163308       0.0107647       0.00948935       0.0119541         M2       Net_10       0.220419       0.0107647       0.00948935       0.0119541         L1       Net_11       0.236482       0.0107673       0.0094918       0.0119574         H4       Net_12       0.073506       0.010766       0.00949058       0.0119557         G5       Net_13       0.00569206       0.00895375       0.00759813       0.0124565         F1       Net_14       0.18993       0.010766       0.00949058       0.0119557         G5       Net_15       0.0247396       0.0134646       0.00851012       0.0119557         J3       Net_17       0.140426       0.010766       0.00949058       0.
G2         Net_5         0.133487         0.0107647         0.00948935         0.0119541           E2         Net_6         0.144806         0.010766         0.00949058         0.0119557           E3         Net_7         0.100455         0.0106971         0.0094918         0.0119574           D2         Net_8         0.151882         0.0107647         0.00948935         0.0119541           C2         Net_9         0.163308         0.0107647         0.00948935         0.0119541           M2         Net_10         0.220419         0.0107647         0.00948935         0.0119541           L1         Net_11         0.236482         0.0107673         0.0094918         0.0119574           H4         Net_12         0.073506         0.010766         0.00949058         0.0119557           G5         Net_13         0.00569206         0.00895375         0.00759813         0.0124565           F1         Net_14         0.18993         0.010766         0.00949058         0.0119557           G5         Net_15         0.0247396         0.0134646         0.00851012         0.0119557           D3         Net_17         0.140426         0.010766         0.00949058         0.0119557
E2         Net_6         0.144806         0.010766         0.00949058         0.0119557           E3         Net_7         0.100455         0.0106971         0.0094918         0.0119574           D2         Net_8         0.151882         0.0107647         0.00948935         0.0119541           C2         Net_9         0.163308         0.0107647         0.00948935         0.0119541           M2         Net_10         0.220419         0.0107647         0.00948935         0.0119541           L1         Net_11         0.236482         0.0107673         0.0094918         0.0119574           H4         Net_12         0.073506         0.010766         0.00949058         0.0119557           G5         Net_13         0.00569206         0.00895375         0.00759813         0.0124565           F1         Net_14         0.18993         0.010766         0.00949058         0.0119557           F5         Net_15         0.0247396         0.0134646         0.00851012         0.0119557           D3         Net_17         0.140426         0.010766         0.00949058         0.0119557           B2         Net_18         0.176829         0.0178275         0.00949183         0.0119557
E3         Net_7         0.100455         0.0106971         0.0094918         0.0119574           D2         Net_8         0.151882         0.0107647         0.00948935         0.0119541           C2         Net_9         0.163308         0.0107647         0.00946071         0.0119541           M2         Net_10         0.220419         0.0107647         0.00948935         0.0119541           L1         Net_11         0.236482         0.0107673         0.0094918         0.0119574           H4         Net_12         0.073506         0.010766         0.00949058         0.0119557           G5         Net_13         0.00569206         0.00895375         0.00759813         0.0124565           F1         Net_14         0.18993         0.010766         0.00949058         0.0119557           F5         Net_15         0.0247396         0.0134646         0.00851012         0.0119557           D1         Net_16         0.2101         0.010766         0.00949058         0.0119557           D3         Net_17         0.140426         0.010766         0.00949058         0.0119557           B2         Net_18         0.176829         0.0178275         0.00946193         0.0119557
D2         Net_8         0.151882         0.0107647         0.00948935         0.0119541           C2         Net_9         0.163308         0.0107647         0.00946071         0.0119541           M2         Net_10         0.220419         0.0107647         0.00948935         0.0119541           L1         Net_11         0.236482         0.0107673         0.0094918         0.0119574           H4         Net_12         0.073506         0.010766         0.00949058         0.0119557           G5         Net_13         0.00569206         0.00895375         0.00759813         0.0124565           F1         Net_14         0.18993         0.010766         0.00949058         0.0119557           F5         Net_15         0.0247396         0.0134646         0.00851012         0.0119541           D1         Net_16         0.2101         0.010766         0.00949058         0.0119557           D3         Net_17         0.140426         0.010766         0.00949058         0.0119557           B2         Net_18         0.176829         0.0178275         0.00946193         0.0119557           J5         Net_19         0.0565564         0.0107647         0.00948355         0.0119541
C2         Net_9         0.163308         0.0107647         0.00946071         0.0119541           M2         Net_10         0.220419         0.0107647         0.00948935         0.0119541           L1         Net_11         0.236482         0.0107673         0.0094918         0.0119574           H4         Net_12         0.073506         0.010766         0.00949058         0.0119557           G5         Net_13         0.00569206         0.00895375         0.00759813         0.0124565           F1         Net_14         0.18993         0.010766         0.00949058         0.0119557           F5         Net_15         0.0247396         0.0134646         0.00851012         0.0119541           D1         Net_16         0.2101         0.010766         0.00949058         0.0119557           D3         Net_17         0.140426         0.010766         0.00949058         0.0119557           B2         Net_18         0.176829         0.0178275         0.00949133         0.0119557           J5         Net_19         0.0565564         0.0107647         0.0094835         0.0119557           J5         Net_20         0.180453         0.0107673         0.00946315         0.0119574
M2         Net_10         0.220419         0.0107647         0.00948935         0.0119541           L1         Net_11         0.236482         0.0107673         0.0094918         0.0119574           H4         Net_12         0.073506         0.010766         0.00949058         0.0119557           G5         Net_13         0.00569206         0.00895375         0.00759813         0.0124565           F1         Net_14         0.18993         0.010766         0.00949058         0.0119557           F5         Net_15         0.0247396         0.0134646         0.00851012         0.0119541           D1         Net_16         0.2101         0.010766         0.00949058         0.0119557           D3         Net_17         0.140426         0.010766         0.00949058         0.0119557           B2         Net_18         0.176829         0.0178275         0.00946193         0.0119557           J5         Net_19         0.0565564         0.0107647         0.00948935         0.0119541           L3         Net_20         0.180453         0.0107673         0.00946315         0.0119574
L1         Net_11         0.236482         0.0107673         0.0094918         0.0119574           H4         Net_12         0.073506         0.010766         0.00949058         0.0119557           G5         Net_13         0.00569206         0.00895375         0.00759813         0.0124565           F1         Net_14         0.18993         0.010766         0.00949058         0.0119557           F5         Net_15         0.0247396         0.0134646         0.00851012         0.0119541           D1         Net_16         0.2101         0.010766         0.00949058         0.0119557           D3         Net_17         0.140426         0.010766         0.00949058         0.0119557           B2         Net_18         0.176829         0.0178275         0.00946193         0.0119557           J5         Net_19         0.0565564         0.0107647         0.00948935         0.0119557           L3         Net_20         0.180453         0.0107673         0.00946315         0.0119574
H4         Net_12         0.073506         0.010766         0.00949058         0.0119557           G5         Net_13         0.00569206         0.00895375         0.00759813         0.0124565           F1         Net_14         0.18993         0.010766         0.00949058         0.0119557           F5         Net_15         0.0247396         0.0134646         0.00851012         0.0119541           D1         Net_16         0.2101         0.010766         0.00949058         0.0119557           D3         Net_17         0.140426         0.010766         0.00949058         0.0119557           B2         Net_18         0.178275         0.00949058         0.0119557           J5         Net_19         0.0565564         0.0107647         0.00948935         0.0119557           L3         Net_20         0.180453         0.0107673         0.00946315         0.0119574
G5         Net_13         0.00569206         0.00895375         0.00759813         0.0124565           F1         Net_14         0.18993         0.010766         0.00949058         0.0119557           F5         Net_15         0.0247396         0.0134646         0.00851012         0.0119541           D1         Net_16         0.2101         0.010766         0.00949058         0.0119557           D3         Net_17         0.140426         0.010766         0.00949058         0.0119557           B2         Net_18         0.176829         0.0178275         0.00946193         0.0119557           J5         Net_19         0.0565564         0.0107647         0.00948935         0.0119541           L3         Net_20         0.180453         0.0107673         0.00946115         0.0119574
F1         Net_14         0.18993         0.010766         0.00949058         0.0119557           F5         Net_15         0.0247396         0.0134646         0.00851012         0.0119541           D1         Net_16         0.2101         0.010766         0.00949058         0.0119557           D3         Net_17         0.140426         0.010766         0.00949058         0.0119557           B2         Net_18         0.176829         0.0178275         0.00946193         0.0119557           J5         Net_19         0.0565564         0.0107647         0.00948935         0.0119541           L3         Net_20         0.180453         0.0107673         0.00946115         0.0119574
F5         Net_15         0.0247396         0.0134646         0.00851012         0.0119541           D1         Net_16         0.2101         0.010766         0.00949058         0.0119557           D3         Net_17         0.140426         0.010766         0.00949058         0.0119557           B2         Net_18         0.176829         0.0178275         0.00946193         0.0119557           J5         Net_19         0.0565564         0.0107647         0.00948935         0.0119541           L3         Net_20         0.180453         0.0107673         0.00946115         0.0119574
D1         Net_16         0.2101         0.010766         0.00949058         0.0119557           D3         Net_17         0.140426         0.010766         0.00949058         0.0119557           B2         Net_18         0.176829         0.0178275         0.00946193         0.0119557           J5         Net_19         0.0565564         0.0107647         0.00948935         0.0119541           L3         Net_20         0.180453         0.0107673         0.00946115         0.0119574
D3         Net_17         0.140426         0.010766         0.00949058         0.0119557           B2         Net_18         0.176829         0.0178275         0.00946193         0.0119557           J5         Net_19         0.0565564         0.0107647         0.00948935         0.0119541           L3         Net_20         0.180453         0.0107673         0.00946315         0.0119574
B2         Net_18         0.176829         0.0178275         0.00946193         0.0119557           J5         Net_19         0.0565564         0.0107647         0.00948935         0.0119541           L3         Net_20         0.180453         0.0107673         0.00946315         0.0119574
J5         Net_19         0.0565564         0.0107647         0.00948935         0.0119541           L3         Net_20         0.180453         0.0107673         0.00946315         0.0119574
L3 Net_20 0.180453 0.0107673 0.00946315 0.0119574
H5 Net_21 0.0728056 0.00613949 0.0050913 0.0269901
K2 Net_22 0.204092 0.0107647 0.00946071 0.0119541
H3 Net_23 0.128777 0.0107673 0.00946315 0.0119574
E4 Net_24 0.0855075 0.0106953 0.00949058 0.0119557
B1 Net_25 0.244964 0.0107673 0.0094918 0.0119574
A2 Net_26 0.240459 0.0107647 0.00948935 0.0119541
C4 Net_27 0.113034 0.0107647 0.00948935 0.0119541
K5 Net 28 0.1011 0.0107647 0.00948935 0.0119541

Resistance(Ohm) Inductance(nH) Capcitance(pF)

#### 2. View the Segment RLC values.

Note the three tabs across the bottom of the screen. These bars are for Resistance, Inductance and Capacitance

- Click on the **Resistance** tab. The Resistance values are displayed.
- Click on the Inductance tab. The Inductance values are displayed.
- Click on the Capacitance tab. The Capacitance values are displayed.

# **Segment RLC Report**

Segment RLC are reported for Signal Nets with single-pin at each of the Die- and Board circuit. Via resistance and inductance are reported at the Via starting layer (the upper layer).

Components	Segment R	Segment L	Segment C
Wirebond	Yes	Yes	Yes
Trace	Yes	Yes	Yes
Via	Yes	Yes	Yes
Pad	-	-	Yes
Leadframe	Yes	Yes	Yes

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# **View RLC vs. Net Length**

1. Click RLC vs. Net Length in the Workflow pane.

The Inductance plot is displayed in the result window.



- To view the Inductance plot, select L vs. Net Length from the drop-down list
- To view the Capacitance plot, select C vs. Net Length from the drop-down list
- To view the Delay plot, select, select Delay vs. Net Length from the drop-down list

#### **View Signal Nets Crosstalk**

# **NEXT and FEXT**

The mathematical definitions for NEXT and FEXT are shown in the following examples.



 $Z_{10} = \sqrt{\frac{L_{11}}{C_{11}}} \quad Z_{20} = \sqrt{\frac{L_{22}}{C_{22}}}$ 

Definitions

К	The near-end coupling coefficient from aggressor net on victim net.
C <sub>11</sub> / C <sub>22</sub>	The self capacitance per unit length of signal net to its reference plane.
L <sub>11</sub> / L <sub>22</sub>	The self-inductance per unit length of signal net.
C <sub>12</sub>	The mutual capacitance per unit length between aggressor and victim net.
L <sub>12</sub>	The mutual inductance per unit length between aggressor and victim net.
V <sub>p1</sub> / V <sub>p2</sub>	The signal velocity propagate on signal net.
Z <sub>10</sub> / Z <sub>20</sub>	The characteristic impedance of signal Traces.

$$FEXT = \frac{\sqrt{L_{ii}C_{ii}}}{2T_r} \left(\frac{C_{ij}}{C_{ii}} - \frac{L_{ij}}{L_{ii}}\right)$$

RLC of differential Pair and crosstalk with others

Assume two nets are different pair which has L1/ L2 and L12 as self-inductance and mutual induc-

tance, and C11/C22 and C12 as loading capacitance and mutual capacitance



- Single-Ended
- Diffpair vs Single-Ended

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View/Export Results
Summary
SPICE/IBIS Model
RLC Per Net
RLC Distributions
Segment RLC
RLC vs. Net Length
CrossTalk (Single-Ended)
3D View
Histogram
CrossTalk (Diffpair vs Single-Ended)
3D View
Histogram
Save Results
Load Results
Report

- To view single-ended near-end and far-end crosstalk (NEXT and FEXT) click **CrossTalk** (Single-Ended) in the Workflow pane
- To view difffpair near-end and far-end crosstalk (NEXT and FEXT) click **CrossTalk (Diffpair vs Single-Ended)** in the **Workflow** pane

A file is created in the project folder. The file name is:

\*signal\_Xtalk.csv

By default, the far-end crosstalk is defined with rise time = 100ps.

								cadence
9 - (*	- II II C	Extractor	Result 🔽	d 10 10 10 10				
Net i	Net j	Rij (mOhm)	Lij (nH)	Cij (pF)	NEXT (%)	Total NEXT (	FEXT (%)	Tr (pS)
Net_1	Net_1	220.586	6.5703	1.011		26.91		
Net_1	Net_11	0	1.0701	0.072	5.33		-3.94	100
Net_1	Net_10	0	0.9105	0.000	3.14		-5.57	100
Net_1	Net_2	0	0.6407	0.010	3.43		-4.14	100
Net_1	Net_20	0	0.6277	0.000	2.48		-4.05	100
Net_1	Net_22	0	0.5013	0.000	1.85		-3.13	100
Net_1	Net_29	0	0.4415	0.000	1.80		-2.87	100
Net_1	Net_40	0	0.4049	0.000	1.58		-2.48	100
Net_1	Net_30	0	0.3650	0.000	1.73		-2.60	100
Net_1	Net_3	0	0.3007	0.000	1.05		-1.93	100
Net_1	Net_12	0	0.2742	0.000	1.56		-2.03	100
Net_1	Net_19	0	0.2512	0.000	1.45		-1.82	100
Net_1	Net_21	0	0.2459	0.000	1.52		-2.01	100
Net_2	Net_2	143.402	4.3835	0.864		29.23		
Net_2	Net_11	0	0.9447	0.119	6.30		-1.31	100
Net_2	Net_1	0	0.6407	0.010	3.03		-3.57	100
Net_2	Net_40	0	0.5993	0.002	2.74		-3.59	100
Net_2	Net_22	0	0.4411	0.000	1.84		-2.76	100
Net_2	Net_12	0	0.4346	0.007	3.14		-3.00	100
Net_2	Net_3	0	0.3957	0.000	1.55		-2.54	100
Net_2	Net_20	0	0.3120	0.000	1.40		-2.01	100
Net_2	Net_30	0	0.3112	0.000	1.70		-2.22	100
Net_2	Net_10	0	0.3019	0.000	1.17		-1.85	100
Net_2	Net_29	0	0.2934	0.000	1.37		-1.91	100
Net_2	Net_23	0	0.2850	0.000	1.32		-1.72	100
Net_2	Net_21	0	0.2638	0.000	1.92		-2.15	100
Net_2	Net_19	0	0.2553	0.000	1.76		-1.85	100
Net_3	Net_3	296.611	8.0109	1.325		12.47		
Net_3	Net_40	0	0.8060	0.000	2.77		-4.94	100
Net_3	Net_2	0	0.3957	0.000	1.69		-2.78	100
Net_3	Net 22	0	0.3864	0.000	1.26		-2.41	100

#### **Change Rise Time**

- **1.** Use the SHIFT key and mouse to select multiple rows.
- 2. Use the CTRL key and mouse click to select the top cell, Tr (ps).
- **3.** In the highlighted cell change the Rise Time to the desired value.
- 4. Click Enter. The values are changed.

Tr (pS)	Tr (pS)	Tr (pS)	Tr (pS)
100	100	100	100
100	100	200	200
100	100	100	200
100	100	100	200
100	100	100	200
100	100	100	200
100	100	100	200
100	100	100	200
100	100	100	200
100	100	100	200
100	100	100	200
100	100	100	200
100	100	100	200
100	100	100	200
100	100	100	200
100	100	100	200
100	100	100	200
100	100	100	200
100	100	100	100
100	100	100	100
100	100	100	100
100	100	100	100
100	100	100	100
100	100	100	100

Upon exiting the window, a pop-up window appears. You are asked if you want to save your changes.



# **Save Simulation Results**

1. Click Save Results in the Workflow pane.

The Save Extractor Result As window appears.

Save Extractor Result As				×
Update:	1 ► SpeedXP ► Samples ► XtractIM ► Single-D	ie_Sample_files	👻 🍫 Search Singl	le-Die_Sam 🔎
Organize 🔹 New fold	der			• •
Downloads	Name Ibis_tlipchip_tlipchip_pin.ibs	Date modified 6/5/2013 2:46 PM	Type IBS File	Size 10 KB
	Options.xml	6/5/2013 2:46 PM	XML Document	9 KB
Libraries	ResourceProfile_XtractIM.log	6/5/2013 2:46 PM	wrifile	12 KB
Jocuments Music	Result_FlipChip_flipchip_060513_144602	6/5/2013 2:46 PM	XIM File	535 KB
le Pictures	wirebond.spd	1/22/2013 9:19 PM	SPEED2000 Docu	849 KB
JUIDE Videos	+ Wirebond.ximx	1/22/2013 9:18 PM	Sigrity XtractIM W	26 KB ≡
secomputer	Xtracted_PinNode_Info.log XtractIMRunTimeError.log	6/5/2013 2:46 PM 6/5/2013 2:46 PM	wrifile wrifile	1 KB 1 KB <del>-</del>
ncal Disk (C)	•	III		•
File <u>n</u> ame: Rest	ult			•
Save as type: All F	ile (*.*)			•
Hide Folders			Save	Cancel

- **2.** Input a file name.
- 3. Click Save.

The results are saved in a binary file. The file is named:

result\_spd\_file\_name.xim

4. (Optional) Click Cancel if you do not want to save the results in the file name you input in earlier steps.

#### **Simulation Output Files**

The result and result\*.xim files save all the output data including Summary, SPICE circuit and the two package model files. The SPICE file and two IBIS files are automatically saved by the tool.

The result file is created automatically when the simulation is finished. The output files can be viewed on the on hard disk.

- One Crosstalk file in Excel Format Signal\_Xtalk.csv for signal net crosstalk
- One IBIS Package Model File \*.pkg file. Both L and C include coupling elements •
- **One Pin Model in Excel Format** \*.csv file includes each signal net length, self-R, self-L, • self-C, and time delay. No coupling elements are included
- One Pin Model in IBIS Format \*.ibs file including each signal net self-R, self-L, and self-• C. No coupling element is included
- **One Summary Content in Excel Format** \*.csv file includes RLC Full Matrix ٠
- Three Segment RLC in Excel Format Segment RLC of each metal layer with \*.csv files ٠
- Two SPICE Circuit Files Pi-model is named \*.ckt and the T-model is named \*\_t.ckt •

Notel	In model (*.ckt, *.pkg, and *PinModel.csv) extraction, XtractIM uses all ground nets as reference for both power and signal nets.
NOTE	The *.ibs model is for signal nets only. In *.ibs model extraction, by IBIS definition, XtractIM uses all ground and power nets as ideal reference to get R, L, and C for each signal net.

**Output Result Displays with Images (PNG or BMP Format)** 

1. Select

Workspace > Export to Image File

The Save As window opens.

Save As				×
🕞 🕞 – 📜 « Up	date1   SpeedXP   Samples   XtractIM   Single-Die_Sample_files	👻 🍫 Sear	ch Single-Die_San	n 🔎
Organize 🔻 Nev	v folder		•	0
	Name	Date modified	Туре	
闫 Libraries				
Documents	No items match your sear	rch.		
📣 Music				
Sector Pictures				
JUI Videos	=			
ike Computer				
🥾 Local Disk (C:)				
Local Disk (D:)				
	▼ <b>∢</b> III			•
File <u>n</u> ame:				-
Save as type:	PNG Files(*.png)			-
	PNG Files(*.png)			
A Hido Foldors	BMP Files (*.bmp)			
- Hide Polders	All files ("")			

- 2. In the new window select the file type (.png or .bmp).
- 3. Click Save. The image file is saved.

# **Load in Saved Results**

1. To load the saved results, click Load Results in the Workflow pane.

The Load Extractor Result(s) From window opens.

🕞 🕞 🗸 « Update	e1 ► Sp	peedXP + Samples + XtractIM + Single-Die_Sample_files	✓ Search	Single-Die_Sam 🔎					
Organize ▼ New fol	lder			≣ <b>-</b> □ 0					
☆ Favorites	^ N	ame	Date modified	Туре					
💻 Desktop		CPU_Info.log	6/5/2013 2:46 PM	wrifile					
🐌 Downloads		flipchip.spd	10/22/2012 1:52 PM	SPEED2000 Docu. ≡					
Skecent Places	= 4	FlipChip.ximx	10/22/2012 1:52 PM	Sigrity XtractIM W					
	6	FlipChip_flipchip_DCResistance.csv	6/5/2013 2:46 PM	Microsoft Office E					
🥞 Libraries	6	FlipChip_flipchip_PinModel.csv	6/5/2013 2:46 PM	Microsoft Office E					
Documents	6	FlipChip_flipchip_SegmentC.csv	6/5/2013 2:46 PM	Microsoft Office E					
Interest description		FlipChip_flipchip_SegmentL.csv	6/5/2013 2:46 PM	Microsoft Office E					
Sectores	1	a FlipChip_flipchip_SegmentR.csv	6/5/2013 2:46 PM	Microsoft Office E					
JUDE Videos	C.	FlipChip_flipchip_signal_Xtalk.csv	6/5/2013 2:46 PM	Microsoft Office E					
	6	FlipChip_flipchip_signal_Xtalk_diffpair.csv	6/5/2013 2:46 PM	Microsoft Office E					
Scomputer .		-x		4					
File <u>n</u>	iame:		▼ All File (*.*)	Cancel					
				t.					

- 2. Browse to select the desired result file.
- 3. Click Open.

The result file is loaded.

- 4. View present results or the loaded results.
  - Loaded Curves Shows the loaded results
  - Present Curves Present extracted results
- **5.** To unload a loaded result:

Unload Extractor Result

#### **Resistance Results**



# Simulation Report with .htm / .html Format

1. Click **Report** in the **Workflow** pane.

The **Options** window appears.

Options	×
File 💿	
General File Manager Save Options Hotkeys	General Information
Grid and Unit View Processing Trace Error Checking 3D Layout View Display	Report template     rary\template\XtractIM\XtractIM_Report_Template_EPA_Default.htm       Notes:     I like XtractIM report
Quality Simulation (Basic) ( General Net and Coupling Special Void Output SPICE Circuit Report Simulation (Advanced) ( Electric Models Mesh Nets and Shapes	Optional Plots
	Default Apply OK Cancel

**2.** Browse to select the Report Template from

<INSTALL\_DIR>\SpeedXP\Library\template\XtractIM\

- **3.** Input notes, if desired.
- 4. Click OK.

The report file is created.

	cādence
XtractIM Simul	ation Report
Date: December 18, 2012	
1 General information	
XtractlM version: 12.0.7.11271	
File names and locations:	
<ul> <li>XtractIM workspace file: FlipChip.ximx</li> <li>XtractIM layout file: flipchip.spd</li> <li>File location: C:/SigritySamples/SpeedPKG 12.0/Xtra</li> </ul>	actIM/Samples/Single-Die_Sample_files/
2 Simulation Setup	
2.1 Package and Components	
Package type Die Board	

# **LESSON FIVE: BATCH MODE SIMULATION**

**1.** To run a simulation in Batch Mode, select:

Start > Run

- 2. Change to the directory where the XtractIM.exe file is located.
- **3.** Upon completing the simulation, all output files are automatically saved in the same directory as the \*.spd file.
  - \*.ckt files
  - \*.ibs files
  - \*.pkg files
  - .csv files

#### **Batch Mode Example**

If you want to use the project (.spd file) defaulted in the workspace file (.xml file), enter

XtractIM -b "Full\_path\_toMy\_xml\_File xml filename"

If you want to use a different project file other than the one in the .xml file, enter

XtractIM -b "Full\_path\_toMy\_xml\_File\xml filename" "Full\_path\_toMy\_xml\_File *new\_spd-file-name*"

# **LESSON SIX: PARTIAL INDUCTANCE REPORT FOR POWER/GROUND NETS**

#### Introduction

Net-based partial inductance of power and ground nets is an optional output result for single-die single-BGA packages. It is used to evaluate the relative power and ground network design quality, while loop inductance of power and ground net pair provides meaningful electrical performance.

In the **SPICE/IBIS Model** section of **View/Export Results**, three partial inductance reports are available.

- Partial RLC for Power and ground nets reported with .csv format
- T-topology SPICE model with Power-ground nets having partial inductance
- Pi-topology SPICE model with Power-ground nets having partial inductance
- 1. Choose Tools > Options > Edit Options....



- 2. Click Output SPICE Circuit in the Options window.
- 3. Check Power-Ground net has partial inductance (single-Die Single-BGA Net-based only).

ile 🔿	
General File Manager Save Options Hotkeys	Change the 'Output SPICE Circuit' options in XtractIM
ayout 📀	
Grid and Unit View Processing Trace Error Checking BD Layout View (*) Display Quality Simulation (Basic) (*) General Net and Coupling Special Void Output SPICE Circuit Report Simulation (Advanced) (*)	<ul> <li>Power-Ground net has partial inductance (Single-Die Single-BGA Net-based only)</li> <li>Net Name Included in Circuit Node Name</li> <li>Keep All Coupling Terms to Power Nets</li> <li>Export RLC Matrices</li> <li>Output IBIS .pkg file for Multi-die Stacked-BGA Package</li> <li>(Each .pkg model represents one-die to one-board path assuming other dies and board to be open/floating )</li> <li>Do not Output T- and Pi-topology SPICE Model</li> <li>Include Decaps in SPICE circuit</li> <li>(If a circuit is selected as decap during workspace-&gt;circuit setup,</li> </ul>
Mesh Nets and Shapes	it can be included in the extracted SPICE circuit by selecting this option  Pin-based: Reference Pin(s) Has Partial Inductance

In the **Model Selection** section, partial inductance reports for power and ground nets are also available.



# LESSON SEVEN: 3D-EM OPTIONAL FIELD SOLVER IN XTRACTIM

#### Introduction

Cadence 3D-EM is an optional field solver for XtractIM. It's targeted to solve simpler packages such as lead frame package and two-layer BGA package with higher accuracy. The workflow is totally consistent with the existing hybrid solver bases.

The integration of 3D-EM and XtractIM is only applied for single-die single-BGA and single-die lead-

frame for Net-based RLGC/IBIS model at single-frequency.

For better performance, it is recommended that you select no more than 20 nets with at most four layers.

#### **Enabling 3D-EM Field Solver**

1. Make sure all the workflow setup is completed with green check-mark.



2. Choose Tools > Options > Edit Options....



- 3. Click Field Solver Engine under Simulation (Advacned) in the Options window.
- 4. Check 3D-EM Solver in Field Solver Engine Option.

Options		×
File  General File Manager Save Options	Change the 'Field Solver Engine' options in XtractIM	
Hotkeys Layout (*) Grid and Unit View Processing Trace Error Checking <b>3D Layout View</b> (*) Display Quality <b>Simulation (Basic)</b> (*) General Net and Coupling Special Void Output SPICE Circuit Report <b>Simulation (Advanced)</b> (*) Electric Models Mesh Nets and Shapes Field Solver Engine	Field Solver Engine Option	
	Default Apply OK Cance	

#### 5. Click OK.

6. Click the Start Simulation button to run simulation.

ſ	XtractIM - 3D_001_Sample_FC_1.ximx - [3D_001_Sample_FC.spd Layer View]										
	<u> </u>	Workspace	Edit	View	Mode	Setup	Tools	Window			
		💕 🔒 🕶 🛛			888	<b>F</b> +	⊡ ⊕	000			
	All	Enabled Net(s)	St	art Simu	lation <b>I</b>	± Ŧ	• = #	) 🔐 ĸ			
	<b>\\$</b>	·									

3D-EM is automatically launched as solver, and RLC result is obtained.

Workspace View Window Help					_ 6' ×
					cādence 💷 🖉
		10 · · · · · · · · · · · · · · · · · · ·	Extractor Result		
Workflow: XtractIM X	👐 ++ \$ \$ 🕆 🕆 🖻 🏫 🖂	II 💭 Self Terms 🔻 Res	istance 🔻		
Model Extraction					
Manage Workspace	Self Terms			Extractor Result	
Load Workenare	(Self)				
Load a New/Different Layout	Mutual Terms				
	(Net1_VDD_1)				
Package Setup	(Net2_VDD_2)				
Package Type: Flip-Chip	(Net3_VDD_3)				
<ul> <li>Circuits</li> </ul>	(Net4_VDD_4)				
<ul> <li>Stackup</li> </ul>	(Net5_Net_1)				
✓ Bumps	(Net6_Net_2)				
<ul> <li>Solder Ball</li> </ul>	(Net7_Net_3)				
Nets	(Net8 Net 4)				
Simulation Setup	(Net9 Net 5)				
Module: IBIS/RLGC	(Net10 Net 6)	-			
Simulation Type: Net-Based	(Net11 Net 7)				
View/Europet Results	(Alust 2 Alust 8)				
view/Export Results					
Summary					
SPICE/IBIS Model					
RLC Per Net					
RLC Distributions					
CrossTalk (Single-Ended)					
3D View					
Histogram					
Save Results					
Load Results					
Report					
Customize Workflow 🛛 🗧					
	TCI Command	1			
	The commons				
	The node {Node05392!!BGA1-D4::VSSc TCL Regult() ins1):	ore) is one of positive poles in the port (Port	_Group2::VSScore}.		
	The node (Node05386!/BGA1-C10::VS5	core} is one of positive poles in the port (Por	t_Group2::VSScore}.		
	TCL Result(Line -1):	and in our of a status sales in the seat from	Comment (Million and )		
	TCL Result(Line -1):	orey is one of positive poles in the port (Port	_oroupz::vsscore).		
	No node is hooked.				
				Generating 2D Mark - [Port Cuper]	
(er: 13.0.2.12022 (XtractIM)	Moure	mm): X: -14 509, X: 11 558		Generating 50 means [Poir Curves]	

A temp3DFEM.spd file is generated for 3D-EM simulation. This SPD file has all settings required for 3D-EM, including:

- Port defined
- Frequency settings
- Solver options
- Geometry settings

You can use this SPD file for advanced 3D-EM simulation.

# **Results Display**

• With 3D-EM field solver enabled, the following result is available.

View/Export Results 🛛 🙆
Summary
SPICE/IBIS Model
RLC Per Net
RLC Distributions
Segment RLC
RLC vs. Net Length
CrossTalk (Single-Ended)
3D View
Histogram
CrossTalk (Diffpair vs Single-Ended)
3D View
Histogram
Save Results
Load Results
Report

• In the SPICE/IBIS Model, partial inductance reports for power and ground nets are also available.



# Chapter

# **RLGC Module: Net-based Simulation of Multi-die Stacked-BGA Packages**

This chapter takes you through the steps to use the XtractIM tool in the simulation of the multi-die stacked BGA Package.

# **PREPARE FOR SIMULATION**

Collect this information before you begin the simulation.

- Make sure your files have been translated into SPD format.
- Have the Stackup information ready.
- Have the Bump and Solderball diameters, length, heights and conductivity ready.

# **LESSON ONE: SIMULATION SETUP**

#### Simulation Overview

- 1. Load an existing file (.xml file) or open a layout file (.spd file).
- 2. Select a package type: Wirebond or Flip-Chip, single BGA or stacked BGA.
- 3. Setup the circuits: Die-circuit or Board circuit.
- 4. Setup the Stackup. Set parameters for the Bump / Solderball medium layer.
- 5. Set the **Bump** data if you choose a Flip-Chip package.
- 6. Set the Solder Ball data. Select the nets for extraction.
- 7. Setup extraction frequency and capacitance / inductance output control.
- 8. Save the workspace.
- 9. Save Layout files.
- **10.** Run the simulation.

#### **Setup Package Simulation**

Simulation setup is similar to the setup procedures described in *IBIS/RLGC Module: Net-based Simulation of Single-die Single-BGA Packages*. The only difference is in three steps.

- Select a Package Type
- Setup Circuits
- Setup Stackup

#### **Setup Package Type**

- 1. Click on the appropriate radio button from these options:
  - Flip-Chip
  - Side-by-side Die
  - Single BGA
  - Single Die
  - Stacked BGA
  - Stacked Die
  - Wirebond

or select both Wirebond and Flip-Chip for various packages.

The default package type is Single Die, Single BGA, Wirebond.

- 2. Click OK to save your selection.
- 3. Click **Cancel** if you wish to start over and re-enter your settings.



#### **Setup Circuits**

- 1. Click on **Circuits** in the Workflow pane to setup the Circuits data for a Flip-Chip package. A new pane opens.
- 2. Right-click on the desired circuit.
- 3. Select it as Die circuit (you can also select it as Capacitor circuit).
- 4. Click Next.
- 5. Right-click on another desired circuit.
- 6. Select it as a **Board** circuit.
- To set up the second as a Board circuit, choose: Select as Board circuit
- 8. Click Finish to finish the setup.
- 9. Select the multi-die circuit if the package has multi-dies.

d Name	Ckt Model $ abla$	Die/Board/Compc Ckt Type		Ckt Name	Ckt Model	Ckt Type	d/Compc	
OPtop	POP top			POPtop	POP top	Board		
OPbottom	POP_bot			POPbottom	POP_bot		_	
1	FC	Die		U1	FC	Die	Se	elect as Board circuit
L	Cap0402			C1	Cap0402		De	eselect as Board circuit
1	Cap0402			C2	Cap0402			
	Cap0402			C3	Cap0402			
	Cap0402	Coloritor	Dia sinanti	C4	Cap0402			
i	Cap0402	Select as	Die dircuit	C5	Cap0402			
i	Cap0402	Deselect	as Die circuit	C6	Cap0402			
7	Cap0402	Select as	Capacitor circuit	C7	Cap0402			
3	Cap0402	Deselect	as Capacitor circuit	C8	Cap0402			

# **Setup Stackup**

- 1. Click on Stackup. The Stackup window opens.
- 2. In the Layer Name column click on:

Signal\$Bottom layer (Signal\$136C4EF0M4)

A pop-up window opens.

3. Select

Insert Under

A second pop-up window opens and displays layer options.

4. Click:

Solderball Medium Layer, Signal01 Layer, and Medium01 Layer

A menu opens.

 To insert all layers under the Signal\$Bottom layer (Signal\$136C4EF0M4) POPbottom

<b></b>	up								_	- 🗆 🗙
Layer Icon	Layer Name		Thickness(	Conductivity(S	с	Trace Width(	Shape Name	Permitti	Loss Tangent	From File
	Signal\$136C4D70	M1	1.5000e-002	5.8000e+007		1.0000e-001				
	Medium\$136C4B70D2 1.2500e-00		1.2500e-001					4.2000	0.0000	
	Signal\$136C4DF0	VSS	1.5000e-002	5.8000e+007		1.0000e-001	Shape\$136			
	Medium\$136C4AF	=0D3	1.2500e-001					4.2000	0.0000	
	Signal\$136C4E70	VDD	2.0000e-002	5.8000e+007		1.0000e-001	Shape\$136			
	Medium\$12F371E	8D4	1.2500e-001					4.2000	0.0000	
	Signal\$136C4EF0	M4	1.5000e-002	5.8000e+007		1.0000e-001				
		]	Insert Above 🕨							
		]	Insert Under 👌	Signal Layer						
		[	Delete	Medium Layer						
				Plane Layer						
				C4Bump Medi	um La	iver, Signal01 La	ver		•	
				Solderball Me	dium	Layer, Signal01 I	Layer, and Med	lium01 Laye	er POPto	op
<						1		)	POPb	ottom
Total Thick	ness: 4.4000e-0	001 mr	n					Unit:	mm 🔽 Vie	w Material
Solder Ball	Layer 🗌 C4 Bum	ip Lay	Right-dick on a er layer.	a dielectric layer to sp	ecify it	as a bump or solder	r ball Impo	ort 🗌	ок	Cancel

#### **Setup Bump and Solder Ball Medium Layers**

The newly-added signal layer is found at the end of the solderball.

- 1. Right-click on the **Signal\$Top** layer.
- **2.** Insert a **Bump Medium Layer** and a **signal layer** above Signal\$Top. The added signal layer is the end of the Bump.
- **3.** Return to the **Stackup**.
- 4. View the Bump and Solder Ball Medium Layers as they are created.
- 5. Edit the medium parameters for Bumps, if desired.
- **6.** Edit the solderball, if desired.
- 7. Edit the PCB medium layers, if desired.

+ œ ∞ ⇔ ≡ € 8: 4 18 A	
Wizard X	
Select the Die circuit from the list and click Next	
Ckt Name Ckt Model Die/Board Ckt Typ	
D1 Die1 Die D2 Die1 Die	
< Back N	
Right-click on a circuit name to select/deselect as Die circuit	Chi   Vi     Computing completed
Mouse(mm):	Computing completed

# Setup Bumps to a Side-by-Side Die Package

If the side-by-side Die Flip-Chip package has the same Bump height in all die circuits, it is treated as a **distributed die package**.

If the heights are different, it is treated as a stacked die package.

- 1. Add one Bump layer.
- 2. Open the Stackup for the distributed Bump die package.

You can bind them together to add the same Bump medium layer for each die circuit.



 After adding the Bump for D1, select: Bind to Die Circuit: D2

Both D2 and D1 have the same layer thickness.

Stackup	)								_	
Layer Icon	Layer Name Signal02 C4bump01 Signal\$02E45508M1	Thickness( 5.0000e-003 1.0000e-001	Conductivi 5.0000e+00	ty(S )7	c	Trace Width( 1.0000e-001	Shape Name	Permitti	Loss Tangent	From File
	Medium\$02F45308 Signal\$02F455888 Medium\$MED_SOL Signal\$EXT_SOLDE	Insert Abo Insert Und Delete Bind to Die	er · ·	7 7 D2		1.0000e-001	Shape\$02F	4.2000 4.0000	0.0000	
	Medium\$MED_REF Solderball01 Signal01 Medium01	5.0000e-002 5.0000e-001 1.0000e-003 5.0000e-002	5.8000e+00	)7		1.0000e-001		4.0000 1.0000 4.0000	0.0000 0.0000 0.0000	
<										>
Total Thickness:     1.3756e+000 mm       Unit:     mm       Solder Ball Layer     C4 Bump Layer         Import     OK   Cancel										

# **Output IBIS .pkg Model for Each Die-to-Board Path**

 To output IBIS .pkg model for each die-to-board path, select Tools > Options > Edit options...

The **Options** window open.

File       Image: Save Options         Save Options       Output SPICE Circuit' options in XtractIM         Use Save Options       Image: Save Options         Hotkeys       Image: Save Options         Card and Unit       Image: Save Options         View       Processing         Processing       Image: Save Options         Trace       Error Checking         3D Layout View       Image: Save Options         Display       Image: Save Options         Quality       Simulation (Bask)         Save Options       Image: Save Options         Save Options       Image: Save Options         Save Options       Image: Save Options         General       Report LC Matrices         Image: Save Options       Image: Save Options         Save Options       Image: Save Options         Simulation (Advanced)       Image: Save Options         Electric Models       Mesh         Mesh       Nets and Shapes	Options		×
General   File Manager   Save Options   Hotkeys	File 💿		
Hotkeys         Layout       Image: Constraint of the stand stapes         Crid and Unit       Image: Constraint of the stand stapes         View       Processing         Trace       Image: Constraint of the stand stapes         Displey       Image: Constraint of the stand stapes         Simulation (Bask)       Image: Constraint of the stand stapes         Simulation (Advanced)       Image: Constraint of the stand stapes         Simulation (Advanced)       Image: Constraint of the stand stapes	General File Manager Save Ontions	Change the 'Output SPICE Circuit' options in XtractIM	
Layout       Image: Constraint of the state	Hotkeys	Output SPICE Circuit	
Grid and Unit         Ylew         Processing         Trace         Error Checking         3D Layout View         Output JBS         Quality         Quality         Quality         General         Net and Coupling         Special Yold         Output JBS         Decirities         Simulation (Advanced) ●         Electric Models         Mesh         Nets and Shapes	Layout 🙆		
Error Checking	Grid and Unit View Processing Trace	Net Name Included in Circuit Node Name	
3D Layout View	Error Checking	Keep All Coupling Terms to Power Nets	
Justice       Output IBIS .pkg file for Multi-die Stacked-BGA Package         Simulation (Basic) <ul> <li>(Each. pkg model represents one-die to one-board path assuming other dies and board to be open/floating )</li> <li>Simulation (Advanced)</li> <li>Electric Models             <ul> <li>Mesh</li> <li>Nets and Shapes</li> <li>Its and Shapes</li> </ul></li></ul>	3D Layout View	Export LC Matrices	
Simulation (Basic) <ul> <li>(Each .pkg model represents one-die to one-board path assuming other dies and board to be open/floating )</li> <li>(Each .pkg model represents one-die to one-board path assuming other dies and board to be open/floating )</li> </ul> Simulation (Advanced)              Electric Models         Mesh           Nets and Shapes             Nets and Shapes <ul> <li>(Instance)</li> <li>(Instance)</li> <li>(Instance)</li> <li>(Instance)</li> <li>(Instance)</li> <li>(Instance)</li> </ul>	Quality	✓ Output IBIS .pkg file for Multi-die Stacked-BGA Package	
Mesh Nets and Shapes	Simulation (Basic) ( General Net and Coupling Special Void Output SPICE Circuit Report Simulation (Advanced) ( Electric Models	(Each .pkg model represents one-die to one-board path assuming other dies and board to be open/floating )	
	Mesh Nets and Shapes		
Default Apply OK Cancel		Default Apply OK Cance	

- 2. Click Output SPICE Circuit under Simulation (Basic).
- 3. Select the Output IBIS .pkg file for Multi-die Stacked-BGA Package checkbox.
- 4. Click OK.

# LESSON TWO: SAVE WORK AREAS

#### **Layout File**

- **1.** Click on the workspace.
- 2. Click on the Open Layout File icon (green) to open the project file.
- 3. Click on the Save Layout File icon (green) to save the project file.
- 4. Use Save as to save the layout file under a different name.

NOTE!Saving the workspace does not automatically save the .spd file.Saving the.spd file does not automatically save the workspace.

#### **Workspace**

- 1. Click on the workspace. The workspace opens. Note the workspace toolbar.
- 2. Click on the Save Workspace icon (yellow) in the toolbar.
- To save the workspace under a different name, select: Save as

# **LESSON THREE: RUN THE SIMULATION**

Click on the **Play** button **I** at the top of the window to start the extraction (simulation).

XtractIM only extracts RLCG for the net which has at least one pin at the Die side and at least one pin at the board side.

At the beginning of the simulation, if some nets have Die-Board mis-match, a pop-up window opens. You are asked to select the next action.

- **Continue** Continue the simulation
- More Information Examine what nets are mis-matched ٠
- **Stop** Cancel the simulation

#### **Investigate Mis-matched Nets**

•

- 1. The More Information window lists all the mis-matched nets.
- 2. Investigate the mis-matched nets to see whether it is a special design or a defective design.
- 3. Decide whether or not to proceed with the simulation.
- 4. Choose Continue, Stop or More Information.

If 30 seconds pass and the user has not made a choice; by default, the simulation continues.

# **LESSON FOUR : OBSERVE AND SAVE SIMULATION RESULTS**

XtractIM performs calculations for each net. The calculations include:

- Conductance
- Mutual capacitance with other nets
- Mutual loop inductance
- Resistance
- Self capacitance
- Self loop inductance

# **Display SPICE Model Results**

The illustration in the right corner shows the detail of the Circuit topology for a 2-die BGA package.

Workflow: XtractIM 🗙	Extractor Result
Default Manage Workspace Load Workspace Load Workspace Load a New/Different Layout Package Setup Package Type: Wirebond ✓ Circuits ✓ Stackup ✓ Solder Ball ✓ Nets	View Model Selection SPICE T-model DC_R of Each Path RLC of Each Path Coupling of Each Path
Simulation Setup (*) Module: IBIS/RLGC Simulation Type: Net-Based View/Export Results (*) Summary SPICE Model Branch RL Save Results Load Results Customize Workflow *	.SUBCKT XIM_MultiDie_Sample3_WB2distributed_2diesidebyside_wbwb_newnl_NetBaseSPICE ↑       +     D1_10       +     D2_10       +     D2_3       +     D2_13       +     D1_14       BGA1_14       +     D1_14       BGA1_18       +     D1_2       +     D1_2       BGA1_7       +     D1_7       BGA1_7       +     D2_7       +     D1_9       BGA1_8       +     D1_8       BGA1_8       +     D1_8       BGA1_9
Ver: 4.0.1.04171 (SIG4) Mouse(u	m): X: -8692.371. Y: 5569.138
#### **View DC Resistance**

**1.** To view the DC Resistance of Power, Ground and Signal Nets of each circuit-to-circuit path, click:

DC\_R of Each path

**2.** In the drop-down pane make a selection for a circuit-to-circuit path. In the following example the selection is:

D1 > D2

<ul> <li>SPICE T-rr</li> <li>DC_R of E</li> <li>RLC of Eac</li> <li>Coupling o</li> </ul>	nodel ach Path ch Path f Each Path			~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
D1 -> D2		·	-	
NetName	DC B(Ohm)			
vdd Net_12 Net_13 Net_14 Net_3 Net_4 Net_5 Net_6 Net_6 Net_7 Net_8 gnd	0.0128746 0.0286816 0.0286816 0.0286816 0.0821354 0.0835846 0.0781685 0.0781685 0.082948 0.0824216 0.00852792			

#### **Display RLC of Each Path**

- To view the Net Length, Self R, Self L, Self C, or Delay of a Signal Net., click on RLC of Each Path
- 2. Use the drop-down pane to select a circuit-to-circuit path.

<ul> <li>SPICE T-mo</li> <li>DC_R of Each</li> <li>RLC of Each</li> <li>Coupling of E</li> <li>D1 -&gt; D2</li> </ul>	del ch Path Path Each Path		~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~		<b>//</b> 78888
SignalNetNa vdd Net_12 Net_13 Net_14 Net_3 Net_4 Net_5 Net_6 Net_7 Net_8	NetLength(m) 0.865615 0.865615 7.32683 7.62281 6.72973 6.72973 7.4928 7.38528	SelfR(Ohm) 0.0259458 0.0389037 0.0388801 0.0390491 0.136337 0.139003 0.135472 0.136465 0.138143 0.13889	SelfL(nH) 0.557809 0.782729 0.774898 0.750168 5.14279 5.43555 5.03568 5.21655 5.37479 5.51948	SelfC(pF) 3.70371 0.0968899 0.097438 0.0969146 1.0151 1.02052 1.09907 1.10419 1.04397 1.0466	Delay(pS) 45.4529 8.70853 8.68934 8.52656 72.2526 74.4787 74.3948 75.8949 74.9076 76.0047

#### **Display Coupling of Each Path**

- To view Mutual Land Mutual C among nets along the path, click: Coupling of Each Path
- 2. Use the drop-down pane to select the circuit-to-circuit path.



#### **Summary of the Extracted Results**

- 1. Click on Summary to open a brief summary of the extracted R, L, and C in the SPICE circuit.
- 2. View the maximum and minimum values, and other information in the Brief Summary window.

```
Extractor Result
[Version]
                               4.0.1.04171
[Date]
                              04/16/2010
[Package Name]
                              C:\Users\gkang\Desktop\Samples\Multi-die Sample
[Description]
                              C:\Users\gkang\Desktop\Samples\Multi-die Sample
[Nets Extracted]
                              16
                              30MHz
[Frequency of Extraction]
                              62.2883
[Max R(mOhm)]
[Min R(mOhm)]
                              7.26778
[Max self-inductance L(nH)]
                             2.40819
[Min self-inductance L(nH)]
                              0.356281
[Max self-capacitance C(pF)] 3.70371
[Min self-capacitance C(pF)] 0.0968899
```

#### **Branch RL and Total C**

Click Branch RL to view the display the Branch R, L, and total C of each net.

If a branch is missing from a net, the cell is left empty.

Net Name	C-total (pF)	R D1(Ohm)	R D2(Ohm)	R BGA1(Ohm)	LD1(nH)	L D2(nH)	L BGA1(nH)
vdd	3.70371	0.0189957	0.0190755	0.00726778	0.502131	0.494327	0.360268
Net_0	0.586283		0.0499985	0.0144941		1.34022	0.898667
Net_1	0.519641		0.0467442	0.0123515		1.23658	0.78594
Net_10	0.507267	0.046825		0.012005	1.33644		0.779702
Net_11	0.573214	0.0502395		0.0140962	1.4453		0.889757
Net_12	0.0968899	0.0183871	0.0502395		0.3721	1.4453	
Net_13	0.097438	0.0183802	0.0183871		0.368179	0.3721	
Net_14	0.0969146	0.0184685	0.0183802		0.356281	0.368179	
Net_2	0.585876		0.0499099	0.0142809		1.32604	0.843666
Net_3	1.0151	0.0611592	0.0589	0.012166	2.2961	1.89191	0.955124
Net_4	1.02052	0.0622883	0.0594929	0.0125821	2.40819	1.96941	1.00588
Net_5	1.09907	0.0607214	0.0603477	0.0129294	2.1364	2.03507	1.023
Net_6	1.10419	0.0607857	0.0610096	0.0129482	2.12252	2.17874	1.0308
Net_7	1.04397	0.0602726	0.0612385	0.012329	2.08603	2.26651	0.99801
Net_8	1.0466	0.0602456	0.0619516	0.0123209	2.07494	2.39202	0.998978
Net_9	0.5723	0.050101		0.0138617	1.42172		0.833771

#### RLGC MODULE: NET-BASED SIMULATION OF MULTI-DIE STACKED-BGA PACK-AGES 68

The figure below illustrates the Branch RL and Total-C for one net of a 2-die 1-BGA package. It is straightforward for multi-die stacked-BGA packages.



#### **Save Results and Output Files**

1. Click:

Save Results

The Save Extractor Result window appears.

- 2. Enter a name in the File name window.
- 3. Click on Save. The results are saved in a binary file named as result and as:

result\_spd\_file\_name.xim

- 4. Click on **Cancel** if you do not want to save the results in the file name you entered.
- 5. Save all the output data including Summary and one SPICE model in the result and result\*.xim files.

The result file is created only when the user chooses to save the output data.

You'll see these output files on hard disk.

- Branch RL File An .csv file including the branch R, L, and total C of each net
- Coupling of Each Patch A .csv file including Mutual L and Mutual C among nets along every circuit-to-circuit path
- DC R of Each Path File A .csv file including each net's DC Resistance
- One SPICE Circuit File Named \*.ckt
- RLC of Each Path File A .csv file including each Signal net name, Length, Self R, Self L, Self C and Delay

Save Extrac	tor Result /	As						?	×
Save in:	C Stacked-BGA	_Sample_Files	*	G	ø	Þ	<b></b> -		
My Recent Documents Desktop My Documents	<ul> <li>ExtractorRun</li> <li>pop_flipchip.:</li> <li>PoP_flipchip.:</li> <li>pop_flipchip_</li> <li>pop_wirebon</li> <li>POP_wirebor</li> <li>ResourceProi</li> <li>Un_Xtracted_</li> <li>New Folder</li> </ul>	TimeError.log spd kml DCResistance.csv Extractor.err RLCofEachPath.Csv TableBranchRL.csv Test_for_Extractor.spd letBaseSPICE.ckt d.spd id.xml file_Extractor.log _NetName.log							
<b></b>	File name:	ResultWanted				*		Save	•
My Network	Save as type:	All File (*.*)				*		Canc	el

#### **Load in Saved Results and Files**

- To load saved results, select: Load Results
- 2. View the present results or the loaded results.
- 3. Unload a loaded result by clicking on the Unload Extractor Result icon in the toolbar.
- 4. Use the Load and Unload Result buttons.

All output files, including .csv files, are saved in the same directory as the \*.spd file.

Workflow: XtractIM	Result_XIM_Saved	<b>FileNames</b>					<b>↓</b>
Default 🛛 🖉							
Manage Workspace ( Load Workspace Load a New/Different Layout Package Setup ( Package Type: Wirebond Circuits Stackup Solder Ball Vets	View Model Sel     O SPICE T-mo     O DC_R of Eac     O RLC of Each     O Coupling of E     D1 -> D2	lection del h Path Path Each Path		^^^~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~		^//70000	
Simulation Setup							
Module: IBIS/RLGC Simulation Type: Net-Based View/Export Results (*) Summary SPICE Model Branch RL Save Results Load Results Customize Workflow *	Signalivetiva vdd Net_12 Net_13 Net_14 Net_3 Net_4 Net_5 Net_6 Net_6 Net_7 Net_8	NetLength(m 0.865615 0.865615 7.32683 7.62281 6.72973 6.72973 7.4928 7.38528	SelfR(Unm) 0.0259458 0.0389037 0.0388801 0.136337 0.139003 0.135472 0.136465 0.138143 0.13889	SelfL(hH) 0.557809 0.782729 0.774898 0.750168 5.14279 5.43555 5.03568 5.21655 5.37479 5.51948	SeffC(pF) 3.70371 0.0968899 0.097438 0.0969146 1.0151 1.02052 1.09907 1.10419 1.04397 1.0466	Delay(ps)           45.4529           8.70853           8.68934           8.52656           72.2526           74.4787           74.3948           75.8949           74.9076           76.0047	
<	e(um): X: -56655.052,	Y: 40557.491			🔗 Ready		

# **LESSON FIVE: BATCH MODE SIMULATION**

- To run a simulation in Batch Mode select: Start -> Run
- 2. Change to the directory where the XtractIM.exe file is located.

#### **Batch Mode Example**

If you want to use the project (.spd file) defaulted in the workspace file (.xml file), enter: xtractIM -b "Full\_path\_toMy\_xml\_File\xml filename"

If you want to use a different project file other than the one in the .xml file, enter:

xtractIM -b "Full\_path\_toMy\_xml\_File\xml

filename" "Full\_path\_toMy\_xml\_File\new\_spd-filename"

# Chapter 5

# Optimized Broadband Module: Net-based Simulation for Single-die Single-BGA Packages or Multi-die, Stacked-BGA Packages

This chapter takes you through the steps to use the XtractIM tool Optimized Broadband Module in the net-based simulation of a single-die BGA package. Simulation of multi-die, stacked-BGA package es is the same as single-die, single-BGA packages.

# **LESSON ONE: SETUP FOR THE SIMULATION**

# **Package and Simulation Setup**

- **1.** Load an existing workspace file (.xml file).
- **2.** Open a layout file (.spd file).
- 3. Select a package type: wirebond or flip-chip.
- 4. Setup the circuits: select or deselect Die-circuit and Board circuit.
- 5. Set the Stackup: set parameters for the Bump / Solderball medium layer.
- 6. Set the Bump data if it is a flip-chip package.
- 7. Set the Solder Ball data.
- 8. Select the **nets** for extraction.
- 9. Select Simulation Module: Optimized Broadband Module.
- **10.** Select output SPICE circuit.
- **11.** Setup the Extraction Frequency band.
- **12.** Save the Workspace and Project file.

Steps 1-8 and Step 11 are exactly the same as *Preparing for the Simulation* in *IBIS/RLGC Module: Netbased Simulation of Single-die Single-BGA Packages*. This chapter describes steps 9-10 in detail.

#### **Simulation Setup**

**1.** Select:

Simulation Setup -> Module

2. Select the IBIS/RLGC Module;

or select Module: 6.



**3.** In the workflow window click:

**Circuit Topology** 

- 4. Select the circuits to be extracted under the Circuit Section.
  - If you do not select a circuit, no RLGC SPICE model is extracted
  - If you select all of the circuits, all three models will be given
  - If you select a single circuit, choose T-model or Pi-model

Simulation Setup -> Circuit topology
✓ 1-section       ✓ 2-section         Model       ● T-model         ● Pi-model       ●
OK Cancel Default

**5.** In the Workflow pane click:

Frequency Range of Extraction

- 6. Set the Frequency Range.
- 7. Input the lower frequency and the upper frequency.

Simulation Setup -> Frequency Range of Extraction	×
Star Frequency: 100KHz	
End Frequency: 2GHz	
	OK Cancel
	Cancer

#### **Output Frequency Range Options**

1. To open the Output Frequency Range window, select:

Tools ->Options -> Edit Options -> Output Frequencies

The default setting is disabled.

**2.** Change the sweeping mode and frequency point number in the set Frequency Range window. The default setting for **Enhanced Circuit Topology** is disabled.

If **Enhanced Circuit Topology** is enabled, the circuit includes more R and L elements to better fit the original S-parameter.

This option requires 3x - 9x simulation time.

The default setting is disabled.

**3.** If the Original S-parameter is enabled. It is saved in Sigrity BNP format and on hard disk in Touchstone format.

File 🤅							
General File Manager Save Options		Chang	e the 'Outpu	t Frequencies' o	options in Xtr	actIM	
Hotkeys		Starting Freq.	Ending Freq.	Sweeping Mo	Freq. Increm	Points/Decade	
Layout	•	1KHz	10MHz	Log		10	
Grid and Unit		10MHz	100MHz	Log		20	
View		100MHz	10GHz	Log		40	
Processing							
Trace							
Error Checking							
BD Layout View	2						
Display							
Quality							
Simulation (Basic)	2						
General							
Net and Coupling							
Network Parameters		· · · · · · · · · · · · · · · · · · ·				1. · · · ·	
Output Frequencies							
Enhanced Circuit Topology		· · · · · · · · · · · · · · · · · · ·				1	
Original S-parameter: More	e Forma						
Report		1				t	
Simulation (Advanced)							
Electric Models		1					
Mesh							
Nets and Shapes							
Special Handling							
			5				
	>						

#### **Output Original S-parameter with More Format**

By default the original S-parameter is saved as a BNP file.

1. Select:

Tools > Options > Edit Options > Original S-parameter: More Format

2. Select:

Original S-parameter in Touchstone

A file with Touchstone format is also saved.

3. Select:

Original S-parameter in BNP AFS format

A file with BNP AFS format is also saved.

# LESSON TWO: SAVE WORK AREAS

#### **Layout File**

- **1.** Click on the workspace.
- 2. Click on the Open Layout File icon (green) to open the project file.
- **3.** To save the layout file under a different name, select:

Save as



#### Workspace

- 1. Click on the workspace. The workspace opens.
- **2.** View the Workspace toolbar.
- 3. Click on the Save Workspace icon (yellow) in the toolbar.
- To save the workspace under a different name, select: Save as

#### **LESSON THREE: RUN THE SIMULATION**

- 1. Click on the **Play** button **i** at the top of the window to start the extraction (simulation).
- 2. The Optimized Broadband Module only extracts RLCG for the net which has at least one pin at the Die-side and at least one pin at the board side.

At the beginning of the simulation, if some nets have Die-Board mis-match, a pop-up window opens.

- **3.** Select the next action.
  - **Continue** Continue the simulation
  - More Information Examine what nets are mis-matched
  - Stop Cancel the simulation

#### **Investigate Mis-matched Nets**

- 1. The More Information window lists all the mis-matched nets.
- 2. Investigate the mis-matched nets to see whether it is a special design or a defective design.
- 3. Decide whether or not to proceed with the simulation.
- 4. Choose Continue, Stop or More Information.

If 30 seconds pass and the user has not made a choice; then, by default, the simulation continues.

Die an	d Board pins do not match $ imes$
	The pins of the die circuit do not correspond to the board circuit pins. Click More Information to see the list of mismatched pins.
	Enabled nets : 19
	Nets in ground group : 1
	Nets with pin-mismatch : 1
	Nets to be extracted : 18
	You may Continue or Stop the simulation.
	Continue Stop More Information

# **LESSON FOUR : OBSERVE AND SAVE SIMULATION RESULTS**

XtractIM performs calculations for each net. The calculations include:

- Conductance
- Mutual Capacitance with other Nets
- Mutual Loop Inductance
- Resistance
- Self Capacitance
- Self Loop Inductance

#### About the S - Parameter and Errors

After the simulation completes, view the S-parameter and errors in the Layer View window

- Bottom figure (S Imaginary) Imaginary / phase of the S-parameter element
- Middle figure (S Real) Real / amplitude of the S-parameter element
- Top figure (Average error in S) Average S-parameter error for each net

#### **View S - Parameter and Errors**

- 1. Drag the black vertical marker to Net i. The  $S_{ii}$  is shown.
- 2. Click on net names in the middle column to view the:

Frequency-averaged S-parameter error of the circuit S-parameter vs. the Original S-Parameter

- 3. View the port names listed with net names plus port at Die- or Board- side.
- 4. View the average error for 1-, 2- and 3-section circuit topology.
- 5. Return to Net i.
- 6. View all sections, single section, or two sections results.
- 7. View averaged S-parameter errors of a non-optimized or optimized circuit.
- 8. View the port name in the error column to view any mutual S-parameters.

#### **S-parameter Examples**

The error definition of circuit S-parameter vs. original or simulated S-parameter is shown in these examples.

Define an error for each net

 $\begin{array}{l} \mbox{Error(net,freq)} = \frac{1}{4} \cdot \{|S_{11\_ckt} - S_{11\_sim}| + |S_{22\_ckt} - S_{22\_sim}| + |S_{12\_ckt} - S_{12\_sim} + |S_{21\_ckt} - S_{21\_sim}| \} \end{array}$ 

Net-averaged performance vs. frequency

Error1(freq)=  $\frac{1}{Net_No} \sum_{Net}$  Error(net,freq)

Freq-averaged performance vs. net

Error2(net)= 
$$\frac{1}{Freq No} \sum_{Freq}$$
 Error(net,freq)



#### **View Net Frequencies**

- 1. Click the S-parameter button in the toolbar.
- 2. In the drop-down menu, select:

Net Performance vs. Frequency

The frequency is displayed in the Layer View window.

- 3. Click on a net name in Net Name list.
- 4. View the Single net average error in S chart.



- 5. Click on each net name in the list.
- 6. View the Single net average error in S chart for every net.



- 7. Click on a figure. A pop-up menu appears.
- 8. Click:

Show Legend Border



#### **View Summaries and Models**

- 1. Click on **Summary** to bring up the summary and tabulated data for R, L, and C.
- 2. View the overall results in the top right window.
- **3.** Examine the results for:
  - Frequency Minimum
  - Frequency Maximum
  - Max R
  - Max self-capacitance C
  - Max self-inductance L
  - Min R
  - Min self-capacitance C
  - Min self-inductance L
  - Package Name
- 4. Click on SPICE Model to bring up the display of the SPICE Circuit model.

		Extractor Result 🗸 🖌 🖺
📂 🚽 🤟 - 🔍 - 🖂 🖽 🖸	2	
Workflow >	Extractor Result	
Load Workspace	[Version]	1.2.b0
Load a New/Different Layout	[Date]	08/07/2007
Package Setup 🔗	[Package Name] [Description]	C:\Documents and Settings\gkang\Desktop\BroadBan C:\Documents and Settings\gkang\Desktop\BroadBan
Package Type: Flip-Chip	[Number of Sections]	2
✓ Circuits	[Nets Extracted]	10
🖌 Stackup	[Frequency Minimum]	0.01MHz
🖌 C4 Bumps	[Frequency Maximum]	2000MHz
🖌 Solder Ball	[Min B (mOhm)]	0.351416
✓ Nets	[Max self-inductance L(nH)]	0.696014
Simulation Setup	[Min self-inductance L(nH)]	0.0453317
Sindladon Secup	[Max self-capacitance C(pF)]	74.2399
Module: Optimized Broadband	[Min self-capacitance C(pF)]	0.0709281
Circuit Topology		
Frequency Range of Extraction		
View/Export Results 🙆		
Summary		
SPICE Model		×
S-parameter and Error		>
Save Decrite	1-section 2-section	
	Mouse(mm): X: -11.996, Y: 3.03	5 Computing completed

- 5. To see the SPICE Model circuit topology click:
  - 1-section
  - 2-section
  - 3-section



#### **Save and Load Results**

- 1. Click Save Result in the workflow. The Save Extractor Result as window opens.
- 2. Enter a name.
- 3. Save the result.

The result file:

- Is saved in a binary file named result and result\_spd\_file\_name.xim
- Contains all the files (all the .csv file names)
- Can be loaded into XtractIM
- 4. In the Workflow pane click:

#### Load result

The pre-saved result is loaded.

- 5. Open the S-parameter view file and check the information.
- 6. Open the Summary view file and check the information.

OPTIMIZED BROADBAND MODULE: NET-BASED SIMULATION FOR SINGLE-DIE SINGLE-BGA PACKAGES OR MULTI-DIE, STACKED-BGA PACKAGES 86

# LESSON FIVE: BROADBAND EXTRACTION OF EXISTING S-PARAMETER

A typical workflow in interaction mode includes the steps described in *Load BNP Files and Setup for Simulation*.

Only supported BNP files are created by XtractIM.

#### Load BNP Files and Setup for Simulation

- 1. Launch XtractIM.
- 2. Open the Workspace file.
- 3. Select the desired file from the pull-down menu in the Files of type field.

Open Work	space File				? ×
Look in:	🚞 Benchmark		S (	• 🖅 🔁 🕏	
My Recent Documents Desktop My Documents	enchmark1 알 Benchmark1	xml xml			
My Computer					
	File name:			<u> </u>	Open
My Network	Files of type:	Extractor Workspace XML F	iles (* xml)	✓	Cancel
		S-parameter BNP Files (*.bnp	p)		barren er

4. Select:

Extractor Workspace XML files

* 🖽 📾 🗂 🗾 🗄 🔡 🌩	N 🔏 🔏	1001	D 🔘 🛛 🖸 🚺	🖸 🔄 🗉 🖃 🕀 🖸	Ð	
Workflow		i0 <mark>4020</mark>		40 60 80	^	Layer Selection X
Package Setup						🥗 Signal02
Nets						💇 Plane02
Simulation Setup						Plane01
D Circuit topology						Signal01
View/Export results	20					
Summary					团	
SPICE Model	0					
S-parameter and Net Error					1	
Save Results						
Load Results	120-1					View Only Active Layer
						-Display Geometry Objects By
	48					⊙ Net Color ◯ Layer Color
					~	
	<		)	>		Re-100
Ver: 1.3.a0 (SIG4)	Mouse	(mm): X: -88.687, Y:	-24.040	Computing com	plete	d

After the S-parameter is loaded the XtractIM window is refreshed.

#### **Select Extraction Nets**

- In the Workflow pane, under the Package Setup heading, click Nets. The Nets window opens.
- 2. De-select any net that is not extracted.
- 3. If VDD is deselected, the cell in the Type column is set on the default Open.

The net is considered open for both ports of this net.

Package Setup -> Nets 🗙 🗙			
	Net:	Find	
NetName	Туре	Value	
VDD			
VDDIO			
✓ D0			
✓ D1			
✓ D2			
✓ D3			
✓ D4			
✓ D5			
✓ D6			
✓ D7			
			Default OK Cancel

- 4. Click on **Type** to open the pull-down menu.
- 5. Select Load.
- 6. In the Value column, enter an actual resistance number (units: Ohm) for a net.

Package Setup -> Ne	ets		×
	Net:	Find	
NetName	Туре	Value	
VDD	Open	*	
VDDIO	Open		
☑ D0	Short		
✓ D1	Match		
✓ D2	Load		
☑ D3			
✓ D4			
✓ D5			
☑ D6			
✓ D7			
			Default OK Cancel

#### **Select Circuit Topology**

- In the Workflow pane click: Circuit Topology
- 2. To open the pull-down menu click: Circuit Section
- 3. Select the circuits to be extracted: T-model or Pi-model.

If you do not select a circuit, no RLGC SPICE model is extracted.

If you select all of the circuits, all three models are given.

#### Example

- Pi-model has already been selected for 1-section
- 1- Section and 2- Section models are selected.

ulation Setup -> Circuit topology		
✓ 1-section ✓ 2-section 3-section		
) T-model		
Pi-model		
OK Cancel Default		

# **LESSON SIX: RUN A BATCH MODE SIMULATION**

1. To run a simulation in Batch Mode, select:

Start > Run

2. Change to the directory where the XtractIM.exe file is located.

Upon completing the simulation, all output files (including .ckt, .bnp, and .csv files) are saved automatically in the same directory as the \*.spd file.

#### **Batch Mode Example**

If you want to use the project (.spd file) defaulted in the workspace file (.xml file), enter:

XtractIM -b broadband "Full\_path\_to\_My\_xml\_File\xml filename"

If you want to use a different project file other than the one in the .xml file, enter:

XtractIM -b -broadband "Full\_path\_to\_My\_xml\_File\xm filename" "Full\_Full\_path\_to\_My\_xml\_File\new\_spd filename"

OPTIMIZED BROADBAND MODULE: NET-BASED SIMULATION FOR SINGLE-DIE SINGLE-BGA PACKAGES OR MULTI-DIE, STACKED-BGA PACKAGES 92

# Chapter

# **RLGC and Optimal Broadband Module: Pin-Based** Simulation

This chapter takes you through the steps to use the XtractIM tool in a pin-based simulation of singledie single-BGA or multi-die stacked-BGA packages. The steps for single-die single-BGA RLGC module are strengthened. Those for multi-die stacked-BGA or for Optimized Broadband module are straightforward.

# **PREPARE FOR THE SIMULATION**

Collect this information before you begin the simulation.

- Make sure your files have been translated into SPD format.
- Have the Stackup information ready.
- Have Bump and Solderball diameters, length, heights and conductivity ready.

### **LESSON ONE: SIMULATION SETUP**

#### **Simulation Overview**

A typical workflow in interaction mode is the same as net-base extraction.

A qualified net is the one which has at least one pin in each of the die- and BGA- circuits.

No open circuit exits for these pairs of pins.

#### **Simulation Options**

Pin-based extraction has four options in RLGC circuit extraction. The Simulation Setup options are located on the right side of the Editor bar.

- **Option 1** In DIE or BGA circuit, choose one net as reference. This would lump all pins of the chosen net together as reference in both DIE and BGA side
- Options 2 & 3 In DIE or BGA circuit, choose one pin node as reference

Choose **auto**. XIM automatically selects a node of the net as reference. This node is generally in the center of the circuit

Choose manual. Specify a node as reference.

• **Option 4** — Mesh DIE or BGA circuit. Use one cell element as reference. Any net pins in a same cell are lumped together

#### **Setup Simulation Type**

1. Click:

Simulation Type

**2.** Select:

Pin-Based

3. Click:

Reference Net

A drop-down menu opens. Qualified nets are displayed.

- 4. Select one net as the reference net for simulation.
- 5. Select a circuit from the Circuit Name Element.
- 6. Select one simulation type from the list of four.
  - Use Reference Element
  - Use Reference Net
  - Use Reference Node (auto)
  - Use Reference Node (manual)
- 7. If you select Use Reference Net or Use Reference Node (auto), no further action is needed.

If you select **Use Reference Node (manual)** or **Use Reference Element**, perform the steps described in the following sections.

- **8.** Repeat steps 5 & 6 for each circuit (DIE and BGA or DIEs and BGAs for multi-die stacked BGA packages).
- 9. Click **OK** to save all the settings.
- 10. Click Cancel if you want to start over and enter new settings.

# **Select Reference Node (Manual)**

1. Click:

Simulation Type

2. Select:

Pin-Based

**3.** Click:

Use Reference Node (manual)

Simulation Setup -> Simulation Type				×
Model Extraction Net-Based  Pin-Based	Layer Signal\$M1 Signal\$M4	Circuit Name U1 BGA1	Circuit Model FC untitled_package	Port Reference Reference Net: VSS Use Reference Node(auto) Use Reference Node(manual) Use Reference Element Element D: (0, 0) Pin Groups: 1 × 1 ~ Use Grouped pins in MCP Header Load MCP header file: 
OK Cancel				

- 4. Click on the mouse icon.
- 5. In the Layout View window, select a Reference Net Node. The Node Name is displayed.

Port Reference Reference Net:	Use Reference Net
VSS	Use Reference Node(manual)
	Node1364!!U1-G6::VSS
	O Use Reference Element Element ID; (0, 0)
	Load MCP header file:
	Choose Group as Reference Element:

#### **Select Reference Element**

**1.** Select:

Use Reference Element

**2.** Choose:

Pin Groups

For example, 1\*1, 2\*4 or 5\*5.

- 3. Click the mouse icon at the right side of Pin Groups.
- **4.** In the Layer View window right-click to select a cell as the reference element. The selected cell becomes **blue**.

A message window appears

Use As Reference Element

5. Repeat these steps for other circuits (DIE or BGA)



**Select User Grouped Pins in MCP Header** 

**1.** To load the file with MCP Header, click <u>mathematication</u> next to the Load MCP header file field.

Name ^	Date modified	Туре	Size
CPU_Info.log	5/21/2012 3:45 PM	Text Document	
First.ckt	5/21/2012 10:49 AM	CKT File	
First_PSI.spd	5/21/2012 10:48 AM	SPD File	
MCP_Header.ckt	5/21/2012 10:49 AM	CKT File	
newx.ximx	5/23/2012 4:29 PM	XIMX File	
pkg_flipchip_6.spd	5/10/2012 3:48 PM	SPD File	
pkg_flipchip_debug.spd	5/21/2012 10:16 AM	SPD File	
Second.ckt	5/21/2012 10:56 AM	CKT File	
www.ximx	5/21/2012 3:32 PM	XIMX File	
x1.ximx	5/23/2012 4:20 PM	XIMX File	<b>•</b>
File name: MCP_Header.ckt	▼ AI	l Files(*.*)	•
		Open Cano	el

- 2. Select the MCP Header file (which has the grouped pin information).
- 3. Click Open.
- 4. In the right side of the Simulation Setup -> Simulation Type pane, select a group as Reference Element from the drop-down list.

<ul> <li>Use Grouped pins in MCP Header Load MCP header file:</li> </ul>			
	kup\XIM-12.0\Example_1\MCP_Header.ckt		
	Choose Group as Referenc	e Element:	
	U1_U1-A1		
	U1_U1-A12		
	U1_U1-E5		
	U1_U1-L11		
	U1_U1-L2		

5. Click OK.

**Reference Options** 

- Use Reference Net Lumps all pin nodes of the Reference Net as port references
- Use Reference Node (auto) Automatically selects a Pin Node of the Reference Net as the port reference; this Node is generally in the center of the circuit
- Use Reference Node (manual) Uses a defined Pin Node for the Reference Net as the Port Reference; we recommend the user choose a Node in the center of the circuit
- Use Reference Element Uses the lump of all the Reference Net Pins in the designed cell as the Port Reference
- Use Grouped Pins in MCP Header Uses the lump of all the reference net pins in the designed group by MCP header as the Port Reference

1) As always, extraction goes to those nets enabled in **Net Manager** only. If a net is included in the MCP Header but is disabled in **Net Manager**, it will not be extracted.

2) If an enabled net is not included in the MCP Header, during extraction, it will be considered as 1-cell by 1-cell lump model extraction.

If the user just wants to extract a model with bumps defined the in the MCP header (i.e. ignore those bumps not in the MCP Header), just select Tools > Options > Edit Options..., and in the **Options** window, click **Net and Couplings**, select the **Use grouped pins in MCP Header:** extraction only for grouped bumps in the input file check box, then click **OK**.

Options	د
File (Seneral General File Manager Save Options	Change the 'Net and Coupling' options in XtractIM
Hotkeys Layout Grid and Unit View Processing Trace Error Checking	Disabled Nets ✓ Keep the shapes in disabled nets (the option is also available in the Net Manager) Disabling nets that are not of interest will result in faster simulation, but might sometimes lead to less accurate result. Keeping the shapes in disabled nets is a balance of the speed (and memory) and result accuracy.
3D Layout View  Display Quality Simulation (Basic) General Net and Coupling Special Void Output SPICE Circuit Report	<ul> <li>✓ Use grouped pins in MCP Header: extraction only for grouped bumps in the input file</li> <li>Coupled traces</li> <li>✓ Disable Coupled Line Simulation (the option is also available in the Net Manager)</li> <li>If there are lots of parallel traces very close to each other, the coupling between them might be strong. Considering the trace coupling usually improves the result accuracy.</li> </ul>
Simulation (Advanced) ( Electric Models Mesh Nets and Shapes	Note: in addition to the switch here, you also need to adjust the coupling parameters for the nets of interest in the Net Manager.
	Default Apply OK Cancel

#### **Generate MCP Header File**

1. Choose Tools > Pin Group Editor...



2. Choose an available circuit name from the Circuit pull-down list. For example, FCHIP in this tutorial.
All of the enabled nets related with this circuit are listed in the Net Selection field.

Pin Group Editor	- x
☐ <u>Z</u> oom window to fit the circuit Circuit: FCHIP ▼ Iype: Die	T
Net Selection Power Nets VDD_15 VDD Ground Nets VSS Signal Nets	
Pin Grouping	
Assign Pin Groups Graphically By Grid 5 X 5 ~C	
<u>G</u> roup UnGroup Save Close	2

3. Choose a power or ground net to perform pin grouping. For example, VDD\_15 in this tutorial.

Pin Group Editor	
☐ <u>Z</u> oom window to fit the circuit <u>C</u> ircuit: FCHIP ▼ <u>Type</u> : Die	•
Net Selection Power Nets VDD_15 VDD Ground Nets VSS ⊕ ∑ Signal Nets	
Pin Grouping	
Assign Pin Groups Graphically By Grid 5 × 5 ~C Group UnGroup	
Save Clos	e

The corresponding pins for the selected net are listed in the **Pin Grouping** field.

4. Choose pins that you want to add in a group.

Pin Group Editor	
☐ Zoom window to fit the circuit Circuit: FCHIP ▼ Iype: Die	<b>•</b>
-Net Selection-	
Power Nets   WDD_15   WDD   WDD	
Pin Grouping	
A10 A10 B7 B8 B9 B10 B11 B11 B11 B12 U7 U7 U7 U9 U9 U10	
Assign Pin Groups Graphically	
By Grid 5 X 5 ~C	
<u>G</u> roup <u>U</u> nGroup	
Save	Close

5. Click the Group button.

A group is generated as Group1.

Pin Group Editor 🗆 🗙
☐ Zoom window to fit the circuit Circuit: FCHIP ▼ Type: Die ▼
-Net Selection
Power Nets
Pin Grouping
·····⊞ U11
Assign Pin Groups Graphically
By Grid 5 X 5 ~C
<u>G</u> roup <u>U</u> nGroup
<u>S</u> ave <u>C</u> lose

6. Repeat Step 4 and 5 to generate multiple groups for a net.

Pin Group Editor	
☐ <u>Z</u> oom window to fit the circuit <u>C</u> ircuit: FCHIP ▼ <u>T</u> ype: Die	T
Net Selection	
Power Nets VDD_15 VDD Cround Nets VSS Signal Nets	
-Pin Grouping	]
<ul> <li>Group1</li> <li>Group2</li> <li>Group3</li> <li>U12</li> <li>Y9</li> <li>V10</li> </ul>	
Assign Pin Groups Graphically	
■ <u>By</u> Grid 5 × 5 ~€	
<u>G</u> roup <u>U</u> nGroup	
<u>S</u> ave	lose

7. Once the pin groupings have been done for all circuits and nets, click the Save button to generate a MCP header file, for example mcp\_header\_by\_gui.ckt.

Save As								×
🕞 💮 – 길 « Ba	ise 🕨	SpeedXP I	<ul> <li>Samples</li> </ul>	► XtractIM	Single-Die_Sample_files	👻 🍫 See	arch Single-Die_Samp	ole_files 🔎
Organize 🔻 Ne	w fold	er					==	• 🔞
😥 My Site	*	Name		^	Date modified	Туре	Size	
🧫 Desktop					No items match your	search.		
🥽 Libraries					a foreigne en en construir e a construir 🥤 en astroise			
Documents								
🌙 Music	=							
Pictures	-							
Videos								
🖳 Computer								
🏭 Local Disk (C:)	)							
👝 Local Disk (D:)	) -							
File <u>n</u> ame:	mcp_	header_by_	_gui.ckt					-
Save as <u>t</u> ype:	MCP	circuit File	(*.ckt)					-
Alide Folders							Save Car	ncel

The .ckt file generated in the above steps can be used in the *Select User Grouped Pins in MCP Header* section.

## **Setup Extraction Frequency**

**1.** Select:

Setup > Extraction Frequency

A pop-up window opens.

- **2.** Update the data in the window.
- **3.** Change the default value. The default value is 30MHz.

Extraction Frequency X						
Extraction Frequency:	30	MHz	OK Cancel			

4. To ignore mutual resistance in RLGC circuits, select:

Setup > Export Without Mutual Resistance

The output circuit does not include the H-elements.



# LESSON TWO: SAVE WORK AREAS

#### **Layout File**

- **1.** Click on the Workspace.
- 2. Click on the Open Layout File icon (green) to open the project file.
- 3. Use Save As to save the layout file under a different name.



#### Workspace

- 1. Click on the Workspace. The Workspace pane opens.
- **2.** View the Workspace toolbar.
- In the toolbar click
   Save Workspace
- To save the Workspace under a different name, use: Save As

#### **Open Workspace**



# LESSON THREE: RUN THE SIMULATION

- 1. Click on the **Play** button **i** at the top of the window to start the extraction (simulation).
- 2. XtractIM only extracts RLCG for a net which has at least one pin at the Die side and at least one pin at the board side.
- **3.** At the beginning of the simulation, if some nets have Die-Board mis-match, a pop-up window opens. Select the next action.
  - **Continue** Continue the simulation
  - More Information Examine what nets are mis-matched
  - Stop Cancel the simulation

#### **Investigate Mis-matched Nets**

The More Information window lists all the mis-matched nets.

Investigate the mis-matched nets to see whether it is a special design or a defective design. Decide whether or not to proceed with the simulation.

Choose **Continue**, **Stop** or **More Information**. If 30 seconds pass and the user has not made a choice; then, by default, the simulation continues.

# **LESSON FOUR: FLY-WIREBOND PACKAGE MODEL EXTRACTION**

#### Introduction

For some wirebond package designs, there are wire connections only among die pads for power and ground nets. These die pads don't have connection to bond fingers or to package pins. Such kind of package is usually named as package with fly-wirebond or jump-wirebond inside. The fly-wirebond is typically used to reduce power IR drop noise.

In this lesson, it is introduced how to get a package model with fly-wirebonds in XtractIM.

#### Workflow

In general, the fly-wirebonds only happen on the same die in a package. It is only supported in singledie/single-package designs flow. The package type can be either BGA or lead-frame.

- 1. Package Setup:
  - a. Select Single Die.
  - b. Select Single BGA or Leadframe.
  - c. Select Wirebond.
- **2.** Simulation Setup:

The fly-wirebond is only supported in the pin-based mode.

a. Select simulation type: Pin-Based.



No specific setting is needed.

## Result

The fly-wirebonds are modeled separately by the tool.

The fly-wirebond model is wrapped into SPICE subcircuit model named

XtractIM - Flybond_3_Leadframe.ximx ·	- [Circuit Topology Result]
💠 File Window Help	
: 🗋 😂 🖵 🚽 💷 🕨 🔳 📘 🚥	
Workflow: XtractIM	Extractor Result
Model Extraction *	C49_52 CGN_49 CGN_52 1.91053e-014 RG49_52 CGN_49 CGN_52 1.28543e+008
Model Extraction	C49_52 CGN_49 CGN_52 1.51053e-014 RG49_52 CGN_49 CGN_53 1.45915e-014 RG49_53 CGN_49 CGN_53 1.45915e-014 RG49_53 CGN_49 CGN_53 1.45915e-014 C50_51 CGN_50 CGN_51 3.56452e-013 RG50_51 CGN_50 CGN_51 2.37823e+006 C50_52 CGN_50 CGN_52 7.09426e-014 RG50_52 CGN_50 CGN_53 2.22214e-014 RG50_53 CGN_50 CGN_53 3.6.74714e+007 C50_53 CGN_50 CGN_52 3.44473e-013 RG51_52 CGN_51 CGN_52 3.44473e-013 RG51_52 CGN_51 CGN_52 3.44473e-013 RG51_52 CGN_51 CGN_53 4.01902e+006 C51_53 CGN_51 CGN_53 4.01902e+006 C51_53 CGN_51 CGN_53 4.23178e-013 RG52_53 CGN_52 CGN_53 4.23178e-014 C52_53 CGN_52 CGN_54 9.14919e-014 Rfb1_1 U1_48 NFB_RL1_1 0.0858952 Lfb1_1 NFB_RL1_1 NFB_Mid_1 7.4464e-010 Rfb2_1 NFB_RL1_2 U1_24 7.4464e-010 Rfb1_2 U1_460 NFB_RL1_2 0.0827256 Lfb2_1 NFB_RL2_2 U1_47 7.14764e-010 Rfb1_2 U1_460 NFB_RL2_2 0.0827256 Lfb2_2 NFB_RL2_2 U1_47 7.14764e-010 Rfb1_2 L1_6D_1_1 Lfb1_2-0.00484792 KFB21_2 Lfb2_1 Lfb2_2 0.00484792 KFB21_2 Lfb2_1 NFB_Mid_1 NFB_MId_2 3.36799e-013 Cfb0_1 NFB_Mid_1 NFB_Mid_2 3.36799e-013 Cfb0_1 NFB_Mid_1 NFB_Mid_2 3.36799e-013 Cfb0_2 NFB_Mid_1 NFB_MId_2 3.36799e-013

#### jobname\_PinBaseSPICE.ckt as shown below.

# **VIEW EXPORT RESULTS**

The View / Exports Results options are displayed on the left side of the window.

- 1. Click on Summary.
- 2. View the maximum and minimum R, L, C, and other information in the Summary.
- 3. Click on SPICE Model. The SPICE Model name \*.ckt is loaded.
- **4.** View the SPICE Model file.

VVorktiow X	Extractor Result	
Manage Workspace 🛛 🔊	* 3 BGA1-U26 VSS	A 1
Load Workspace	* 3 BGA1-027 VSS	
Load a New/Different Layout	* 3 BGA1-V1 VSS	
Dackage Setun	- 3 BGAI-V2 VSS - 3 BGAI-V27 VSS	
Package Setup	* 3 BGA1-V28 VSS	
Package Type: Wirebond	3 BGA1-W2 VSS 3 BGA1-W26 VSS	
Circuits	* 3 BGA1-W27 VSS	
✓ Stackup	* 3 BGA1-W3 VSS * 3 BGA1-Y1 VSS	
Solder Ball	* 3 BGA1-Y2 VSS	
✓ Nets	* 3 BGA1-Y26 VSS	
Simulation Setup 🔗	* 3 BGA1-Y28 VSS	
Module: IBIS/RLGC	* 3 BGA1-Y3 VSS	
Simulation Type: PinBased	* BGA1-P14	
✓ Set Reference Net	* PD1 U1 112 D-N1 0 110422	
View/Export Results	VD1 DrN1 DVn1 0	
	Hd1_2 DVn1 CCVSr1_2 CCVS VD2 0.0390498	
Summary	Hd 1_3 CCVSr1_2 CCVSr1_3 CCVS VD3 0.037191 Hd 1_4 CCVSr1_3 CCVSr1_4 CCVS VD4 0.0364626	
SPICE Model	Hd1_5 CCVSr1_4 CCVSr1_5 CCVS VD5 0.0360892	
	Hd1_6 CCVSr1_5 CCVSr1_6 CCVS VD6 0.0359549	
	Hd1_8 CCVSr1_7 CCVSr1_8 CCVS VD8 0.0358705	
	Hd1_9 CCVSr1_8 CCVSr1_9 CCVS VD9 0.0357969	
	Hd1_11 CCVSr1_9 CCVSr1_10 CCVS VD10 0.0368331	
	Hd1_12 CCVSr1_11 CCVSr1_12 CCVS VD12 0.0356264	
	Hd1_13 CCVSr1_12 CCVSr1_13 CCVS VD13 0.0357708	
	Hd1_15 CCVSr1_14 CCVSr1_15 CCVS VD14 0.0358785	
	Hd1_16 CCVSr1_15 CCVSr1_16 CCVS VD16 0.0358522	
	Hd1_18 CCVSr1_16 CCVSr1_17 CCVS VD17 0.0369935 Hd1_18 CCVSr1_17 CCVSr1_18 CCVS VD18 0.035952	
	Hd1_19 CCVSr1_18 CCVSr1_19 CCVS VD19 0.0379053	
	Hd1_20 CCVSr1_19 CCVSr1_20 CCVS VD20 0.0408726	
	Hu1_21 CCV3H_20 CCV3H_21 CCV3 VD21 0.0362641	✓
	<	>
	Mouse(mm): X: -23.750, Y: 10.885	Computing completed

#### **Optimized Broadband Module**

A typical workflow in Iteration Mode is the same as RLGC Module Pin-based Extraction. Additional steps in the Simulation Setup include:

1. Click:

Module > Optimized Broadband

2. Click:

Workspace > Frequency Range of Extraction

A new Edit pane opens at the bottom of the window.

3. Input the highest frequency for simulation.



# **Circuit Topology**

The circuit topology is a generalized T-model with series terms. No multi-sections circuit model is used as those in a net-based Broadband module.

Extraction frequency points for S-parameters are limited to a few points. Frequency band goes up to a few hundred MHz.



# **IBIS/RLGC Module: Simulation of Leadframe Package**

This chapter takes you through the steps to use the XtractIM tool in the simulation of Leadframe package.

# **PREPARE FOR SIMULATION**

Collect this information before you begin the simulation.

- Make sure the Leadframe file is in DXF or SPD format
- Have the Stackup information ready
- Have the outer lead width, length, height and conductivity ready

If the leadframe file is in DXF format, make note of:

- Ball pad parameters
- Die pads
- Layers you wish to import
- Leadframe conductor Wirebonds

# **LESSON ONE : SIMULATION SETUP**

- **1.** Launch XtractIM.
- 2. Click Open to open an existing workspace.
- **3.** Click:

Load an existing layout

4. Click OK.

The Attach DXF File window opens.

- 5. Select the desired file. The example shows only one file selected: Lead1.dxf.
- 6. Click Open.

Attach DXF	<sup>-</sup> file				? >	<
Look in:	違 LeadFrame		<b>•</b> (	G 🦻 🖻 🛄	•	
My Recent Documents	🖬 Lead1.dxf					
Desktop						
My Documents						
My Computer						
	File name:	Lead1.dxf		-	<u>O</u> pen	]
My Network	Files of type:	DXF File (*.dxf)		-	Cancel	].

- 7. Launch XtractIM.
- 8. Click New to create a new workspace;

or select:

Workspace -> New

 To load the Package Structure, select: Load a New / Different Layout **10.** Click **OK** to load a **DXF file**. The Sigrity Speed Editor is launched.





11. Translate a package file from DXF to SPD format; it is automatically loaded into XtractIM

#### **Package Type**

XtractIM classifies the leadframe family package into three kinds of packages:

- No Outer Lead No board pin has outer lead. Typical package is QFN
  - **Partial Outer Lead** Some of the board pins have outer lead
- With Outer Lead Every board pin has outer lead. Typical package is QFP
- 1. Select Package Type.

The default is Single-Die, Single-BGA, Wirebond Package.

- 2. Click Leadframe.
- 3. Select one of:

•

- No Outer Lead
- Partial Outer Lead
- With Outer Lead
- 4. Click **OK** to save your selection.

5. Click Cancel if you want to change your selection, start over, or cancel your session.



6. Click on the Single\$1 layer. The Inner Lead Converter locates Single\$1.

Layer Selection $-\Box \times$
🥗 Signal\$WB
🍉 Signal\$1
View Only Active Layer
Display Geometry Objects By
Net Color      Layer Color

### **Shape to Trace Conversion**

- 1. Click on Inner Lead Converter to convert narrow shapes into traces. The Inner Lead Converter window opens.
- **2.** Choose:

Manually convert selected shapes to traces



3. Use the toolbar icon to select shapes in the Layer View.



4. Click Convert. All narrow shapes are converted into Traces.



#### NOTE!

A No Outer Lead Package generally does not need this converter.

#### **Setup Circuits and Stackup**

- 1. Click on **Circuits** in the Workflow pane to setup circuit data for the leadframe package. A new pane opens in the left side of the workspace.
- **2.** Right-click on the desired circuits.
- **3.** Select it as a **Die circuit**.
- 4. Click Next.
- 5. Right-click on another desired circuit. Select it as a **Board circuit**.
- 6. Click Finish to finish the circuits setup.
- 7. Click on Stackup. The Stackup window opens.
- 8. Right-click on the Signal\$ layer. A pop-up window opens.
- 9. Select:

Insert Under

A second pop-up menu opens.

#### **Outer Lead Setup**

The following steps are performed for **Outer Lead** only.

- To insert a Leadframe layer, select Leadframe Medium Layer, Signal01 Layer, and Medium01 Layer
- 2. To insert an empty signal layer, select **Package**.

Stack	up								_	D X
Layer Icon	Layer Name		Thickness(mm)	Conductivity(S/m)	Color	Trace Width(mm)	Shape Name	Permittivity	Loss Tangent	From File
	Signal\$WB		1.0000e-003	5.9561e+007		1.0000e-001				
	Medium\$Dielect	tric0	8.8000e-002					3.3000	0.0000	
	Signal\$1		3.3000e-002	5.9561e+007		1.0000e-001	Shape\$1			
		Inser	t Above 🕨							
		Inser	t Under 🖻	Signal Layer						
		Delet	e	Medium Layer					_	
	4	-	_	Plane Laver						
									_	_
				Leadframe Mediu	m Lay	er, Signal01 Lay	er, and Mediur	n01 Layer 🕨	Package	
<				111						>
Total Thick	ness: 1.22006	e-001 mm						Unit:	mm 🔻 View	Material
Leadfram	e Layer		Right-click on a	dielectric(or signal) la	ayer to	insert a leadframe l	ayer.	rt	ок	Cancel

- 3. Insert a medium layer standing for a PCB medium layer.
- **4.** All layers are inserted into **Signal\$1**. The added signal layer is located at the end of the lead-frame.
- 5. Click OK to close the Stackup window.

Stack	up							_	$\square X$
Laver Icon	Laver Name	Thickness(mm)	Conductivity(S/m)	Color	Trace Width(mm)	Shape Name	Permittivity	Loss Tangent	From File
	Signal\$WB	1.0000e-003	5.9561e+007		1.0000e-001				
	Medium\$Dielectric0	8.8000e-002					3.3000	0.0000	
	Signal\$1	3.3000e-002	5.9561e+007		1.0000e-001	Shape\$1			
111	MediumLeadframe01	5.0000e-001					1.0000	0.0000	
	Signal01	1.0000e-003	5.8000e+007		1.0000e-001				
	Medium01	5.0000e-002					4.0000	0.0000	
<			111						>
Total Thickness: 6.7300e-001 mm View Material									
✓ Leadframe Layer       Right-click on a dielectric(or signal) layer to insert a leadframe layer.       Import       OK       Cancel									

#### Leadframe Data for the Leadframe Package

- 1. Click on Leadframe in the Workflow pane to setup the data for the Leadframe package. A new pane opens up in the bottom portion of the windows.
- **2.** Select:

Package Setup -> Leadframe

- 3. Input the settings for Leadframe (Standard Setup).
  - **Conductivity** Conductivity of the outer leads
  - **D** Total horizontal length
  - **H** Heights of the leads
  - Hs Heights of the lower part
  - LI Length of lower leads
  - Lu Length of upper leads
  - Medium PCB medium thickness
  - **RI** Radius of lower arc
  - **Ru** Radius of upper arc
  - **T** Thickness of the leads
  - WI Width of lower leads
  - Wu Width of upper leads

## **Standard Setup Example**

Package Setup -> Lead															
O Simplified Setup															
Layer Name	Circuit Name	D (mm)	Lu (mm)	Wu (mm)	Ru (mm)	Ll (mm)	WI (mm)	RI (mm)	T (mm)	H (mm)	Hs (mm)	Material	Cor (S/	nductivity /m)	Medium Thickness (mm)
Mediu	Package	1	0.5	0.24	0	0.5	0.24	0	0.033	0.5	0		5.8	3e7	0.05
												aluminum			
												copper			
												gold			
												silver			
												Solder60			
												Solder63			

# Simplified Setup Example

Package Setup -> Lead												
Simplified Setup     Standard Setup												
Layer Name	Circuit Name	D (mm)	Lu (mm)	W (mm)	LI (mm)	T (mm)	H (mm)	Material		Conductivity (S/m)	Medium Thickness (mm)	
Mediu	Package	1	0.5	0.24	0.5	0.033	0.5		•	5.8e7	0.05	
								aluminum				
								copper				
								gold				
								silver				
								Solder60				
								Solder63				
-							1					

#### Standard Lead Plot Example



Simplified Lead Plot Example



- 4. Click OK to save your entries.
- 5. Click Cancel if you do not want to save your changes. You can start over.

#### **Setup Nets**

- 1. Click on Nets in the workflow window. The Net Manager window opens.
- 2. Choose any desired nets for RLC extraction.
- Move the signal net into and out of PowerNets and Ground Nets, as needed.
   At least one Ground Net must be selected to act as a reference ground net.
- 4. Choose only the desired Ground Net as the reference ground net.

#### **Extraction Frequency**

1. To change the extraction frequency, select:

Setup -> Frequency of Extraction

A pop-up window opens.

- 2. Update the data in the pop-up window.
- 3. Use the Extraction Frequency window to change the default value. The default value is 30MHz.

#### **Threshold for Exporting Mutual Terms**

- 1. Use the XtractIM options to reduce the size of the output circuit during the export stage. XtractIM captures all the coupling during the extraction stage.
- 2. Open:

Setup > Threshold for Exporting Coupling Terms

A pop-up window opens.

3. Choose the number of strongest coupling neighbors to be kept in the circuit model.

The default on number of strongest coupling neighbors is 10; which means only outputting the 10 strongest neighbors (including self).

**4.** Ignore mutual capacitance or inductance if the ratio of mutual terms over self term is less than a percentage.

The default percentage threshold for ignoring mutual capacitance and inductance is 0.005.

If the mutual capacitance or inductance is less than the 0.5% of the minimum of the two selfcapacitances / inductances, then it does not output the mutual capacitance / inductance.

# LESSON TWO: SAVE WORK AREAS

#### **Layout File**

- **1.** Click on the workspace.
- 2. Click on the Open Layout File icon (green) to open the project file.
- 3. Click on the Save Layout File icon (green) to save the project file.
- To save the layout file under a different name, select:
   Save as

NOTE!

Saving the workspace automatically saves the .spd file.Saving the.spd file does not automatically saves the workspace.

#### Workspace

- 1. Click on the Workspace. The workspace opens.
- 2. Click on the Save Workspace icon (yellow) in the toolbar.
- 3. Use Save as to save the Workspace under a different name.

#### LESSON THREE: RUN THE SIMULATION

- 1. Click on the **Play** button **l** at the top of the window to start the extraction (simulation).
- 2. XtractIM only extracts RLCG for a net which has at least one pin at the Die-side and at least one pin at the board side.
- **3.** At the beginning of the simulation, if some nets have Die-Board mis-match, a pop-up window opens.
- **4.** Select the next action.
  - **Continue** Continue the simulation
  - More Information Examine what nets are mis-matched
  - **Stop** Cancel the simulation

#### **Investigate Mis-matched Nets**

The More Information window lists all the mis-matched nets.

- 1. Investigate the mis-matched nets to see whether it is a special design or a defective design.
- 2. Decide whether or not to proceed with the simulation.
- 3. Choose Continue, Stop or More Information.

If 30 seconds pass and the user has not made a choice; then, by default, the simulation continues.

# **LESSON FOUR : OBSERVE AND SAVE SIMULATION RESULTS**

XtractIM performs calculations for each net. The calculations include:

- Conductance
- Mutual capacitance with other nets
- Mutual loop inductance
- Resistance
- Self capacitance
- Self loop inductance

The inductance and capacitance are matrices.

In the Inductance Matrix, the Diagonal Element is the Self Inductance of each net.

The off-diagonal elements are mutual Inductance.

There are two concepts for capacitance matrix.

- Maxwell Capacitance Matrix
- SPICE Capacitance Matrix

Maxwell Capacitance Matrix — Each diagonal element is the loading capacitance

#### Example

Capacitance-to-ground when other nets are grounded. This represents the worst-case capacitive loading. Off-diagonal elements are mutual capacitance with negative values.

**SPICE Capacitance Matrix** — Each diagonal element is capacitance-to-ground. Off-diagonal elements are mutual capacitance with positive values.

View the relationship between Maxwell capacitance and SPICE capacitance matrix.

#### R, L and C

- 1. View Resistance for each net.
- 2. View Self-inductance for each net.
- 3. View Self-capacitance for each net.

## **Mutual Terms**

- 1. View Mutual Terms.
- 2. View Mutual Inductance.
- 3. View SPICE Mutual Capacitance.

Usually conductance is very low, so there is no view for conductance.

#### **Summary of the Extracted Results**

- 1. Click on Summary.
- 2. View the data for R, L and C.
  - Extraction Frequency
  - Full RLC Matrix
  - Maximum / Minimum R, L, C
  - Nets Extracted
  - Package Name
- **3.** Reorder the list if you wish.
- 4. Click on R/L/C full matrix. The matrix is saved on hard disk in .csv format.

#### **SPICE Model Files Saved**

Upon completing the simulation, both model files are saved in the same directory as the .spd file.

The total number of elements (R, L, M, C and G where M is the mutual inductance) in the circuit is displayed at the bottom of the window.

The SPICE Model is saved as a SPICE sub-circuit with the extension .ckt.

The SPICE model is a T-circuit.

#### **IBIS Model Saved**

The IBIS Model is saved as an IBIS package model. The saved model has the extension .pkg.

#### **Pin Model: IBIS Format**

An .ibs format file is saved.

The saved file includes each single net R, L and C.

All power nets and ground nets are lumped together.

#### **Pin Model: Excel Format**

- 1. Click on Pin Model: Excel format in the SPICE / IBIS Model window.
- 2. A .csv file is loaded. The .csv file includes information for each Signal Net.
  - Net Length
  - Net Name
  - Pin Name
  - Self-C
  - Self-L
  - Self-R
  - Time Delay

Self-C is the Maxwell Capacitance.

The information for Power Nets does not include Net Length.

#### **DC Resistance**

1. Click:

DC Resistance

2. View the .csv file. DC Resistance is given for each of the Power, Ground and Signal Nets. A .csv file is saved on hard disk.

#### **RLC Distributions**

1. Click:

**RLC Distributions** 

- View the full matrix value of R, L and C.
   RLC Distributions offers eight kinds of views.
- **3.** View the RLC distributions.

#### Segment RLC

1. Click on Segment RLC in the workflow pane under:

View / Export Results

For each signal net, XtractIM outputs the segment RLC of each metal layer.

- 2. View the Segment RLC values. Note the three bars for Resistance, Inductance and Capacitance across the bottom of the screen.
- 3. Click on the **Resistance** bar. The Resistance values are displayed.
- 4. Click on the Inductance bar. The Inductance values are displayed.
- 5. Click on the Capacitance bar. The Capacitance values are displayed.

#### **Save Simulation Results**

**1.** In the Workflow pane click:

#### Save Results

The Save Extractor Result window appears.

- **2.** Enter a file name.
- **3.** Click on **Save**. The results are saved in a binary file. The file is named: result\_spd\_file\_name.xim
- 4. Click on Cancel if you do not want to save the results in the file name you entered.

#### **Simulation Output Files**

The result and result\*.xim files save all the output data including:

- Package Model Files.
- SPICE Circuit
- Summary

The SPICE file and two IBIS files are automatically saved by the tool.

The result file is created only when the user chooses to save all the output data.

View the output files on hard disk.

- One **IBIS Package Model File** The \*.pkg file includes both L and C coupling elements
- One **Pin Model in Excel Format** The \*.csv file includes each signal net length, self-R, self-L, self-C, and time delay. No coupling elements are included
- One **Pin Model in IBIS Format** The\*.ibs file includes each signal net self-R, self-L, and self-C. No coupling element is included
- One Summary Content in Excel Format The \*.csv file includes the RLC Full Matrix
- Two SPICE Circuit Files The Pi-model is named \*.ckt; the T-model is named \*\_t.ckt
- Three Segment RLC in Excel Format This segment includes the RLC of each metal layer with \*.csv files

#### **Load in Saved Results**

- 1. Select Load Results in the workflow pane to load the saved results. The main window shows the selected result.
- 2. View present results or the loaded results.
  - Loaded Curves Shows the loaded results
  - **Present Curves** Present extracted results
- **3.** To unload a loaded result, click on the toolbar icon:

Unload Extractor Result

#### **LESSON FIVE: BATCH MODE SIMULATION**

**1.** To run a simulation in batch mode, select:

Start > Run

- 2. Change to the directory where the XtractIM.exe file is located.
- **3.** Upon completing the simulation, all output files are automatically saved in the same directory as the \*.spd file.
  - \*.ckt files
  - \*.ibs files
  - \*.pkg files
  - .csv files

# Chapter

# 8

# **Electrical Performance Assessment**

This chapter takes you through the steps to use the XtractIM tool to analyze the electrical performance of the Power / Ground / Signal distribution system. XtractIM checks the Power / Ground distribution system by checking:

- Power-ground Net Pair: Inductance, Capacitance and Broadband Impedance
- Per pin Resistance and Inductance
- Current Density: Via Current, Plane Current Density, Voltage Distribution (PowerDC license required)

XtractIM checks the Signal Distribution System by checking:

- Wirebond / Trace Layout: Impedance and Coupling
- Net Couplings: Mutual LC and Near-ended Crosstalk
- Insertion and Return Loss

XtractIM can also create Html report including all features in electrical performance assessment:

- Html report can be manually created after the simulation is completed
- Html report can be automatically created upon the simulation's completion

# **LESSON ONE: SIMULATION SETUP**

- 1. Launch XtractIM.
- 2. Select:

Mode > Elec. Perf. Assessment (EPA)

The Electrical Performance Assessment Workflow appears.

(೫ ⊕ ⊕ ₽ ₪ 🗒												
Workflow: XtractIM	x		-60 -5	040	-30 -2	0	 10 20	 40	50		ayer Selection	;
Electrical Performance Assessm	≈	1							2		Signal02	
Manage Workspace		8									Plane02	
Load Workspace Load a New/Different Layout Package Setup		40 30									Signal01	
Package Type: Wirebond Circuits Stackup Solder Ball Vets	-	20 10 10 1-10							=		7	
Setup for Power-Ground Analysis Setup for Signal Analysis Setup for Current Checking View/Export Results		1-20 -30 -40									View Only Active Layer  Display Geometry Objects By  Net Color O Layer Color	-
Save Result Load Result	-	-50							*	L	ayer Selection Net Manager	
Mouse(mn	n): X	-68.	372, Y:	-17.519	)				🔴 Rea	dy		

#### **Setup Steps**

Follow these steps to perform a Type Workflow in Interactive Mode.

- 1. Load an existing file (.xml file), if any.
- 2. Open a layout file (.spd file).
- **3.** Select a package type.
- 4. Setup the circuits.
- 5. Select or deselect Die-circuit and Board circuit.
- 6. Setup the Stackup.
- 7. Set parameters for the Bump or Solderball Medium layer.
- 8. Set the Bump data if it is a Flip-chip package.
- **9.** Set the Solderball data.
- **10.** Select the nets for simulation.
- **11.** Simulation Setup.
- 12. Select automatically generate and save report.
- **13.** Save the Workspace and Layout file.

Except for Step 11 and 12, all steps are exactly the same as the steps described in *IBIS/RLGC Module: Net-Based Simulation Single-Die Single-BGA Packages*.

#### **Setup for Power/Ground Analysis**

1. Select:

Simulation Setup > Setup for Power / Ground Analysis

Simulation Setup -> Simulation Type	
Power-Ground Analysis	Per Pin Properties     Grouped Pin Properties
Per Net-Pair Properties	✓ DiePad-to-BGA DC Resistance ✓ Self- and Total-loop Inductance
✓ Inductance and Capacitance	○ From Die-side ○ From Board-side
Broadband Impedance (Single Die-Single BGA without Decaps)     Frequency up to     2.00     GHz	Advanced per-pin RL setup: Advanced Use Advanced Setup for Simulation Nets to Be Assessed:
	Net Net type A Inductance of a pin is obtained from
	VDD_1 PowerNets the loop of this pin and the pins of all other enabled power and ground pets
	VDD_2 PowerNets as current return path.
	VDD_3 PowerNets
	VDD_4 PowerNets Resistance of a pin is the DC-resistance
	VDDcore PowerNets Tom the pin at die/board-side to the
	✓ III board/die-side.
OK Cancel	

- **2.** Select any or all of the following:
  - (Power to Ground) Inductances and Capacitances
  - **Broadband Impedance (Single Die-Single BGA without Decaps)** Edit the highest frequency
  - Bump-to-BGA DC Resistance Select Nets to be assessed
  - Self- and Total-loop Inductance Select Nets to be assessed
- **3.** Click **OK** to accept the selections.

#### **Grouped Pin Property**

If Grouped Pin Property is selected, user can choose n\* n groups.

Per Pin Properties       Image: Comparison of the properties         DiePad-to-BGA DC Resistance       Self- and Total-loop Inductance         From Die-side       From Board-side       Both									
Advanced per-pin RL setup:     Advanced       Nets to Be Assessed:     Pin Groups:       5     X									
Net	Net type	Â	Inductance of grouped pins is obtained from the loop of these grouped pins and the pins of all other enabled power and ground nets as current return path.						
VDD_1	PowerNets								
VDD_2	PowerNets	=							
VDD_3	PowerNets								
VDD_4	PowerNets		Resistance of grouped pins is the						
VDDcore	PowerNets	-	DC-resistance from the lumped grouped						
•	III 🕨		pins of the same net at board/die-side.						





In each of the cells, instead of per pin assessment, all pins of the under assessment net will be lumped and assessed as one. The return paths are kept the same as per-pin properties assessment.

#### **Setup for Signal Analysis**

1. Select

Simulation Setup > Setup for Signal Analysis

Simulation Setup -> Simulation Type							
Signal Analysis							
Trace Layout Checking							
Impedance, Continuity and Net-Length							
Coupling Coefficient							
Net Coupling (Single Die-Single BGA without Decaps)							
Mutual L&C, Total NEXT							
Insertion and Return Loss (Single Die-Single BGA without Decaps)							
Frequency up to 2.00 GHz							
OK Cancel							

**2.** Select any or all of the following:

#### **Trace Layout Checking**

Impedance, Continuity and Net-Length: Before running coupling and insertion and return loss analysis, it is helpful to run this check first to generate a length report for filtering out

Signal Net Name 💫 🛆	Net Length (mm)	
FCHIP_A1	2785.115	
FCHIP_A2	3663.313	
FCHIP_A3	4550.800	
FCHIP_A6	3442.505	
FCHIP_A7	2442.132	
FCHIP_A12	2484.810	
FCHIP_A13	3407.297	
FCHIP_A16	4623.287	
FCHIP_A17	3678.313	
FCHIP_A18	2785.115	
FCHIP_B3	2865.140	
FCHIP_B4	3758.338	
FCHIP_B5	4659.820	
FCHIP_B6	3613.363	
FCHIP_B13	3671.353	
FCHIP_B14	4651.536	
FCHIP_B15	3758.338	

the worse nets for insertion and returen loss analysis, which is usually completed in seconds.

**Coupling Coefficient** 

#### Net Couplings (Single Die-Single BGA without Decaps)

Mutual L&C, Total NEXT

#### Insertion and Return Loss (Single Die-Single BGA without Decaps)

Frequency up to GHz

Insert the highest frequency in the GHz box.

- **3.** Click **OK** to accept the selections.
- 4. Select

Simulation Setup > Setup for Current Checking



• Check DC Current Density (Single Die-Single BGA without Decaps) — Every VRM voltage is set as 1V internally

5. Set the Sink Current. Sink current is set for each power net and its reference ground net. The simulation will be based on equal voltage at the Sink Side.



6. Click **OK** to accept the selections.

**Select Automatically Generate and Save Report** 

 To automatically generate and save report upon simulation's completion, select Tools > Options > Edit Options... > Simulation (Basic) > General
Options		×
File       Image:         General       File Manager         Save Options       Hotkeys         Layout       Image:         Grid and Unit       View         Processing       Trace         Error Checking       Image:         Image:       Image:         Jbalayout View       Image:         Display       Image:         Quality       Image:         Simulation (Basic)       Image:         General       Image:         Net and Coupling       Special Void         Output SPICE Circuit       Report         Simulation (Advanced)       Image:         Electric Models       Mesh         Nets and Shapes       Nets and Shapes	Change the 'General' options in XtractIM     Automatically save the result when simulation is complete   Automatically output enforced passive results     Automatically generate and save report at the end of simulation   Simulation complete notification   Send mail to:   Outgoing mail server (SMTP,   Logon Information   User Name:   Password:     Multiple CPU usage   Maximum number of CPU to use in the   4 (Recomment)   Simulation Process Priority	
	Default Apply OK	Cancel

- 2. Select the Automatically generate and save report at the end of simulation option.
- 3. Click OK.

# Save Workspace

**1.** To save the workspace, click:

Workspace > Save

or

**2.** Click to save both workspace and SPD file.

# **LESSON TWO: RUN AND SIMULATION**

Click on the **Play** button **i** at the top of window to start the extraction.

# **LESSON THREE: OBSERVE AND SAVE SIMULATION RESULTS**

The results are displayed after the simulation is finished.

ower-Ground Analysis	0
Per Net-Pair Properties	•
Inductance and Capacitance	
Broadband Impedance	
Per Pin Properties	•
R&L Histogram	
R&L by Layer	
R&L Distributions	
R&L Per Pin	
R&L 2D View	
ignal Analysis	•
Trace Layout Checking	•
Net Length Summary	
Net Impedance Summary	
Net Coupling Summary	
Impedance Plot (collapsed)	
Impedance Plot (expanded)	
Impedance Table	
Impedance by Layer	
Coupling Coefficient Plot (coll	apsed)
Coupling Coefficient Plot (exp	anded
Coupling Coefficient Table	
Coupling Coefficient by Layer	
Net Coupling	•
Single-ended Based	•
Mutual Inductance and Cap	acitan
Total NEXT Histogram	
Diffpair and Single-ended	•
	acitan
Mutual Inductance and Cap	autan
Mutual Inductance and Cap Total NEXT Histogram	acitari
Mutual Inductance and Cap Total NEXT Histogram Insertion and Return Loss	
Mutual Inductance and Cap Total NEXT Histogram Insertion and Return Loss Insertion Loss	
Mutual Inductance and Cap Total NEXT Histogram Insertion and Return Loss Insertion Loss Return Loss	
Mutual Inductance and Cap Total NEXT Histogram Insertion and Return Loss Insertion Loss Return Loss Surrent Checking	<u> </u>
Mutual Inductance and Cap Total NEXT Histogram Insertion and Return Loss Insertion Loss Return Loss Unrent Checking Via Counts	
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Mutual Inductance and Cap Total NEXT Histogram Insertion and Return Loss Return Loss Acturn Loss Via Counts Via Counts Via Current Histogram Via Current by Layer	
Mutual Inductance and Cap Total NEXT Histogram Insertion and Return Loss Return Loss Acturn Loss Via Counts Via Counts Via Current Histogram Via Current by Layer Via Current Table	
Mutual Inductance and Cap Total NEXT Histogram Insertion Loss Return Loss Active Loss Active Checking Via Counts Via Current Histogram Via Current by Layer Via Current Table Voltage Distribution by Layer	

### **Power-Ground Analysis**

#### **Per Net-Pair Property**

The Workspace lists the options to display all results. Click on the desired option.

### Per Net-Pair Properties

Inductance and Capacitance Broadband Impedance

1. Click:

Inductance and Capacitance

A table is displayed.

Power Net	Ref Ground Net	L(nH)	C(pF)	Ground Net	L(nH)	$ \Delta $
VDD_1	VSS	0.454952	43.3595	VSS	0.454952	
VDD_2	VSS	0.458492	43.3065	VSScore	0.590788	
VDD_3	VSS	0.451241	43.4001			
VDD_4	VSS	0.455836	43.2714			

- **Power Net** Power Net Names
- Ref Ground Net Reference Ground Net Name of smallest loop Inductance.
- L(nH) Loop Inductance referring to the Ref Ground Net.
- C(pF) Capacitance referring to the Ref Ground Net.
- Ground Net Ground Net Name. Displays when Net Name is clicked.
- L(nH) Inductance when the Power Net uses each Ground Net as the current return path. Displays when Net Name is clicked.
- 2. Click:

**Broadband Impedance** 

**Short** and **Open Impedance** (Z-parameter) vs. **Frequency** (1MHz-Fmax) are shown in the same plot. The **Observation Ports** are at Die Side. Each Port is defined as a Power Net refers to its Reference Ground Net.

**Definition of Short and Open** 

- **Short** Short each Power Net and its Reference Net at the Board Side.
- **Open** Keep its Power Net and its reference Net open at the Board Side.





Enable all curves of one port, both the self-impedance and transfer impedance are shown.

# **Per Pin Property**

The Workspace lists the options to display all results. Click on the desired option.

# **Per Pin Properties**

R&L Histogram R&L by Layer R&L Distributions R&L Per Pin R&L 2D View

**R&L Histogram** 

#### All pin RL values are plotted from the smallest (left) to the larget.



# R&L by Layer

Inductance or resistance values are super-displayed in the layout.



### **R&L** Distributions

	_ @ ×
💼 🖾 🍬 • 🔍 🖾 🛄 🗔 🖻	9 🖸 🔣 Extractor Result 💌 🛍 👘 👘 😵 🛠 🍄 🍄 꾿
Resistance	
Net	
VCC	

- Use the **Rotation** icon to choose the preferred view.
- To save a file to any preferred name, select the name and click Save.

R&L Per Pin

Net	Pin NodeName	Self L(nH)	Total L(nH)	R(mOhm)	Induced Voltage(V)	Current(A)
FCHIP	Node03060!!A2::VDD	1.872	2.332	6.151	1.466	1.000
VDD	Node03069!!A11::VDD	1.845	2.315	6.149	1.454	1.000
VDD_15	Node03097!!D3::VDD	1.099	1.558	3.289	0.979	1.000
VSS	Node03104!!D10::VDD	1.071	1.534	2.966	0.964	1.000
BGA	Node03112!!E6::VDD	0.694	0.975	2.508	0.613	1.000
VDD	Node03114!!E8::VDD	0.817	1.301	14.615	0.818	1.000
VDD_15	Node03124!!F6::VDD	0.700	1.024	14.178	0.643	1.000
VSS	Node03126!!F8::VDD	0.784	1.227	14.229	0.771	1.000
	Node03136!!G6::VDD	0.761	1.212	14.036	0.762	1.000
	Node03138!!G8::VDD	0.728	1.078	14.593	0.677	1.000
	Node03148!!H6::VDD	0.813	1.238	14.529	0.778	1.000
	Node03150!!H8::VDD	0.792	1.176	14.647	0.739	1.000
	Node03157!!J3::VDD	1.053	2.196	3.233	1.380	1.000
	Node03164!!J10::VDD	0.961	1.968	2.931	1.237	1.000
	Node03170!!K4::VDD	1.288	2.423	34.876	1.522	1.000
	Node03175!!K9::VDD	1.190	2.190	34.574	1.376	1.000
	Node03192!!M2::VDD	1.993	2.362	6.120	1.484	1.000
	Node03201!!M11::VDD	1.634	2.040	6.132	1.282	1.000

- Column 1 Net names
- Column 2 Pin node name of the selected net
- Columns 3 and 4 DC Resistance and Loop Inductance of each pin
- Columns 5 and 6 Induced Voltage and Current of each pin

These two columns provide a current-weighted per-pin power/ground RL assessment before running a system-level PI/SI analysis if you have a current vector.

- Induced Voltage is calculated by dv=L\*(di/dt)
- The induced Current is calculated by [L\_matrix]<sub>N\*N</sub>\*[Current]

N is pin number for a net. By default, all the pins have the same current value 1A.

1. Click the E button in the Current column of a pin, and input the pin Current value.

The Induced Voltage result will be updated instantly.

Induced Voltage(V)	Current(A)
2.054	1.500 E
1.527	1.000
0.995	1.000
0.972	1.000
0.620	1.000
0.834	1.000
0.645	1.000
0.777	1.000
0.763	1.000
0.679	1.000
0.779	1.000
0.740	1.000
1.383	1.000
1.238	1.000
1.526	1.000
1.378	1.000
1.485	1.000
1.282	1.000

2. Click:

#### Pin Node Name

- 3. Sort the list in ascending or descending order.
- 4. Click:

R(mOhm) or L(nH)

5. Sort the items in ascending or descending order. The results are displayed in a table.

R&L 2D View



- 1. Select from the drop-down menu to see **Resistance** or **Inductance**.
- 2. Move the cursor across the Layout window.
- 3. Pause the cursor on a point of interest. The display shows:
  - Node Name
  - X-Y coordinates
  - Actual number

# **Signal Distribution System Checking**

Trace coupling is defined with Near-ended Crosstalk as a victim.



Aggressor: Z10, L11, C11

Victim: Z20, L22, C22

$$\begin{split} & K = \frac{V_{y}}{4} \left( C_{12} Z_{20} + \frac{L_{12}}{Z_{10}} \right) \\ & Where, \quad \frac{2}{V_{y}} = \frac{1}{V_{y1}} + \frac{1}{V_{y2}} \\ & V_{y1} = \frac{1}{\sqrt{L_{11}C_{11}}} \quad V_{y2} = \frac{1}{\sqrt{L_{22}C_{22}}} \\ & Z_{10} = \sqrt{\frac{L_{11}}{C_{11}}} \quad Z_{20} = \sqrt{\frac{L_{22}}{C_{22}}} \end{split}$$

**Definitions** 

К	The near-end coupling coefficient from aggressor Net on victim Net.
C <sub>11</sub> / C <sub>22</sub>	The loading capacitance per unit length of Signal Net to its Reference Net.
L <sub>11</sub> / L <sub>22</sub>	The self-inductance per unit length of Signal Net.
C <sub>12</sub>	The mutual capacitance per unit length between aggressor and victim Net.
L <sub>12</sub>	The mutual inductance per unit length between aggressor and victim Net.
V <sub>p1</sub> / V <sub>p2</sub>	The signal velocity propagates on Signal Net.
Z <sub>10</sub> / Z <sub>20</sub>	The characteristic impedance of Signal Traces.

# **Trace / Wirebond Layout Checking**

The Workspace lists all results to be displayed. The first three summaries are for all enabled Signal

Nets in the package.

The rest of the summaries are for a specific path from one component to another component. For the Single-die Single-BGA package, the path is from Die to Board.

Signal Analysis 📀	
Trace Layout Checking 📀	
Net Length Summary	
Net Impedance Summary	
Net Coupling Summary	
Impedance Plot (collapsed)	
Impedance Plot (expanded)	
Impedance Table	
Impedance by Layer	
Coupling Coefficient Plot (collapsed)	
Coupling Coefficient Plot (expanded)	
Coupling Coefficient Table	
Coupling Coefficient by Layer	

1. Click

Net Length Summary.

A summary table for enabled signal nets is displayed.

Signal Net Name 💫 🛆	Net Length (mm)
FCHIP_A1	2785.115
FCHIP_A2	3663.313
FCHIP_A3	4550.800
FCHIP_A6	3442.505
FCHIP_A7	2442.132
FCHIP_A12	2484.810
FCHIP_A13	3407.297
FCHIP_A16	4623.287
FCHIP_A17	3678.313
FCHIP_A18	2785.115
FCHIP_B3	2865.140
FCHIP_B4	3758.338
FCHIP_B5	4659.820
FCHIP_B6	3613.363
FCHIP_B13	3671.353
FCHIP_B14	4651.536
FCHIP_B15	3758.338
FCHIP_B16	2865.140
FCHIP_C2	3758.338
FCHIP_C17	3783.338
FCHIP_F2	3588.363
FCHIP_F17	3563.363
FCHIP_H2	2639.099
FCHIP_H17	2639.099
FCHIP_K2	3729.343
FCHIP_K17	3654.784
FCHIP_M2	2748.339
FCHIP_M17	2699.454
FCHIP_U3	3640.140
FCHIP_U5	3638.069
FCHIP_U6	2846.734
FCHIP_U13	2753.008

**2.** Click:

### Net Impedance Summary

A summary table is displayed. The table includes the following information for all selected Signal Nets.

- Net Name
- Number of Tace Reference Discontinuity
- Number of Vias
- Maximum Impedance
- Minimum Impedance
- Dominant Impedance
- Dominant Impedance Length Percentage
- Trace / Wirebond Length

Net Count	Net Name	A No. of Trace Ref	No. of Vias	Maximum Impedance (Ohm)	Minimum Impedance (Ohm)	Dominant Impedance (Ohm)	Dominant Imp Length (%)	Trace ,wirebond total length(n
1	Net_1	0	2	74.012	35.423	74.012	92.567	6.727
2	Net_2	0	2	74.012	35.423	74.012	91.363	5.790
3	Net_3	0	2	74.012	35.423	74.012	91.562	5.927
4	Net_4	0	2	74.012	35.423	74.012	92.618	6.774
5	Net_5	0	2	74.012	35.423	74.012	93.888	8.181
6	Net_6	0	2	74.012	35.423	74.012	92.951	7.094
7	Net_7	0	2	74.012	35.423	74.012	92.412	6.590
8	Net_8	0	2	74.012	35.423	74.012	91.860	6.143
9	Net_9	0	2	74.012	35.423	74.012	91.255	5.718
10	Net_10	0	2	74.012	35.423	74.012	90.623	5.333
11	Net_11	0	2	74.012	35.423	74.012	89.975	4.988
12	Net_12	0	2	74.012	35.423	74.012	89.315	4.680
13	Net_13	0	2	74.012	35.423	74.012	88.811	4.469
14	Net_14	0	2	74.012	35.423	74.012	88.227	4.247

### Net Coupling Summary

A summary table is displayed. It includes the following information for all selected Signal Nets.

- Net Name
- Aggressor Net with Max Coupling
- Maximum Coupling Coefficient
- % Length with Max Coupling over the total length
- % Length with Coupling Coefficient > 0.05
- % Length with Coupling Coefficient 0.03 0.05
- % Length with Coupling Coefficient 0.02 0.03

Net count	Net name	Aggressor net with max coupling	Max coupling coefficient	% length with max coupling	% length with coupling coef > 0.05	% length with coupling coef 0.03~0.05	% length with
1	Net_1	Net_10	0.109	39.193	39.193		
2	Net_2	Net_13	0.106	43.369	43.369		
3	Net_3	Net_18	0.042	42.764		42.764	
4	Net_4	Net_21	0.140	39.293	80.033		
5	Net_5	Net_24	0.057	34.417	34.417		
6	Net_6	Net_7	0.036	37.776		37.776	
7	Net_7	Net_8	0.057	39.445	39.445		
8	Net_8	Net_9	0.110	41.265	41.265		
9	Net_9	Net_8	0.111	42.986	42.986		
10	Net_10	Net_1	0.109	44.843	44.843		
11	Net_11	Net_12	0.043	46.771		46.771	
12	Net_12	Net_2	0.044	48.573		48.573	
13	Net_13	Net_2	0.107	49.801	49.801		

4. Click:

Impedance Plot (collapsed)

The Trace and Wirebond Impedance is displayed (collapsed) from Die to Board Circuit.

NOTE!	If it is a Multi-die package, then follow these steps.
	1. Select a Component Name in the From: drop-down list.
	2. Select a Component Name in the To: drop-down list.
	The Trace and Wirebond Impedance along the path of the Start-Com- ponent to the End-Component is shown for all Nets between the se- lected two components.





If there are any reference changes on the same layer, those changes are clearly marked.



Impedance Plot (expanded)

Trace and Wirebond Impedance is displayed from Die to Board Circuit (expanded).



#### Impedance Plot (expanded)

Place your cursor on a Curve or Line. Detailed information about the selected Cureve or Line is displayed.

# NOTE!

To use the Cross Probe feature, double-click on any Trace section in the plot. The Trace is shown in the layout with the highlighted line.



# Impedance

**1.** Click:

Impedance Table

For each Net, the table displays each:

- Section name
- Length percentage over the whole length
- Impedance
- Total length
- Distance from starting component

Net 🗠	*	Trace/wirebond Name	% of its net length	Impedance(Ohm)	Length(mm)	Trace/wirebond distance from Starting Component(mm)
Net_1		WireBond175_wb_u	37.32%	106.885	4.336	0.000
Net_2		Trace701::Net_1	3.68%	74.012	0.427	4.336
Net_3		Trace700::Net_1	6.89%	74.012	0.800	4.763
Net_4		Trace699::Net_1	27.08%	74.012	3.146	5.563
Net_5	Ξ	Trace698::Net_1	11.24%	74.012	1.306	8.710
Net_6		Trace697::Net_1	4.72%	74.012	0.548	10.015
Net_7		Trace239::Net_1	4.30%	35.423	0.500	11.118
Net_8						
Net_9						
Net_10						

2. Click:

Impedance in Layout

- 3. Select a Component Name in the From: drop-down list.
- **4.** Select a Component Name in the **To:** drop-down list. The Impedance along the Traces and Wirebonds between the two selected components is shown.



# **Coupling Coefficient**

1. Click:

Coupling Coefficient Plot (collapsed)

- 2. Select a Component Name in the From: drop-down list.
- 3. Select a Component Name in the To: drop-down list.

The strongest coupling coefficient of each Trace and Wirebond section is displayed (collapsed) from the **Start Component** to the **End Component**.



- 4. Select Nets in the Netlist.
- 5. Right-click to select or deselect the Net.



6. Select Single Net from the top drop-down menu. A Single Net Coupling Coefficient is displayed. It includes a few of the strongest couplings to each section.

The same color is used for the same layer.

7. Place your mouse on a Curve. Detailed information about the Curve is displayed.



Coupling Coefficient Plot (expanded)

- 9. Select a Component Name in the From: drop-down list.
- 10. Select a Component Name in the To: drop-down list.

The strongest **Coupling Coefficient** for each Trace and Wirebond section is displayed (expanded) from the **Start Component** to the **End Component**.



11. Click:

**Coupling Coefficient Table** 

- **12.** Select a Component Name in the **From:** drop-down list.
- **13.** Select a Component Name in the **To:** drop-down list.

The strongest Coupling Coefficient for each Trace and Wirebond section is listed with the table.

14. Choose a specific Net to view the detailed results.

Net	🛆 Length(mm 📥	Trace/wirebond Name	Length(mm)	% of its net length	Coupled Lines	Coupling Coefficient
Net_1	11.618	WireBond175_wb_u	4.336	37.32%	WireBond67_wb_u1::Net_10	0.109
Net_2	10.779	Trace701::Net_1	0.427	3.68%		
Net_3	10.910	Trace700::Net_1	0.800	6.89%		
Net_4	11.713	Trace699::Net_1	3.146	27.08%		
Net_5	13.030	Trace698::Net_1	1.306	11.24%		
Net_6	11.956	Trace697::Net_1	0.548	4.72%		
Net_7	11.438	Trace239::Net_1	0.500	4.30%		
Net_8	11.014					
Net_9	10.584					
Net_10	10.224					

Coupling Coefficient in Layout

- 16. Select a Component Name in the From: drop-down list.
- 17. Select a Component Name in the To: drop-down list.

The strongest Coupling Coefficient of each Trace and Wirebond section is overlaid on the Layout.

**18.** Move your cursor onto the Layout. The Net Name and Coupling Coefficient is shown.



# Single-Ended and Diff. Pair Net Checking Switching

If there are differential pair signal nets defined and enabled in Net Manager, you can switch

the trace checking report and plot between single-ended and differential pair signal nets.

The impedance and coupling coefficient table and plot can be switched by choosing **SingleEnded** or **Diff** from the **Single Ended or Diff** column.



# **Net Couplings**

This feature is for Single-die Single-BGA package only. Using all Power and Ground Nets ad Reference Nets, couplings report the:

- Mutual Inductance
- Mutual Capacitance
- Crosstalk among all Signal Nets

Every signal net can be considered as a single-ended net. Or, if differential pair exists, it can be considered as a whole in discussing crosstalk with other nets, i.e. Differential pair vs. Single-ended or another differential pair.



### Signle-ended Based

1. Click:

Mutual Inductance and Capacitance (under Signle-edned Based)

A table shows:

- Resistance
- Mutual Inductance and Capacitance
- Near-ended Crosstalk
- Total Near-ended Crosstalk of each Net as Victim
- Far-ended Crosstalk assuming the Rise Rime is 100 ps

Net i	Net 1	Rij (mOhm)	LIJ (nH)	CIJ (pF)	NEXT (%)	Total NEXT (%)	FEXT (%)	Tr (pS)	
Net_1	Net_1	271.466	6.77129	1.40194		8.56234			
Net_1	Net_10	0	0.673844	0.0543725	3.63607		-3.00417	100	
Net_1	Net_9	0	0.433952	0.0181933	1.99271		-2.49417	100	
Net_1	Net_8	0	0.254391	0	0.958141		-1.83376	100	
Net_1	Net_11	0	0.160449	0	0.629086		-1.16111	100	
Net_1	Net_7	0	0.123555	0	0.456147		-0.884778	100	
Net_1	Net_12	0	0.0781773	0	0.310549		-0.566104	100	
Net_1	Net_6	0	0.076406	0	0.280166		-0.547804	100	
Net_1	Net_14	0	0.0263146	0	0.10684		-0.191491	100	
Net_1	Net_16	0	0.0235187	0	0.096987		-0.172855	100	
Net_1	Net_15	0	0.0232635	0	0.0956424		-0.169863	100	
Net_2	Net_2	257.394	6.36301	1.3223		8.51554			
Net_2	Net_13	0	0.671347	0.0534184	3.83533		-3.01932	100	
Net_2	Net_12	0	0.419509	0.0188933	2.09137		-2.38551	100	
Net_2	Net_14	0	0.161937	0	0.679096		-1.17841	100	
Net_2	Net_11	0	0.161062	0	0.651631		-1.16554	100	
Net_2	Net_15	0	0.0884465	0	0.375694		-0.645807	100	
Net_2	Net_10	0	0.0877581	0	0.352181		-0.635655	100	
Net_2	Net_9	0	0.0378359	0	0.149022		-0.272522	100	
Net_2	Net_16	0	0.0315619	0	0.13446		-0.23197	100	
Net_2	Net_8	0	0.0315379	0	0.122435		-0.227339	100	
Net_2	Net_17	0	0.0299699	0	0.124315		-0.217064	100	
Net_3	Net_3	259.857	6.4191	1.33039		7.15329			
Net_3	Net_18	0	0.371279	0.0182203	1.87086		-2.05114	100	
Net_3	Net_19	0	0.331794	0.0120447	1.58481		-2.01174	100	
Net_3	Net_20	0	0.22027	0	0.88141		-1.59764	100	
Net_3	Net_17	0	0.21053	0.00616289	0.991971		-1.31208	100	
Net_3	Net_16	0	0.106873	0	0.453499		-0.78548	100	
Not 3	Not 21	0	0 103712	0	0.41142		-0 754057	100	

### **Change Rise Time**

Use the following steps to change the Rise Time.

- **1.** Select several lines.
- 2. Click in the corner of Ts (ps). One cell is enabled for change.
- **3.** Change the enabled cell to a new number.
- 4. Click Enter. All selected lines are changed.

	_
FEXT (%)	Tr (μS)
3.00417	100
-2.49417	100
-1.83376	100
-1.16111	100
-0.884781	100
-0.566105	100
-0.547804	100
-0.191492	100
-0.172854	100
-0.169863	100
3.01932	100
-2.38551	100
-1.17841	100
-1.16554	100

EXT (%)	Tr (pS)
-3.00417	100
-2.49417	100
1.83376	100
-1.16111	100
0.884778	100
-0.566104	100
0.547804	100
-0.191491	100
0.172855	100
-0.169863	100
-3.01932	100
-2.38551	100
-1.17841	100
-1.16554	100

FEXT (%)	Tr (pS)
-1.50209	200
-1.24708	200
-0.916881	200
-0.580556	200
0.442391	200
0.283052	200
-0.2/3902	200
-0.0957459	200
-0.0864272	200
-0.0849313	200
3.01932	100
-2.38551	100
-1.17841	100
-1.16554	100

### **Histogram View**

1. Click:

Total NEXT Histogram View

The total NEXT for each Net as victim is plotted left-to-right and smallest-to-largest.

2. Stop your mouse on a Bar. Detailed information for the Bar is displayed.



# **Diffpair and Single-ended**

1. Click

#### Mutual Inductance and Capacitance (Under Diffpair and Single-ended)

A table shows:

- Nets: differential pair are shown a whole unit
- Resistance (see definition of R for differential pair)
- Mutual Inductance and Capacitance
- Near-ended Crosstalk
- Total Near-ended Crosstalk of each Net (or differential pair) as Victim
- Far-ended Crosstalk assuming the Rise Rime is 100 ps

Net i	Net j	Rij (mOhm)	Lij (nH)	Cij (pF)	NEXT (%)	Total NEXT (	FEXT (%)	Tr (pS)
Diff_L_05N-L_05P	Diff_L_05N-L_05P	832.524	10.8655	0.583		9.64		
Diff_L_05N-L_05P	Single_2	0	0.7882	0.097	5.57		1.51	100
Diff_L_05N-L_05P	Diff_L_08N-L_08P	0	0.4329	0.126	3.34		0.42	100
Diff_L_05N-L_05P	Single_1	0	0.1097	0.006	0.74		0.58	100
Diff_L_08N-L_08P	Diff_L_08N-L_08P	1213.52	12.6047	0.971		4.65		
Diff_L_08N-L_08P	Diff_L_05N-L_05P	0	0.4329	0.126	3.09		-0.07	100
Diff_L_08N-L_08P	Single_2	0	0.1642	0.015	0.79		-0.51	100
Diff_L_08N-L_08P	Single_1	0	0.1180	0.015	0.76		-0.30	100
Single_1	Single_1	217.127	3.5739	0.711		2.30		
Single_1	Single_2	0	0.1343	0.006	0.88		-0.64	100
Single_1	Diff_L_08N-L_08P	0	0.1180	0.015	0.73		-0.25	100
Single_1	Diff_L_05N-L_05P	0	0.1097	0.006	0.68		0.51	100
Single_2	Single_2	345.325	5.5739	0.942		7.12		
Single_2	Diff_L_05N-L_05P	0	0.7882	0.097	5.32		1.13	100
Single_2	Diff_L_08N-L_08P	0	0.1642	0.015	0.84		-0.61	100
Single_2	Single_1	0	0.1343	0.006	0.96		-0.73	100

#### **Change Rise Time**

Use the following steps to change the Rise Time (Similiar to Single-ended Based).

- **1.** Select several lines.
- 2. Click in the corner of Ts (ps). One cell is enabled for change.
- 3. Change the enabled cell to a new number.
- 4. Click Enter. All selected lines are changed.

#### **Histogram View**

Use the following steps to show the Histogam View (Similar to Single-ended Based).

1. Click:

Total NEXT Histogram View

The total NEXT for each Net as victim is plotted left-to-right and smallest-to-largest.

2. Stop your mouse on a Bar. Detailed information for the Bar is displayed.

# **Insertion and Return Loss**

Insertion and Loss is reported for all Signal Nets by using Power and Ground Nets as Reference Nets. This feature is only available for Single-die Single-BGA packages.

Insertion and Return Loss	٢
Insertion Loss	
Return Loss	

1. Click:

#### Insertion Loss

The Insertion Loss for all Signal Nets is shown.



### Return Loss

The Return Loss for all Signal Nets is shown.



# **Current Checking**

The Workspace lists options to display results. Click on the desired option.

#### **Current Checking**

- Via Counts Via Current Histogram Via Current by Layer Via Current Table Voltage Distribution by Layer Plane Current Density by Layer
- 1. Click:

Via Counts

The **Via Counts Table** is shown for each Power / Ground Net. The number is classified at each Via starting layer.

Net	Signal\$M1->Signal\$VSS	Signal\$VSS->Signal\$VDD	Signal\$VDD->Signal\$M4
VSS	28	256	256
VDD_1	4	4	14
VDD_2	4	4	14
VDD_3	4	4	14
VDD_4	4	4	14

Via Current Table

A detailed table showing Current Density is displayed. The table includes:

- Via Name
- Via Net
- Actual Current
- Current Density
- X,Y Coordinates
- Start Layer
- Upper Node Name
- End Layer
- Lower Node Name
- Padstack

Via Name	Net	Current (A)	Current Density (A/mm^2)	PosX (mm)	PosY (mm)	StartLayer	Upper Node	EndLayer	Lower Node	PadStack
Via254::VDD_1	VDD_1	-0.0807358	2.5699	-13.8536	-6.8536	Signal\$VDD	Node2598:	Signal\$M4	Node477::	via4003
Via264::VDD_1	VDD_1	-0.0620086	1.9738	-13.8536	-8.8536	Signal\$VDD	Node2600:	Signal\$M4	Node493::	via4003
Via273::VDD_1	VDD_1	-0.0372965	1.18719	-13.8536	-10.8536	Signal\$VDD	Node2602:	Signal\$M4	Node507::	via4003
Via302::VDD_1	VDD_1	-0.0134064	0.42674	-13.8536	-12.8536	Signal\$VDD	Node2604:	Signal\$M4	Node561::	via4003
Via334::VDD_1	VDD_1	-0.0133563	0.425144	-13.8536	12.8536	Signal\$VDD	Node2620:	Signal\$M4	Node593::	via4003
Via343::VDD_1	VDD_1	-0.0371082	1.18119	-13.8536	10.8536	Signal\$VDD	Node2622:	Signal\$M4	Node607::	via4003
Via370::VDD_1	VDD_1	-0.0618354	1.96828	-13.8536	8.8536	Signal\$VDD	Node2624:	Signal\$M4	Node657::	via4003
Via378::VDD_1	VDD_1	-0.0803316	2.55703	-13.8536	6.8536	Signal\$VDD	Node2626:	Signal\$M4	Node669::	via4003
Via388::VDD_1	VDD_1	-0.0935236	2.97695	-13.8536	4.8536	Signal\$VDD	Node2628:	Signal\$M4	Node685::	via4003

3. Click:

Via Current Histogram View

The Via Absolute Current window appears.

👄 🐽 💲 🏌 🔁 📷 🖂 I	🗷 🖸 Va Absolute Currer 🔻
Net	
VDD_1	Via Absolute Current (A) Via Absolute Current
VDD_2	
VDD_3	4
VDD_4	
VSS	
VSSCOre	
	3
	2
	1

4. For each Net, the Via Current is plotted from the smallest (left) to the largest (right), click: Net Name

The Via Current is changed.

### 5. Select Via Absolute Current Density.

It is plotted from the smallest (left) to the largest (right)

6. Click the desired Net Name.

The via current density is changed.



Current Checking > Via Current in Layout

The **Via Current** is overlaid on the layout to quickly identify the location. The **Color Map** is used as a current value scale.

- 8. In the **Present Results** window, click on a Layer Name. The Layer changes to reflect the selected Layer Name.
- 9. Select or Deselect:

**Results Overlay** 

The display changes between overlay results and the physical layout.



Current Checking > Voltage Distribution in Layout

Voltage distribution (IR Drop) is overlaid for each layer.

- **11.** Select a different layer. The display changes according to the selected layer.
- **12.** Stop the mouse cursor on the display, The actual value is shown.



Current Density Checking > Plane Current Density in Layout

Each Plane Current Density is overlaid on each layer.

- **14.** Select a different layer. The display changes according to the selected layer.
- **15.** Stop the mouse cursor on the display, The actual value is shown.


## **Save Results**

- 1. Click:
  - Workspace > Save Results
- **2.** Input a file name.
- 3. Click **OK** to save the results.

🕥 🗼 🕶 Dbug				🝷 🔯 Search Dbug	) 🖉
Organize 👻 New folder					iii • 📀
🔺 Favorites 🔶	Name *	Date modified	Туре	Size	
🚱 Recently Changed	A03141A.spd	11/7/2011 10:13 AM	SPD Fie	792 KB	
📜 Public 📰 Desktop 🕕 Downloads	Demo1.xml	11/7/2011 10:13 AM	XML Document	55 KB	
Libraries Documents Music Pictures Videos					
Computer OS (C:) RECOVERY (D:)					
File name: EPAR	Result				-
Save as type: EPA r	result file (*.*)				-
Hide Folders				Save	Cancel

## **Load Results**

- 1. Launch XtractIM.
- 2. Load in the Workspace file.
- **3.** Load in the SPD file.
- 4. Click:

## Workspace > Load Results

The Load Result window opens.

+Load EPA result From				×
🔿 🔂 🕶 Dbug			🔹 🛂 Search Dbu	ıg 🔎
Organize 🔻 New folder			đ	• 🔳 🥹
🖃 🌟 Favorites -	Name *	Date modified	Туре	Size
Recently Changed	A03141A.spd	11/7/2011 10:13 AM	SPD File	792 KB
Public     Desitton	Demo1.xml	11/7/2011 10:13 AM	XML Document	55 KB
Desktop	EPAResult	11/7/2011 2:53 PM	File	1 KB
	EPAResult_BI	11/7/2011 2:53 PM	File	1 KB
🗆 🚞 Libraries	EPAResult_DC	11/7/2011 2:53 PM	Fie	0 KB
E Documents	EPAResult_IC	11/7/2011 2:53 PM	Fie	1 KB
E 🛃 Music	EPAResult_IR	11/7/2011 2:53 PM	File	1 KB
H S Pictures	EPAResult_LC	11/7/2011 2:53 PM	Fie	1 KB
a vicus	EPAResult_NC	11/7/2011 2:53 PM	Fie	3 KB
🖃 🍓 Computer	EPAResult_TC	11/7/2011 2:53 PM	File	1 KB
🗄 🧶 OS (C:)				
E 🚙 RECOVERY (D:)				
E 🛫 Code (\\SOURCE) (Z:)				
H10.0 Task Plan on sharepoint	<u>.</u>			
File name: EPAResult			<ul> <li>EPA result File (</li> </ul>	*.*) 👻
			Open	Cancel
				11

- 5. Select the file you want to open.
- 6. Click **Open** to view the results.

All results can be displayed with the same operation.



## **Create Report**

1. Select

View / Export Results > Report

The following window pops up. A default \*.htm template is loaded and highlighted.

File			
General File Manager Save Options Hotkeys		Change the 'Rep	oort' options in XtractIM
Grid and Unit View Processing Trace Error Checking 3D Layout View	•	General Information Report template Notes:	rary\template\XtractIM\XtractIM_Report_Template_EPA_Default.htm
Display Quality Simulation (Basic) General Net and Coupling Special Void Output SPICE Circuit Report Simulation (Advanced) Electric Models Mesh Nets and Shapes	<u> </u>	Optional Plots	

2. Click OK.

The report file is created.



3. To save the report file as \*.htm, \*.html, or \*.mht format, select

File > Save As (\*.htm)...



The Save Webpage window opens.

Save Webpage				×
New fo	older 🔻	👻 🔯 Search New fo	older	2
Organize 👻 New fo	older		•	0
┢ Favorites	Name *	Date modified	Туре	
Recently Chang	ed EPA_DC	1/17/2012 6:06 PM	File folder	
U Public	EPA_DC_20120113084226	1/13/2012 8:42 AM	File folder	
Downloads	EPA_DC_20120113143438	1/13/2012 2:34 PM	File folder	
Dominouus	EPA_DC_20120117181201	1/17/2012 6:12 PM	File folder	
Computer				
RECOVERY (D·)				
File name:	Simulation Report.htm			-
Save as type:	Webpage, complete (*.htm;*.html)			-
• Hide Folders	Web Archive, single file (*.mht) Webpage, HTML only (*.htm;*.html) Text File (*.txt)	• <u>S</u> ave	Cancel	

- **4.** Select the location, file name and type.
- 5. Click Save to save the file.

# **Load Previously Saved Results**

- **1.** Click *io* open an XtractIM workspace file \*.ximx.
  - Save Result Load Result Report
- 2. Click Load Result in the Workflow pane.

The result should be related with above \*.ximx project.

3. Click Report.

A new report can be created.

# SUMMARY OF ELECTRICAL PERFORMANCE ASSESSMENT FEATURES

DISTRIBUTION System	FEAT	URES	BGA PACKAGES	LEADFRAME
	Power-Ground	Inductance & Capacitance	Single-die Multi-die Stacked-BGA	No
Power and Ground		Broadband Impedance	adband Single-die edance Single-BGA	
	Per-pin Property	Inductance & Resistance	Single-die Multi-die Stacked-BGA	No
	DC Current Density	Current Density	Single-die Single-BGA	No
	Layout Checking	Trace / Wirebond Impedance & Coupling Coefficient	Single-die Multi-die Stacked BGA	Single-die Multi-die
Signal	Net Couplings	Mutual LC and NEXT	Single-die Single-BGA	No
	Insertion and Return Loss	Insertion & Return Loss	Single-die Single-BGA	No

# Chapter

# **TCL Command Support for Workspace Setup**

This chapter takes you through the steps to use TCL command for workspace setup in the XtractIM tool.

# **PREPARE FOR THE SIMULATION**

Get the following issues ready before you begin the simulation.

- The Bump diameters, length, heights and conductivity
- The Stackup information
- The files to be simulated in SPD format

# LESSON ONE: RUNNING TCL COMMAND FOR WORKSPACE SETUP

## Introduction

TCL (Tool Command Language) scripts can be used to configure and automate frequently used command in Allegro Sigrity tools. They can also be launched outside the Sigrity tools in batch mode to automate company design flows.

New TCL command is developed to support workspace setting in XtractIM.

For the other existing TCL command, please refer to *Tcl\_Scripting\_Reference.pdf* in <ASI\_INSTALL\_DIR>\Update3\Doc\Common Documents\ for details.

Three package types are used in this tutorial to practice the new TCL command.

## Single-Die BGA Package Sample

1. Load *flipchip.spd*.

It is typically located in <ASI\_INSTALL\_DIR>\Update3\SpeedXP\Samples\XtractIM\Single-Die\_Sample\_files\.



2. Remove the existing bump and solder ball layers if any before running TCL command.

Layer Mana	ager -> St	ack Up											□ ×
Stack Up	Pad Sta	:k											
Layer #	Color	Layer Icon	Layer Name	Thickness(	Material	Conductivity(S	Fill-in Dielectric	Permittivity	Loss Tangent	Shape Name	Trace Width(mm)	Trapezoidal Angle(°)	Roughness(mm)
1			Signal02	0.005		5e+007		[1]	[0]		0.1	90	0
			Bump01	0.1		D.		4	0				
2			Signal\$M1	0.015		5.8e+007		[4.1]	[0]		0.1	90	0
			Medium\$dielectric2	0.125		0		4.2	0				
3			Signal\$VDD	0.02		5.8e+007		[4.2]	[0]	Shape\$VDD	0.1	90	0
			Medium\$dielectric3	0.25		0		4.2	0				
4			Signal\$VSS	0.02		5.8e+007		[4.2]	[0]	Shape\$VSS	0.1	90	0
			Medium\$dielectric4	0.125		0		4.2	0				
5			Signal\$M4	0.015		5.8e+007		[2.6]	[0]		0.1	90	0
			Solderball01	0.4		0		1	0				
6			Signal01	0.001		5.8e+007		[2.5]	[0]		0.1	90	0
			Medium01	0.05		0		4	0				
						2							
4				14	111								•
Total Thid	mess: 1.1	260e +000 mn	n								Enforce causalit	y View Material	Import
Solder	Ball Layer			Right-dick on	a dielectric(or signal)	layer to insert a so	lder ball layer.				Export	Auto Set Layer Special V	xid Filter
										Unit:	mm 🔻 O	K Cancel	Apply

A fresh example is like the following.

Workspace Edit	View N	lode	Setup	Tools	s Win	dow He	slp									cādence
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II Enabled Net(s)	0-0	I I	L 🖛 -			5	► × 🖏 🖸	0000	) 😰 🔸 🐿	😐 co 🚍   🖻	8 14 🔿 🖪	1 #A	-		@ Ø @ <b>@</b>	
×I I*							-									
orkflow: XtractIM			e14 e	13 ,-12	e11	-10 -9	.8 .7 .6 .	5 -4 -3	21 .0	1 ,2 ,3 ,	4 ,5 ,6 ,	7 ,8 ,9	,10 ,11 ,7	12 ,13 1	Laver Selection	
Indel Extraction			uluutuulu	adardant	anduntum	lantarilanta	համահանահան	տեսակատեսակատես	ոհանահանան	ոհանականուհանու	untardantandantand	առնուհամասնու	ասհամասհանուհ	minulanian	Constants	
	0														Signal SVDD	
Manage Workspace	$\odot$	1													Signal\$VSS	
Load Workspace		6										1			Signal\$M4	
Load a New/Different	Layout	1.3														
Package Setup		0							$\sim$ $\sim$ 1							
Package Type: Wrebo	nd	1	Layer	r Manag	er -> Sta	ck Up										
X Circuits		1.3														
X Stackup		0	Sta	ck Up	Pad Stad	<	100 200	100000	1000000000	100000000000000000000000000000000000000	Terrore and the second second	1.00		1	1	
Nets		0	Lay	er#	Color	Layer Icon	Layer Name	Thickness(	Material	Conductivity(S	Fill-in Dielectric	Permittivity	Loss Tangent	Shape Name	Trace Width(mm)	Trapez
Cimulation Cotur		1.3	1				Signal \$M1 Madium Edial activity?	0.015		5.8e+007		[1]	(0)		0.1	90
simulation setup	0	1	2	_	-		Signal\$VDD	0.02		5.8e+007		[4.2]	[0]	Shape \$VDD	0.1	90
Module: 1815/RLGC	bood	5			-		Medium\$dielectric3	0.25		0		4.2	0			
Manufactori Type, Nece	(a)	1	3				Signal\$VSS	0.02		5.8e+007		[4.2]	[0]	Shape\$VSS	0.1	90
View/Export Results	$\overline{\mathbf{O}}$	N					Medium\$dielectric4	0.125		0		4.2	0			
Summary		4	4		_		Signal\$M4	0.015		5.8e+007		[1]	[0]		0.1	90
Branch RI		1														
Save Results		-														
Load Results		14														
Report		1														
ustomize Workflow		Ň														
		6														
		1														
		1-1														
		6			_			111								>
			Tot	al Thicko	ess: 5.7	00e-001 mm							Enforce causali	ty View M	aterial Imr	ort
		6		Solder B	alLaver			Right-click or	a dielectric(or sign	al) layer to insert a sol	der ball layer.		Export	Auto Set Laver S	pecial Void Eilte	
		4														
												Unit: m	m 🔽 🤇	ж	Cancel A	pply
		6					-/	/							Online Calm	y objects by
															What Color C	Layer Color
																-
			_													
		53												-		

**3.** Choose View > Pane > TCL Command to open the TCL command input console.

XtractIM - Untitled - [flipchip.spd Layer	View]	
I Workspace Edit View Mo	de Setup Tools Window Help	
	💼 😥 🖲 🗉 🐵 🔿 🖓 🕼 🖓 🖗 🖉 🎯 💌 💌 💭 💟 🔯 Extractor Resul	t <b>→ 1</b> 1 40 40
All Enabled Net(s)		
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Model Extraction		
Manage Workspace 🔗		
Load Workspace	003	
Load a New/Different Layout		
Package Setup	6	
Package Type: Wirebond		
× Circuits	4	
X Stackup		
X Solder Ball	2211	_
<ul> <li>Nets</li> </ul>		
Simulation Setup 💿		
Module: IBIS/RLGC		
Simulation Type: Net-Based		
View/Export Results	4	
Summary		
SPICE/IBIS Model	6	
RLC Per Net		
RLC Distributions		
Segment RLC		
RLC vs. Net Length		*
3D View		r
Histogram	ICL Command	×
CrossTalk (Diffpair vs Single-Ended)		
3D View		
Histogram		
Save Results		
Load Results		
Report		
Customize Workflow ¥		
		Run
Ver: 13.0.a0.11113 (XtractIM)	Mouse(mm): X: -19.076 Y: 7.262	Ready

4. Copy the following TCL command to the TCL Command console. sigrity::update PackageType -dieType {0} -bgaType {0} -attachType {1} sigrity::update Circuits -dieCkts {U1} -boardCkts {BGA1} sigrity::add Layer {bump} -above {Signal\$M1} -circuit {U1} sigrity::add Layer {ball} -under {Signal\$M4} -circuit {BGA1}

sigrity::update Attributes -circuit {U1} -Dmax {0.1e-3} -D1 {0.08e-3} -D2 {0.08e-3} -HT {0.1e-3} -conductivity {5.0e+7}

sigrity::update Attributes -circuit {BGA1} -Dmax {0.4e-3} -D1 {0.3e-3} -D2 {0.3e-3} -HT {0.3e-3} -conductivity {5.0e+7}

sigrity::update ExtractionFreq {30e+6}

sigrity::update cpline -risetime {100} -percent {3} -all



5. Click the *Run* button in the TCL Command console.

The Package Setup is automated.

XtractIM - Untitled - [flipchip.spd Layer	r View]		
♦ Workspace Edit View Mo	de Setup Tools	Window Help	
	- <b>.</b>	A C L A C A B A + N +	E Extractor Result
All Enabled Net(s)	I = T ·		
Workflow: XtractIM X	2 -20 -18 -1	16 -14 -12 -10 -8 -6 -4 -2	10 12 14 16 18 10 12 14 16 18 20 A
Model Extraction 🔗			
Manage Workspace	10		
Manage Workspace			
Load workspace	0		
Load a New/Diriel ent Layout			
Package Setup	0		
Package Type: Flip-Chip			
<ul> <li>Circuits</li> </ul>	4		
<ul> <li>Stackup</li> </ul>			
V Bumps			
Solder Ball			
✓ Nets			
Simulation Setup			
Module: IBIS/RLGC	12		
Simulation Type: Net-Based			
View/Export Results	4		
Summary			
SPICE/IBIS Model			
RLC Per Net	6		
RLC Distributions			
Segment RLC	4		
RLC vs. Net Length	1		▶
CrossTalk (Single-Ended)	TCL Command		v
3D View			1
Histogram			
CrossTalk (Diffpair vs Single-Ended)			
3D View			
Histogram			
Save Results			
Load Results			
Report			
Customize Workflow ×			
			Run
	1		
Ver: 13.0 a0 11113 (XtractIM)	Mou	se(mm): X: -9.26 V: 0.654	Ready

The relationship between individual TCL command and the corresponding Package Setup is described as follows.

• sigrity::update PackageType -dieType {0} -bgaType {0} -attachType {1}

Package Setup ->	Package Type	
Single Die	O Stacked Die	O Side-by-side Die
Single BGA	O Stacked BGA	OLeadframe
O Wirebond	Flip-Chip (WL-CSP)	OBoth

• sigrity::update Circuits -dieCkts {U1} -boardCkts {BGA1}

Ckt Name	Ckt Model	Ckt Type	
C1	Cap0402		
C2	Cap0402		
C3	Cap0402		
C4	Cap0402		
C5	Cap0402		
C6	Cap0402		
C7	Cap0402		
C8	Cap0402		
U1	FC	Die	
BGA1	untitled_pac	. Board	

- sigrity::add Layer {bump} -above {Signal\$M1} -circuit {U1}
- sigrity::add Layer {ball} -under {Signal\$M4} -circuit {BGA1}

Static Up	Fau Sta	uk j	1	1	1	1	1	1	1	1	1	_
Layer #	Color	Layer Icon	Layer Name	Thickness(	Material	Conductivity(S	Fill-in Dielectric	Permittivity	Loss Tangent	Shape Name	Trace Width(mm)	Trapezo
1			Signal01	0.001		5.8e+007		[1]	[0]		0.1	90
			Bump01	0.1		0		1	0			
2			Signal\$M1	0.015		5.8e+007		[2.6]	[0]		0.1	90
			Medium\$dielectric2	0.125		0		4.2	0			
3			Signal\$VDD	0.02		5.8e+007		[4.2]	[0]	Shape\$VDD	0.1	90
			Medium\$dielectric3	0.25		0		4.2	0			
4			Signal\$VSS	0.02		5.8e+007		[4.2]	[0]	Shape\$VSS	0.1	90
			Medium\$dielectric4	0.125		0		4.2	0			
5			Signal\$M4	0.015		5.8e+007		[2.6]	[0]		0.1	90
			Solderball01	0.3		0		1	0			
6		TE	Signal02	0.001		5.8e+007		[2.5]	[0]		0.1	90
			Medium01	0.05		0		4	0			
7		<b>TTTTTTTTTTTTT</b>	Signal03	0.03556		5.95e+009		[1]	[0]	Shape001	0.1	90
4				111								•
Total Thic	mess: 1.0	576e+000 mm	1						Enforce causali	ty View N	laterial Imp	port
V Soldar	Rall Laver	Bumpla	ver						Export	Auto Set Laver	Special Void Filte	er.

 sigrity::update Attributes -circuit {U1} -Dmax {0.1e-3} -D1 {0.08e-3} -D2 {0.08e-3} -HT {0.1e-3} -conductivity {5.0e+7}

Package Setup -> 8	Bumps							×
Layer Name	Circuit Name	Dmax (mm)	D1 (mm)	D2 (mm)	HT (mm)	Material	Conductivity (S/m)	
Bump02	U1	0.1	0.08	0.08	0.1		5e7	Bump Model
								$\begin{array}{c} H \longrightarrow D1 \longrightarrow H \\ \leftarrow Dmax \longrightarrow HT \\ H \longrightarrow D2 \longrightarrow H \end{array}$
ОК	Cancel							

• sigrity::add Layer {ball} -under {Signal\$M4} -circuit {BGA1}

Package Setup ->	Solder Ball								×
Layer Name	Circuit Name	Dmax (mm)	D1 (mm)	D2 (mm)	HT (mm)	Material	Conductivity (S/m)	Medium Thickness (mm)	Solder Ball Model
Solderball02	BGA1	0.4	0.3	0.3	0.951		5e7	0.05	i← D2→ N (← Dmax → HT ↓ → D1→ ↓ ↓ Medium Thickness ↑ Ground
•					111			<b>&gt;</b>	
OK	Cancel								

sigrity::update ExtractionFreq {30e+6}

Extraction Frequency			×
Extraction Frequency:	30	MHz	OK Cancel

• sigrity::update cpline -risetime {100} -percent {3} -all

Net	Mana	ager			×			
Net:				- D Show	Coupled I			
Net	List (	Sort enabled first) $\triangle$	%Coupling	Rise Time (ps)				
	R	Unnamed Net(s)	3	100				
	V	PowerNets	3	100				
	-	VDDcore			=			
	V	VDD_1						
	V	VDD_2						
	$\checkmark$	VDD_3						
	$\checkmark$	VDD_4						
	~	GroundNets	3	100				
	$\checkmark$	VSS						
	~	DEFAULT	3	100				
	~	Net_1	3	100				
	~	🖊 Net_2	3	100				
	~	🖊 Net_3	3	100				
	~	🖊 Net_4	3	100				
	~	🖊 Net_5	3	100				
	~	🖊 Net_6	3	100				
	~	Net_7	3	100				
	~	🗾 Net_8	3	100				
	~	🖊 Net_9	3	100				
	~	🖊 Net_10	3	100				
	✓	🖊 Net_11	3	100				
	✓	<mark>/</mark> Net_12	3	100				
	$\checkmark$	Net_13	3	100				
	$\checkmark$	Net_14	3	100				
	$\checkmark$	Met_15	3	100				
	$\checkmark$	Net_16	3	100	-			
General C Keep shape enabled when the net is disabled Gray Disabled Coupled Lines Disable Coupled Line Simulation Coupled Lines Report								
1.00	or Col	action Net Manage						
Lay	erse	Net Manage	=1					

6. The TCL command used above can also be prepared in a .tcl file.

ĺ	FlipChip.tcl - Notepad		3
	Eile Edit Format View Help		
	<pre>sigrity::update PackageType -dieType {0} -bgaType {0} -attachType {1} sigrity::update Circuits -dieCkts {u1} -boardckts {B6A1} sigrity::add Layer {bump} -above {SignalSM1} -circuit {u1} sigrity::add Layer {ba1} -under {signalSM4} -circuit {B6A1} sigrity::update Attributes -circuit {u1} -Dmax {0.1e-3} -D1 {0.08e-3} -D2 {0.08e-3} -HT {0.1e-3} -conductivity {5.0e+7} sigrity::update Attributes -circuit {B6A1} -Dmax {0.4e-3} -D1 {0.3e-3} -D2 {0.3e-3} -HT {0.3e-3} -conductivity {5.0e+7} sigrity::update Attributes -circuit {B6A1} -Dmax {0.4e-3} -D1 {0.3e-3} -D2 {0.3e-3} -HT {0.3e-3} -conductivity {5.0e+7} sigrity::update Attributes -circuit {B6A1} -Dmax {0.4e-3} -D1 {0.3e-3} -D2 {0.3e-3} -HT {0.3e-3} -conductivity {5.0e+7} sigrity::update cpline -risetime {100} -percent {3} -all</pre>		*
			Ŧ
	4	F.	

7. Click the **Open a TCL file** icon to load in the prepared \*.tcl file



8. Click the Play TCL icon to run the prepared TCL command.

) 📲 🚂 🔮	
	Play TCL 🛛 🖓 🕢 🔂 🚱 📕

The same result will come out as in Step 5.

#### Multiple-Die BGA Package Sample

1. Load 2diestacked\_fcwb\_newnl.spd.

It is typically located in <ASI\_INSTALL\_DIR>\Update3\SpeedXP\Samples\XtractIM\Single-Die\_Sample\_files\.

A wirebond die is placed above a flipchip die on a BGA package.



*XtractIM - Untitled - [2diestacked_fcwb	_newnl.spd Layer View]					- 🗆 ×
🔶 Workspace Edit View Mo	de Setup Tools Wind	ow Help				cādence 🗕 🗗 🛪
Zoom All Enabled Net(s) V Workflow: Xtractim Model Extraction Page	ection			Extractor Result		
Load a New/Differen  Active Stackape Type: Wret Could a New/Differen Active Stackape Stackape Show Log	r ler w Network Parameter Display g Files	Editor Pane Output Pane Object Selection Folder Browser TCL Reader TCL Command			Signal\$0353F508BOTTOM	
Johne Lee     Meter     Meter     Meter     Module: IBIS/RLGC     Simulation Setup     Module: IBIS/RLGC     Simulatory Type: Net-Based     View/Export Results     Module: IBIS/RLGC     Summary     SICCE/IBIS Model     RLCCer Net     RLCCer Net     RLCCer Net     RLCCer Net     RLCCer Net     Some RLC     RLC's Net Length     CrostTak (Single-Ended)     JO View     Histogram     Save Results	Function at most of more front and more at more		02		View Only Active Layer	
Load Results Report Customize Workflow	۰ ۲۰۰۰ ا				Net Color O Layer Color     Net Color Manager	
Show or hide TCL Command pane	Mouse(mm): X: -5.	987, Y: 5.22		Ready		

2. Choose View > Pane > TCL Command to open the TCL command input console.

**3.** Copy the following TCL command to the **TCL Command** console.

sigrity::update PackageType -dieType {1} -bgaType {0} -attachType {3}

sigrity::update Circuits -dieCkts {D1} -boardCkts {BGA1} -wbCkts {D2}

sigrity::add Layer {bump} -above {Signal\$0353F408M1} -circuit {D1}

sigrity::add Layer {ball} -under {Signal\$0353F508BOTTOM} -circuit {BGA1}

sigrity::update Attributes -circuit {D1} -Dmax {0.12e-3} -D1 {0.10e-3} -D2 {0.10e-3} -HT {0.08e-3} -conductivity {5.0e+7}

sigrity::update Attributes -circuit {BGA1} -Dmax {0.4e-3} -D1 {0.35e-3} -D2 {0.35e-3} - HT {0.45e-3} -conductivity {5.2e+7}

sigrity::update ExtractionFreq {30e+6}

sigrity::update cpline -risetime {100} -percent {3} -all



4. Click the *Run* button in the TCL Command console.

The Package Setup is automated.

r		
XtractIM - Untitled - [2diestacked_fcw]	/b_newnl.spd Layer View]	_ 🗆 ×
💠 Workspace Edit View Mi	lode Setup Tools Window Help	cādence 💷 🛎 🗙
: 🗋 💕 🖬 🔹 🛯 🕨 🔳 🚦 💼	💼 🛃 🖲 🗇 🔿 🕤 🗇 🕼 🖉 🖓 🗸 🕅 💭 🖸 🚺 🔂 🔂 🔂 🔂 🚵 💁	• •
All Enabled Net(s) 👻 🖓 — 🕰	. ] 📥 🝸 • 🏛 📾 📧 🐨 🖕 X 🔤 💿 🕑 🕼 🔃 🗣 🕫 📼 🚥 🗮 🖗 🗄 🕂 🔿 🗶 🗛	- P 🗉 🗱 🙆 🖸
iai a		
Workflow: XtractIM	-8 -7 -8 - 7 -8 - 1 -2 -1 0 -1 -4 -3 -4 -5 -6 -7 -8 ▲ Laver Selection	×
Model Extraction		_
Manage Workspace	Signal 50353F408M1	
Load Workspace	Signal \$0353 # 508BOTTOM	
Load a New/Litterent Layout	signal02	
Package Setup	Signal03	
Package Type: Both		
✓ Circuits		
V Bumps		
🗸 Solder Ball		
✓ Nets		
Simulation Setup		
Module: IBIS/RLGC		
Simulation Type: Net-Based		
View/Export Results		
Summary		
SPICE Model		
Save Results		
Load Results		
Report	I CC commana X	
Customize Workflow ×		
	View Only Active Layer	
	- Display Geometry Objects By	
	• Net Color • Layer Color	
	Layer Selection Net Manager	
Ver: 13.0.a0.11113 (XtractIM)	Mouse(mm): X: 2.18, Y: 6.058 🥥 Ready	

The relationship between individual TCL command and the corresponding Package Setup is described as follows.

• sigrity::update PackageType -dieType {1} -bgaType {0} -attachType {3}



sigrity::update Circuits -dieCkts {D1} -boardCkts {BGA1} -wbCkts {D2}

ukt Name	Ckt Model	Die/Board/Componer Ckt Type	
D1	Die1	Die(FlipChip)	
D2	Die2	Die(WireBond)	
BGA1	untitled_pac	Board	

- sigrity::add Layer {bump} -above {Signal\$0353F408M1} -circuit {D1}
- sigrity::add Layer {ball} -under {Signal\$0353F508BOTTOM} -circuit {BGA1}

Layer Manager -> Stack Up 🛛 🗸 🗙											
Stack Up	Pad Sta	sk									
Layer #	Color	Layer Icon	Layer Name	Thickness(mm)	Material	Conductivity(S	Fill-in Dielectric	Permittivity	Loss Tangent	Shape Name	Trace \
1			Signal\$0353F488WBOND	0.001		5.95614e+007		[1]	[0]		0.1
			Medium\$0353F208dieletric1	0.3		0		4.2	0		
2			Signal01	0.001		5.8e+007		[2.6]	[0]		0.1
			Bump01	0.08		0		1	0		
3			Signal\$0353F408M1	0.03429		5.95614e+007		[2.6]	[0]	Shape\$035	0.1
			Medium\$0353F188dielectric2	0.1		0		4.2	0		
4			Signal\$0353F508BOTTOM	0.03429		5.95614e+007		[2.6]	[0]	Shape\$035	0.1
			Solderball01	0.45		0		1	0		
5			Signal02	0.001		5.8e+007		[2.5]	[0]		0.1
			Medium01	0.05		0		4	0		
6			Signal03	0.03556		5.95e+009		[1]	[0]	Shape001	0.1
4											
											P
Total Thick	ness: 1.0	871e+000 mm					En	force causality	View Mate	rial Im	port
Solder	Rall Laver	Rumpla	ver					where Au	to Cat Lawer Coo	rial Void Eilt	_
E- Solder	our cayer	C. Joamp La	10					AU	to set cayer spec		3
							Unit: mm	- OK	Can	cel A	pply

 sigrity::update Attributes -circuit {D1} -Dmax {0.12e-3} -D1 {0.10e-3} -D2 {0.10e-3} -HT {0.08e-3} -conductivity {5.0e+7}

Package Setup ->	ackage Setup -> Bumps X									
Layer Name	Circuit Name	Dmax (mm)	D1 (mm)	D2 (mm)	HT (mm)	Material	Conductivity (S/m)	D 1611		
Bump01	D1	0.12	0.1	0.1	0.08		5e7	Bump Model		
							•			
ОК	Cancel									

sigrity::update Attributes -circuit {BGA1} -Dmax {0.4e-3} -D1 {0.35e-3} -D2 {0.35e-3} -HT {0.45e-3} -conductivity {5.2e+7}

Package Setup ->	Solder Ball							×
Layer Name	Circuit Name	Dmax (mm)	D1 (mm)	D2 (mm)	HT (mm)	Material	Conductivity (S/m)	Solder Ball Model
Solderball01	BGA1	0.4	0.35	0.35	0.45		5.2e7	H→D2→H HT H→Dmax→HT H→Dickness 1 Ground
			111					
ОК	Cancel							

• sigrity::update ExtractionFreq {30e+6}

Extraction Frequency			×
Extraction Frequency:	30	MHz	ОК
			Cancel

• sigrity::update cpline -risetime {100} -percent {3} -all

Net N	Mana	ger				×
Net:				- 🔎 Show (	Coupled I	•
Netl	List (S	Fort enabled first) $ riangle$	%Coupling	Rise Time (ps)		1
E	2	Unnamed Net(s)	3	100		
	2	PowerNets	3	100		
	$\checkmark$	VDDcore				Ξ
	$\checkmark$	VDD_1				
	$\checkmark$	VDD_2				
	$\checkmark$	VDD_3				-
	$\checkmark$	VDD_4				
	2	🔀 GroundNets	3	100		
	$\checkmark$	VSS				
E	2	DEFAULT	3	100		
E	2	🖊 Net_1	3	100		
- E	2	🖊 Net_2	3	100		
- E	2	🖊 Net_3	3	100		
- E	2	🖊 Net_4	3	100		
5	2	🖊 Net_5	3	100		
6	2	🖊 Net_6	3	100		
6	2	🖊 Net_7	3	100		
<b>E</b>	2	🖊 Net_8	3	100		
<b>E</b>	2	🖊 Net_9	3	100		
<b>E</b>	2	🖊 Net_10	3	100		
<u> </u>	2	<mark>∕</mark> Net_11	3	100		
<b>E</b>	2	Net_12	3	100		
<u> </u>	2	🖊 Net_13	3	100		
<u> </u>	2	Net_14	3	100		
6	2	Net_15	3	100		
	2	Net_16	3	100		•
Ger	neral-					
⊻к	leep s	shape enabled when t	the net is disab	led		
<b>V</b> 6	Gray D	Disabled		Hide D	isabled	
Cou	upled	Lines				
	isable	e Coupled Line Simula	tion			
Cout	pled L	ines Report				
Laye	er Sel	ection Net Manage	er			

5. The TCL command used above can also be prepared in a .tcl file.

2_Stacked_fcwb.tcl - Notepad	x
Eile Edit Format View Help	
<pre>sigrity::update PackageType -dieType {1} -bgaType {0} -attachType {3} sigrity::update Circuits -dieCkts {D1} -boardCkts {BGA1} -wbCkts {D2} sigrity::add Layer {bump} -above {signal\$0335F4080M1} -circuit {D1} sigrity::add Layer {ball} -under {signal\$0335F50800TOM} -circuit {BGA1} sigrity::update Attributes -circuit {D1} -Dmax {0.12e-3} -D1 {0.10e-3} -D2 {0.10e-3} -HT {0.08e-3} -conductivity {5.0e+7} sigrity::update Attributes -circuit {BGA1} -Dmax {0.4e-3} -D1 {0.35e-3} -D2 {0.35e-3} -HT {0.45e-3} -conductivity {5.2e+7} sigrity::update Attributes -circuit {0} -Dmax {0.4e-3} -D1 {0.35e-3} -D2 {0.35e-3} -HT {0.45e-3} -conductivity {5.2e+7} sigrity::update cpline -risetime {100} -percent {3} -all</pre>	}
	-
	►

6. Click the Open a TCL file icon to load the prepared \*.tcl file.



7. Click the Play TCL icon to run the prepared TCL command.

) 📴 💁 🕒 😐		
	Play TCL	🕢 🕑 🐼 🚺 📃

The same result will come out as in *Step 4*.

## **Stacked-BGA Package Sample**

1. Load *pop\_flipchip.spd*.

It is typically located in <ASI\_INSTALL\_DIR>\Update3\SpeedXP\Samples\XtractIM\Single-Die\_Sample\_files\.

A flipchip BGA package is placed above a flipchip BGA package.



2. Choose View > Pane > TCL Command to open the TCL command input console.



Copy the following TCL command to the TCL Command console.
 sigrity::update PackageType -dieType {0} -bgaType {1} -attachType {1}
 sigrity::update Circuits -dieCkts {U1} -boardCkts {POPtop} -boardCkts {POPbottom}

sigrity::add Layer {bump} -above {Signal\$136C4D70M1} -circuit {U1}

sigrity::add Layer {ball} -above {Signal\$136C4D70M1} -circuit {POPtop}

sigrity::add Layer {ball} -under {Signal\$136C4EF0M4} -circuit {POPbottom}

sigrity::update Attributes -circuit {U1} -Dmax {0.12e-3} -D1 {0.10e-3} -D2 {0.10e-3} -HT {0.08e-3} -conductivity {5.0e+7}

sigrity::update Attributes -circuit {POPbottom} -Dmax {0.4e-3} -D1 {0.35e-3} -D2 {0.35e-3} -HT {0.45e-3} -conductivity {5.2e+7}

sigrity::update Attributes -circuit {POPtop} -Dmax {0.42e-3} -D1 {0.36e-3} -D2 {0.36e-3} -HT {0.3e-3} -conductivity {5.6e+7}

sigrity::update ExtractionFreq {30e+6}

sigrity::update cpline -risetime {100} -percent {3} -all

TCL Command	×
1	
sprity::update Attributes surcut (POPtep)-Dmax (0.42e-3) -D1 (0.36e-3) -D2 (0.36e-3) +fT (0.3e-3) -conductivity (5.6e+7)	Run

4. Click the *Run* button in the TCL Command console.

The Package Setup is automated.



The relationship between individual TCL command and the corresponding Package Setup is described as follows.

sigrity::update PackageType -dieType {0} -bgaType {1} -attachType {1}

• Single Die	O Stacked Die	O Side-by-side Die
O Single BGA	• Stacked BGA	OLeadframe
O Wirebond	Flip-Chip     (WL-CSP)	OBoth
ОК	Cancel	

 sigrity::update Circuits -dieCkts {U1} -boardCkts {POPtop} -boardCkts {POPbottom}

C1         Cap0402         Cap0402           C2         Cap0402         Cap0402           C3         Cap0402         Cap0402           C4         Cap0402         Cap0402           C5         Cap0402         Cap0402           C6         Cap0402         Cap0402           C7         Cap0402         Cap0402           C8         Cap0402         Cap0402           U1         FC         Die           POPbottom         POP bot         Board	exchouse exchouse	Ckt Type
C2     Cap0402       C3     Cap0402       C4     Cap0402       C5     Cap0402       C6     Cap0402       C7     Cap0402       C8     Cap0402       U1     FC       POPbottom     POP bot	C1 Cap0402	
C3     Cap0402       C4     Cap0402       C5     Cap0402       C6     Cap0402       C7     Cap0402       C8     Cap0402       U1     FC       POPbottom     POP bot	C2 Cap0402	
C4         Cap0402           C5         Cap0402           C6         Cap0402           C7         Cap0402           C8         Cap0402           U1         FC         Die           POPbottom         POP bot         Board	C3 Cap0402	
C5         Cap0402           C6         Cap0402           C7         Cap0402           C8         Cap0402           U1         FC         Die           POPbottom         POP bot         Board	C4 Cap0402	
C6         Cap0402           C7         Cap0402           C8         Cap0402           U1         FC         Die           POPbottom         POP bot         Board	C5 Cap0402	
C7         Cap0402           C8         Cap0402           U1         FC         Die           POPbottom         POP bot         Board	C6 Cap0402	
C8         Cap0402           U1         FC         Die           POPbottom         POP bot         Board	C7 Cap0402	
U1         FC         Die           POPbottom         POP bot         Board	C8 Cap0402	
POPbottom POP bot Board	J1 FC	Die
-	POPbottom POP_bot	Board
POPtop POP_top Board	POPtop POP_top	Board

- sigrity::add Layer {bump} -above {Signal\$136C4D70M1} -circuit {U1}
- sigrity::add Layer {ball} -above {Signal\$136C4D70M1} -circuit {POPtop}
- sigrity::add Layer {ball} -under {Signal\$136C4EF0M4} -circuit {POPbottom}

ayer Mana	ager -> Sta	ack Up								0	X
Stack Up	Pad Stad	:k									
Layer #	Color	Layer Icon	Layer Name	Thickness(	Material	Conductivity(S	Fill-in Dielectric	Permittivity	Loss Tangent	Shape Name	Trace W
1			Signal03	0.03556		5.95e+009		[1]	[0]		0.1
			Medium01	0.05							
2		TE	Signal02	0.001 <b>{b</b> :	all} -above {Sig	nal\$136C4D7	OM1} -circuit {	POPtop}	0]		0.1
			Solderball01	0.219	_			-			
3			Signal01	0.001		5.8e+007		[1]	[0]		0.1
			Bump01	(human) al	have (Signals)	2604070841	ainauit (114)		0		
4			Signal\$136C4D70M1	{bump} -a	bove (signals i	30040701013	-circuit {01}		[0]		0.1
			Medium\$136C4870D2	0.125		0		4.2	0		
5			Signal\$136C4DF0VSS	0.015		1.81429e+006		[4.2]	[0]	Shape\$136	0.1
			Medium\$136C4AF0D3	0.125		0		4.2	0		
6			Signal\$136C4E70VDD	0.02		1.81429e+006		[4.2]	[0]	Shape\$136	0.1
			Medium\$12F371E8D4	0.125		0		4.2	0		
7			Signal\$136C4EF0M4	0.015		1.81429e+006		[2.6]	[0]		0.1
			Solderball02	_		-		_	0		
8			Signal04	{ball}-unde	er {Signal\$136	C4EF0M4} -cir	cuit (POPbotte	om}	[0]		0.1
			Medium02					_	0		
9			Signal05	0.03556		5.95e+009		[1]	[0]	Shape001	0.1
<			111								•
Total Thid	merer 1 3	631e±000 mm					Enf	ince causality	View Mate	rial Im	wrt
								orec cousoncy			
Solder	bai Layer	Bump Lay	/er				E	xport Au	to Set Layer Spec	cial Void Filb	sr
							Units and	-	C	col A	naly
							Unit: mm	T UK	Can	UCI A	hhuà

 sigrity::update Attributes -circuit {U1} -Dmax {0.12e-3} -D1 {0.10e-3} -D2 {0.10e-3} -HT {0.08e-3} -conductivity {5.0e+7}



- sigrity::update Attributes -circuit {POPbottom} -Dmax {0.4e-3} -D1 {0.35e-3} -D2 {0.35e-3} -HT {0.45e-3} -conductivity {5.2e+7}
- sigrity::update Attributes -circuit {POPtop} -Dmax {0.42e-3} -D1 {0.36e-3} -D2 {0.36e-3} -HT {0.3e-3} -conductivity {5.6e+7}

Package Setup ->	Solder Ball							×
Layer Name	Circuit Name	Dmax (mm)	D1 (mm)	D2 (mm)	HT (mm)	Material	Conductivity (S/m)	Solder Ball Model
Solderball02 Solderball01	POPbottom POPtop	0.4 0.42	0.35	0.35	0.45		5.2e7 5.6e7	← Dmax → HT ← Dmax → HT ← D1 → HT Medium Thickness
•			111					
ОК	Cancel							

sigrity::update ExtractionFreq {30e+6}

		~
30	MHz	ОК
		Cancel
	30	30 MHz

sigrity::update cpline -risetime {100} -percent {3} –all

d first) / %Cc ed Nets 3 Nets 3 Dcore / 1 / / 2 / / 3 / 4	P Shoupping Rise Time (     100     100	ps)
d first) ∕ %Cc ed Net(s) 3 Nets 3 Docore )_1 )_2 )_3 )_4 Nets 3	Dupling Rise Time ( 100 100	ps)
and Net(s)         3           Nets         3           Ocore         -           0_1         -           0_2         -           0_3         -           0_4         Whete	100 100	=
Nets         3           Ocore         -           0_1         -           0_2         -           0_3         -           0_4         -	100	=
Decore         Image: Constraint of the second		=
0_1 0_2 0_3 0_4 Nets 3		
0_2 0_3 0_4		
)_3 )_4		
)_4		
Note 3		
110CG 3	100	
1		
LT 3	100	
3	100	
3	100	
3	100	
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3	100	
3	100	
3	100	
3	100	
) 3	100	
3	100	
2 3	100	
3 3	100	
3	100	
i 3	100	
i <b>3</b>	100	
	LT 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	LT 3 100 3 100 5 3

5. The TCL command used above can also be prepared as a .tcl file.

PoP_FC.tcl - Notepad	×
File Edit Format View Help	
<pre>sigrity::update PackageType -dieType {0} -bgaType {1} -attachType {1} sigrity::update circuits -dieckts {U1} -boardckts {PoPbotp} -boardckts {PoPbottom} sigrity::add Layer {bump} -above {signal\$I36c4070M1} -circuit {U1} sigrity::add Layer {ball} -above {signal\$I36c4070M1} -circuit {PoPbotp} sigrity::add Layer {ball} -above {signal\$I36c4070M1} -circuit {PoPbotp} sigrity::add Layer {ball} -above {signal\$I36c4070M1} -circuit {PoPbotp} sigrity::update attributes -circuit {0} -bomax {0.12e-3} -D1 {0.10e-3} -HT {0.08e-3} -conductivity {5.0e+7} sigrity::update attributes -circuit {00} -bomax {0.42e-3} -D1 {0.35e-3} -D2 {0.35e-3} -HT {0.45e-3} -conductivity {5.0e+7} sigrity::update attributes -circuit {00Pbottom} -bmax {0.42e-3} -D1 {0.35e-3} -D2 {0.36e-3} -HT {0.3e-3} -conductivity {5.6e+7} sigrity::update extractionFreq {30e+6} sigrity::update extractionFreq {30e+6</pre>	*
	~
	►

6. Click the Open a TCL file icon to load in the prepared \*.tcl file.

	-	B ×
	cādence	_ 8 ×
Open a TCL file 🗸 🔎 🔤 🗱 🛃 🛃		

7. Click the **Play TCL** icon to run the prepared TCL command.



This same result will come out as in Step 4.

# **LESSON Two: TCL COMMAND RECORDING SUPPORT FOR WORKSPACE SETUP**

In this lesson, the TCL recording function for XtractIM workflow setup is introduced for preparing a reusable TCL file.

### **Load Design**

**1.** Load a sample spd file.

flipchip.spd is used as sample case in this tutorial. It is by default located at <INSTALL\_DIR>\Update4\SpeedXP\Samples\XtractIM\Single-Die\_Sample\_files\.



2. Remove existing bump and solder ball layers before running TCL recoding command.

Layer Manag	ger -> Sta	ck Up											□ ×
Stack Up	Pad Stac	k											
Layer #	Color	Layer Icon	Layer Name	Thickness(	Material	Conductivity(S	Fill-in Dielectric	Permittivity	Loss Tangent	Shape Name	Trace Width(mm)	Trapezoidal Angle(°)	Roughness(mm)
1			Signal02			ie+007					0.1		
			Bump01	0.1		þ		4	0				
2			Signal\$M1	0.015		5.8e+007		[4.1]	[0]		0.1	90	0
			Medium\$dielectric2	0.125		0		4.2	0				
3			Signal\$VDD	0.02		5.8e+007		[4.2]	[0]	Shape\$VDD	0.1	90	0
			Medium\$dielectric3	0.25		0		4.2	0				
4			Signal\$VSS	0.02		5.8e+007		[4.2]	[0]	Shape\$VSS	0.1	90	0
			Medium\$dielectric4	0.125		0		4.2	0				
5			Signal\$M4	0.015		5.8e+007		[2.6]	[0]		0.1	90	0
			Solderball01	0.4		0		1	0				
6			Signal01	0.001		5.8e+007		[2.5]	[0]		0.1	90	0
			Medium01	0.05		0		4	0				
4					111								•
Total Thickr	ness: 1.13 Ball Layer	:60e +000 mm	1	Right-click on	a dielectric(or signal)	layer to insert a sol	der ball layer.				Enforce causalit	y View Material uto Set Layer Special Vo	id Filter
										Unit:	mm 🔻 O	Cancel	Apply

3. Click OK.

<b>m</b> i <u>a</u> i				1 1
The Stee	7110 10	cotun	00	bolow
THE MAC	K I I I I I N	Senn	28	
I IIC Diuc	Kup 15	Secup	uo	0010

Layer Mana	ger -> St	ack Up									0	x
Stack Up	Pad Sta	ck										
Layer #	Color	Layer Icon	Layer Name	Thickness(	Material	Conductivity(S	Fill-in Dielectric	Permittivity	Loss Tangent	Shape Name	Trace Width(mm)	Trapez
1			Signal\$M1	0.015		5.8e+007		[1]	[0]		0.1	90
			Medium\$dielectric2	0.125		0		4.2	0			
2			Signal\$VDD	0.02		5.8e+007		[4.2]	[0]	Shape\$VDD	0.1	90
			Medium\$dielectric3	0.25		0		4.2	0			
3			Signal\$VSS	0.02		5.8e+007		[4.2]	[0]	Shape\$VSS	0.1	90
			Medium\$dielectric4	0.125		0		4.2	0			
4			Signal\$M4	0.015		5.8e+007		[1]	[0]		0.1	90
< [				111								
Total Thick	ness: 5.7	000e-001 mm							Enforce causali	ty View M	laterial Imp	port
Solder I	Ball Layer			Right-dick on	a dielectric(or signa	l) layer to insert a sol	der ball layer.		Export	Auto Set Layer S	Special Void Filte	er
-								Unit:	m 🔻 (	ж	Cancel	poly

4. Save the clean spd file to the working directory.



## **Record TCL Command for Workspace Setup**



1. Choose View > Pane > TCL Reader.

2. Click the Record TCL button.



**3.** Set up the workflow as usual.



The used TCL command will be written in the TCL reader.

4. Click the Stop button to stop TCL recording.

XtractIM - Untit	led - [tli	pchip.spd	Layer Vie	N]						
🔶 Workspace	Edit	View	Mode	Setup	Tools	Window	Help			
i 🗋 💕 🛃 🕶 🗌			···· 😐	<i>C</i> •	- •	0 @ @		🕐 🖓 🕼 💌 🔹 💭 💭 🚺 🚺 Extractor Result 💿 🖬 👘 👘 👘 🚱 🚱 🗤	<b>.</b>	
All Enabled Net(s	)	0-	n I	- T	• := •••	9 <b>1</b> 🔊	😭 🌬	× 🐚 🗶 🖲 🕒 🞯 🕻 🗓 📴 🐂 🖷 📼 💷 🗮 🗄 🖓 💾 🔿 🔊 🗛	Stop &	100
Workflow: XtractIN	1		×	20000	-18000	-16000	-14000	_12000 _10000 _8000 _6000 _4000 _2000 _0 _2000 _4000 _6000	8000	100

5. Click the Save TCL button to save the TCL command to a file for reuse.

AtractiM - Untitled - [flipchip.spd	Layer View]			
🗇 Workspace Edit View	Mode Setup	Tools Windo	w Help	_
🗋 💕 🔒 🔹 🗊 🕨 🔳 📳	🚥 💼 🙆 🗉		e ge	🛿 🕐 🖓 🐨 🕫 💌 👘 💭 💭 💭 🞑 🗄 Extractor Result 🔤 👘 👘 👘 🖄 🖄 🚱 📦 🗼 🔍 💷 👘 👘 👘
All Enabled Net(s) 🔽 🖓 🗕	🔨 i 📥 Ŧ	• = • 91	rs 😭 🌬	+ X 🕼 2월, 🗿 🕒 🮯 🖸 📴 🦮 🕷 📼 🚥 🗮 🗄 🕸 🔣 🏹 🕼 🖉 🖉 🖪
Workflow: XtractIM	× 20000	-18000 -1600	-14000	) <u>-12000 -10000 8000 -8000 4000 -2000 0 2000 4000 8000 8000 10000 12000 14000</u>

🔄 flipchip.tcl - Notepad
File Edit Format View Help
sigrity::update PackageType -d {0} -b {0} -a {1} {!} sigrity::update Circuits -d {U1} -b {BGA1} {!} sigrity::add Layer {bump} -above {Signal\$M1} -circuit {U1} {!} sigrity::add Layer {ball} -under {Signal\$M4} -circuit {BGA1} {!}

# Chapter

# **Network Parameter Viewer**

This chapter takes you through the steps to use the XtractIM tool to view Network Parameter with both BNP and Touchstone files.

# LOAD BNP / TOUCHSTONE FILES

- **1.** Launch XtractIM.
- **2.** Click the **New** button on the toolbar.
- **3.** To open new Network Parameter Display, choose

View > Open New Network Parameter Display.

The Network Parameters pane appears.



4. Choose

File > Open

or right-click in the upper left pane.

- 5. Select Load from the Context menu.
- 6. Select the network parameter files to be loaded.

Multiple BNP/ Touchstone files can be opened at the same time. Once a file is loaded successfully, there is a new entry of the Network Parameter Matrix added to the Matrix pane.

7. Click on the **Open** button.

By default the diagonal elements of the matrix are shown. The corresponding frequency curves are displayed in the Curve pane. A unique ID is assigned to the matrix and its elements, followed by a customizable display names.

The icon denotes a matrix corresponding to a Touchstone file while the icon denotes a matrix corresponding to a BNP file.

### **Select Matrix Elements**

- 1. Select one or more parameter matrices.
- 2. Select

View > Select Matrix Elements

or right click on a selected matrix.

**3.** From the context menu select

Select Matrix Elements

The Matrix Element Selection dialog appears.

- 4. From the drop-down box choose from the pre-defined patterns.
  - Diagonal
  - Full Matrix
  - Lower Triangular Matrix
  - Sub Matrix
  - Upper Triangular Matrix

The **Sub Matrix** option is not available if more than one matrix is selected and the dimensions are different

5. If Sub Matrix is selected, enter the row and column numbers in the input boxes;

6. Click the Replace button to replace the existing displayed curves with the selections;

or click the Add button to add the selected curves to the existing list.

SubMatrix Setting		
Rows		e
Columns		Ð
Note:		
The matrix dimension is: 1		
Click the icons on the right to sele indices in the box. Example: 1, 3,	et rows or columns, or en 5-8. Empty input assume	ter the port s all rows or

## **Hide / Show Matrix Elements**

- **1.** Single-click on the color icon in front of a matrix element to trigger the visibility; or select multiple matrices or matrix elements.
- 2. Select

View > Show/Hide Curves

or right-click on a selected matrix or curve.

3. Select

Show/Hide Curves

4. Choose from the available Visibility Control options.

## **Delete Matrix Elements**

- 1. Select one or more matrix elements.
- 2. Select

View > Delete Selected Curves

or right-click on the selection.

3. Select

**Delete Selected Curves** 

or press the Delete key.

## **Unload Networks**

- 1. Select one or more matrices.
- 2. Select

File > Unload Network

or right-click on the selection.

- To remove the selection from the Matrix pane select Unload Network
- 4. To remove all the loaded networks select

**Unload All Networks** 

The simulation result cannot be unloaded.

# **SAVE BNP / TOUCHSTONE FILES**

## Save a Modified Network

A network can be modified by editing the comments of the file, or by performing matrix operations such as re-normalization or frequency truncation, etc. When a network is modified, a star is added to the icon before the matrix entry. To save the modification follow these steps.

- **1.** Select a matrix entry that has been modified.
- 2. Select

File > Save

or right-click on the selected matrix.

3. Select Save from the context menu.

The modified information is saved into the original file, over-writing its contents with the exact same settings of the file.

## **Save Network as Another File**

- 1. Select a matrix.
- 2. Select

File > Save As

or right-click on the selection.

3. Select

Save As

In the Save Curves dialog, follow the same steps as in saving the simulation result

This feature allows you to convert between the BNP and Touchstone formats. Some of the information in the BNP file (such as AFS compression) is not supported by the Touchstone format.

If you save a BNP file with AFS compression into a Touchstone file, the matrices at discrete frequency samples is saved.

#### Export the Curves to Other Format

1. To save the screen shot of the curve window into a BMP file or PNG file select

File > Export to Image File

- **2.** Select a matrix.
- **3.** To save the displayed curves into a Excel .csv file select

File > Export To Excel

## **View Network Properties**

- **1.** Select a matrix entry.
- 2. Select

View > Property

or right-click on the selection.

3. Select Properties from the context menu.

The **Network Property** dialog allows you to view various information of the network. You can edit the comments in the dialog.

- Data Types
- Design Information
- Differential Pair Setup
- Port Setup
- Sampling Frequencies
- User Comments

## **CUSTOMIZE THE NETWORK AND ELEMENT DISPLAY NAME**

- 1. Select one or more matrix entries.
- 2. Select

View > Name Display > Customize

or right-click on the selection.

3. From the context menu select

Name Display > Customize

**4.** Check the appropriate fields you want to include in the network name, matrix element name and curve legend.

Examples of the element name and the curve legend are displayed as you change the settings.

5. Click **OK** to apply the setting to the selected matrices;

or, to apply the setting to all matrices, select

Save as Default

The default settings are saved into the registry and used for the networks loaded in the future.

- 6. In additional to the default names, the display names can also be modified. Select an entry.
- 7. Select

View > Name Display > Rename

or right-click on the selection.

- **8.** From the context menu select
  - Name Display > Rename

You can then edit the name to any string. You can switch back to the default name.

9. From the View or Context menu, select

Name Display > Default Name

Di	splay Name Opti	ons					×
	Network Name Path Name File Extension						
	Element Name						
	Matrix Type	🗹 Port Nan	ne 🔽 P	ort Number	💌 Ne	et Name	
	Example: 50[1,1] - S(1:P	Port1::VCC, 1:	Port1::VCC)				
	Tip:						
	Select "Differentia Otherwise, to sho normal style: Matr	l Channel Styl w matrix elem ix type, Port r	e" to show m ent name wit name, Port n	atrix element h long type o umber, Net na	name v ompose ame.	iith short type; d by four options in	
	The "Differential C and differential vi matrices of mix mo	Thannel Style" ew. The four ode in normal	is only used options are u style.	for mix mode sed for single	matrice ended	s in both normal vie matrix and the two	ew
	In all, it's not allo	wed to clear t	he four optio	ns all.			
	-Curve Legend Nan	ne					
	(Empty)	<b>-</b>	(Empty)	-	-	Element Name	-
	Example:						
	S(1:Port1::VCC,	1:Port1::VCC)	I				
	Se	et As Default		ок		ancel	

# **ADVANCED MATRIX OPERATIONS**

**Copy Network** 

- **1.** Select one or more matrices.
- 2. Select

Operation > Copy

or right-click on the selection.

**3.** Select **Copy** from the context menu. When a network is copied, a new network is created. A matrix entry is added to the matrix pane.

The status of this network is set to **modified**. It is not saved to the hard drive until you manually save it.

## **Network Re-normalization**

- **1.** Select a network in the Matrix pane.
- 2. Select

Operation > Re-normalize

or right-click on the selection.

**3.** From the Context menu select

Matrix Operation > Re-normalize

The Change Port Setting dialog appears.

- 4. To edit the reference impedance of a single port select the line and click on the impedance value.
- **5.** To change several ports at the same time, select multiple ports. A reference impedance input box appears.
- 6. Click OK to apply the changes. The S parameter curves are updated. The matrix is marked as modified.

No.	Port Name	Ref Impedance
<b>P</b> 1	Port1_die_1::VDD25	50.00000
<b>P</b> 2	Port2_die_6::VDD125	50.00000
<b>P</b> 3	Port3_die_3::DATA1	50.000000
<b>P</b> 4	Port4_die_4::DATA2	50.000000
<b>P</b> 5	Port5_BGA::VDD25	50.000000
<b>P</b> 6	Port6_BGA::VDD125	50.000000
<b>P</b> 7	Port7_BGA_1::DATA1	50.000000
<b>P</b> 8	Port8_BGA_2::DATA2	50.00000

## **Port Reduction**

- **1.** Select a network in the matrix pane.
- 2. Select

Operation > Reduction

or right-click on the selection.

**3.** From the context menu select

Matrix Operations > Reduction

The Change Port Setting dialog appears.

- 4. To change the status of a single port by select the line. Each port has 4 connection settings:
  - Match
  - Open
  - Remain as a Port
  - Short
- 5. Click on its connection status or select multiple ports.
- 6. Change their status together in the combo box at the bottom of the window.
- 7. Click **OK** to perform port reduction. The result is a new network added to the matrix pane. The network parameters are not saved to the hard drive until you manually perform a **Save**.

Note!	A BNP file with AFS compression cannot be reduced directly, since the AFS compression information in the original matrix is not necessarily valid for the reduced matrix. A warning message is shown. The matrix is converted into a discretely sampled format.
-------	---

No.	Port Name	Port Connection Status
<b>P</b> 1	Port1_die_1::VDD25	Matched
<b>P</b> 2	Port2_die_6::VDD125	Matched
<b>P</b> 3	Port3_die_3::DATA1	Port
<b>P</b> 4	Port4_die_4::DATA2	Port
<b>P</b> 5	Port5_BGA::VDD25	Open
<b>P</b> 6	Port6_BGA::VDD125	Open
<b>P</b> 7	Port7_BGA_1::DATA1	Port
<b>P</b> 8	Port8_BGA_2::DATA2	Port
#### **Passivity Enforcement**

- **1.** Select a network in the Matrix pane.
- 2. Select

Operation > Passivity Enforce

or right-click on the selection.

**3.** From the Context menu select

Matrix Operations > Passivity Enforce

A new network with passivity enforcement at each sampling frequency is generated.

**NOTE!** Passivity enforcement is not available for BNP files with AFS compression.

# **Edit the Differential Pairs**

A differential pair is defined with two nets. Pairs of differential ports can be defined under each differential pair. The differential pair and differential port information can be defined in PowerSI before the simulation and can be modified in the network parameter display.

- 1. Select a network in the matrix pane.
- 2. Select

**Operation > Redefine Differential Port** 

or right-click on the selection.

**3.** From the context menu select

Matrix Operations > Redefine Differential Port

The Define Differential Ports dialog appears.

- 4. To remove an existing definition, select a pair of nets or a pair of ports.
- 5. Click the Delete button.
- 6. To add a new pair, select a pair of nets from the net combo boxes.
- 7. Select a pair of ports from the port combo boxes.
- 8. Click Add Pair to create the differential ports.
- 9. Click OK to apply the changes. The mixed-mode network parameters are updated.

	Differential Pair	Positive Net/Po	ort	Negative Net/Port		
6	Diff_Channel_DATA1_\$_DATA2	DATA1	DATA2			
		Port3_die_3 Port7_BGA_1		Port4_die_4 Port8_BGA_2		
-						
Add	Differential Pair					
Sel	ect Positive Net:		Select Negative	Net:		
Sel DA	ect Positive Net: TA1	-	Select Negative DATA2	Net:	•	
Sel DA Sel	ect Positive Net: TA1 ect Positive Net Port:	•	Select Negative DATA2 Select Negative	Net: Net Port:	•	
Sel DA Sel	ect Positive Net: TA1 ect Positive Net Port:	• •	Select Negative DATA2 Select Negative	Net: Net Port:	•	
Sel DA Sel	ect Positive Net: TA1 ect Positive Net Port:	•	Select Negative DATA2 Select Negative	Net: Net Port:	↓ ↓	
Sel DA Sel	ect Positive Net: .TA1 ect Positive Net Port:	•	Select Negative DATA2 Select Negative	Net: Net Port:	• Add Pair	
Sel DA	ect Positive Net: .TA1 ect Positive Net Port:	•	Select Negative DATA2 Select Negative	Net: Net Port:	▼ Add Pair	
Sel	ect Positive Net: .TA1 ect Positive Net Port:	•	Select Negative DATA2 Select Negative	Net: Net Port:	Add Pair	
Sel DA Sel	ect Positive Net: .TA1 ect Positive Net Port: define differential pairs, please select prets are candidates of the d one port belong to the positive net and	two nets as pos liff ports. A pair o l the other belon	Select Negative DATA2 Select Negative	Net: Net Port: A n the diff pair. Ports belong ified as differential port if:	Add Pair to these	

# **Redefine Mixed Mode Port**

- **1.** Select a network in the matrix pane.
- 2. Select

Operation > Redefine Mixed Mode Port or right-click on the selection.

**3.** From the context menu select

Matrix Operations > Redefine Mixed Mode Port

The Define Mixed Mode Port dialog appears.

De	efine Mixed Mode Port	х
		_
	Order of Mixed Mode Port	
	51	
	52	
	53	
	54	
		_
		_
		-
	Mix Port Up Down OK Cancel	

- 4. Hold down CTRL key and select two ports.
- 5. Click Mix Port to generate new mixed S-parameter.
- 6. Click Ok to apply changes.

The mixed-mode network parameters are updated.

# SHOW NETWORK PARAMETERS VIA CHANNEL FILTER

- **1.** Select a matrix.
- 2. Click

View > Channel Filter



or select the pop-up menu

## Channel Filter

-

<u> </u>	Property
	Merge Network Parameters
	UnLoad Network
	UnLoad All Networks
	Сору
	Show/Hide Curves
	Name Display 🔹 🕨
	Show Insertion Loss
	Show Return Loss
	Select Matrix Elements
	Channel Filter
	Delete Selected Curves
	Calc Curves by Expression
	View Available Parameters 🔸
	Frequency Truncation
	Frequency Resampling
	Matrix Operations
2	Load
	Save
	Save As
	Export To Excel

If no network matrix is selected, the Channel Filter menu or toolbar button appears gray.

- 3. A Channel Filter dialog appears.
  - For every network, there are 3 views of the matrices items.
  - It depends on the port setting and different channel setting.
  - If there is no different channel setting defined in a network, there is only one view of a single channel matrix.

# **Port Setting Example**

Mo					
NU.	Port Name	Net Name	Ref Impedance		
1	Port1	VCC	5.000000e+		
2	Port2	D2	5.000000e+		
3	Port3	D2	5.000000e+		
4	Port4	D3	5.000000e+		
5	Port5	D3	5.000000e+		
6	Port6	D4	5.000000e+		
7	Port7	D4	5.000000e+		
8	Port8	D5	5.000000e+		
9	Port9	D5	5.000000e+		
10	Port10	VCC	5.000000e+		
				577	
	1 2 3 4 5 6 7 8 9 10	1       Port1         2       Port2         3       Port3         4       Port4         5       Port5         6       Port6         7       Port7         8       Port9         10       Port10	1     Port1     VCC       2     Port2     D2       3     Port3     D2       4     Port4     D3       5     Port5     D3       6     Port6     D4       7     Port7     D4       8     Port9     D5       10     Port10     VCC	1       Port1       VCC       5.000000e+         2       Port2       D2       5.000000e+         3       Port3       D2       5.000000e+         4       Port4       D3       5.000000e+         5       Port5       D3       5.000000e+         6       Port6       D4       5.000000e+         7       Port7       D4       5.000000e+         8       Port8       D5       5.000000e+         9       Port9       D5       5.000000e+         10       Port10       VCC       5.000000e+         9       Port10       VCC       5.000000e+         9       Port9       D5       5.000000e+         9       Port10       VCC       5.000000e+         9       Port10       VCC       5.000000e+         9       Port10       VCC       5.000000e+	1       Port1       VCC       5.000000e+         2       Port2       D2       5.000000e+         3       Port3       D2       5.000000e+         4       Port4       D3       5.000000e+         5       Port5       D3       5.000000e+         6       Port6       D4       5.000000e+         7       Port7       D4       5.000000e+         8       Port8       D5       5.000000e+         9       Port9       D5       5.000000e+         10       Port10       VCC       5.000000e+         -       -       -       -         -       -       -       -         -       -       -       -         -       -       -       -         -       -       -       -         -       -       -       -         -       -       -       -         -       -       -       -         -       -       -       -         -       -       -       -         -       -       -       -         -       <

# **Differential Port Setting Dialog**

neral Info	1	Diff_Channel_D4_\$_D5	D4	D5	
<u> </u>			Port6	Port8	
			Port7	Port9	
	2	Diff_Channel_D2_\$_D3	D2	D3	
			Port2 Port2	Port4	
3/			FOIG	FOIG	
unan arr Infa					
frency muo					
ort Info					
	121				
'ort Info					

There are three Channel Filter dialogs.

- Mixed Mode Matrix in Differential Channel View.
- Mixed Mode Matrix in Normal View.
- Single Channel Matrix in Normal View.

# Single Channel Matrix in Normal View

Channel Filter		×
All Channels		
Channel	Ports in Channel	Return Loss
✓ D4	2	Insertion Loss
☑ D5	2	Crosstalk
✓ D2	2	
☑ D3	2	
VCC	2	
		UN OK
		Cancel

## Mixed Mode Matrix in Normal View

All Channels			
Channel	Ports in Channel	Return Loss	
✓ D4<>D5	4	Insertion Loss	
🔽 D2<>D3	4	Crosstalk	
VCC	2		

**Mixed Mode Matrix in Differential Channel View** 

The dialog below lists all the channels in current matrix. Users can select the channels in the list by a multiple-select method. To select all channels select

All Channels		
Channel Filter		×
All Channels		
Channel	Ports in Channel	Return Loss
✓ D4<>D5	4	✓ Insertion Loss
✓ D2<>D3	4	
		ОК
		Cancel

- Mixed Mode Network Parameters A channel is defined as all the port pairs in a differential net pair.
- Single-ended Network Parameters A channel is defined as all the ports in a net.

Once a channel is selected, all ports under this channel are selected. The sub-matrix corresponding to all the selected ports are used for further selection. The elements in the selected sub-matrix are divided into three categories:

- Crosstalk Rest of the elements.
- Insertion Loss Off diagonal elements whose two ports are in the same channel.
- Return Loss Diagonal elements.

The **Insertion Loss** and **Crosstalk** elements consider the elements in the lower triangular matrix. This dialog can remember last user's selection including:

- Channels
- Crosstalk
- Insertion Loss
- Return Loss
- 1. Select channels.
- 2. Check and uncheck the three options on the right side of the pane.
- 3. Click OK.

The displayed elements in the selected network should be replaced by the elements specified in the user selection.

#### New Organization of Mixed Mode Network Parameters

Mode Definitions under the mixed mode network matrix lists all port pairs of differential channel setting and single channel ports. Single channel ports are only listed in normal view.

This tree item is collapsed by default.

There are two pop-up menus. Use these menus to determine the sorting of the port pairs and single channel ports.

- Mode Definitions > Sort by Index (Default)
- Sort by Channel



Four curve views are available in the differential channel view pane.

- 1. Double-click in a curve view to maximize this curve view.
- 2. Double-click again to restore the size.
- 3. To restore the default layout of the four curve views click

View -> Reset Channel Views' Layout

4. Double-click in the differential channel view to maximize and restore a curve window.

Viev	<ul> <li>Operation</li> </ul>	Options	Windo
1	Property		
	View Availab	le Parameter	s 🕨
	Parameter View		•
	Matrix Type		+
	Curve View		+
	Reset Chann	iel Views' Lay	out
	Name Display	/	+

# VIEW MIXED-MODE NETWORK PARAMETERS

The mixed mode parameters can be viewed in the normal view with the single-ended network parameters or in the differential channel view, which shows only the differential channels. The two views can be toggled by selecting

View > Parameter View > Normal View

or

View > Parameter View > Differential Channel View

This can also be done with the combo box in the **Curve Settings** toolbar. If a loaded network contains differential pair definitions, but the mixed-mode network parameters are not displayed.

- **1.** Select the matrix.
- 2. Select

View > View Available Parameters

or right-click on the selection.

**3.** From the context menu select

View Available Parameters

4. Choose the desired view.

#### **Frequency Truncation**

- 1. Select a network from the Matrix pane.
- 2. Select

Operation > Frequency Truncation

or right-click on the selection.

3. From the context menu, select

Frequency Truncation

- 4. Select the frequencies that you want to remove.
- 5. Click **Truncate** to remove these frequencies.

- Frequency Truncation Setting × Frequency 300 Automatic Selection No. Freq Point ~ 1.000000e+007 Start 2.000000e+007 2 З 3.000000e+007 Every other: 4.000000e+007 4 5 5.000000e+007 6 6.000000e+007 **Reverse Selection** 7 7.000000e+007 8 8.000000e+007 9 9.000000e+007 10 1.000000e+008 1.100000e+008 11 12 1.200000e+008 13 1.300000e+008 14 1.400000e+008 15 1.500000e+008 Truncate 16 1.600000e+008 1.700000e+008 17 18 1.800000e+008 OK Cancel < 111 >
- 6. Click OK the accept the final frequency sampling. The display is updated.

#### **Frequency Re-sampling**

If the network parameters are saved in a BNP file with AFS compression, the sampling frequencies can be changed in the display.

- 1. Select a network in the matrix pane.
- 2. Select

Operation > Operation > Frequency Resampling

or right-click on the selection.

3. In the Context menu, select

Frequency Resampling

- 4. Right-click to select the frequency band. You can choose to:
  - Add a new band.
  - Delete the band.
  - Edit the ending frequency of the band.
  - Edit the starting frequency of the band.
- 5. Select a Sweeping Mode from the Automatic Output Sampling combo box.
- 6. Modify the sweeping information and click Return. The sampling with this band is updated.
- 7. Select a frequency from the list on the right. Right-click.
- 8. Edit the value or insert a frequency point above or below the selected frequency.
- 9. You can select multiples of some frequencies. Right-click.
- **10.** Remove them from the list.

**11.** Click **OK** the accept the change. The display curves id updated.

**NOTE!** The re-sampling is for display purpose. If you save the file in BNP format with AFS compression, the new sampling is not kept. To keep the new sampling, you can save the file in Touchstone format or discretely sampled BNP format.

equency	Bands: 1			Output Frequencies in 646		
and	Starting Freq.	Ending Freq.		No.	Freq Point	
	10 MHz			1	10 MHz	
	Add	d T		2	12 MHz	
	Edit	t Starting Freg.		З	14 MHz	
	-			4	16 MHz	
	Edit	Edit Ending Freq.			18 MHz	
	Del	ete		6	20 MHz	
				7	22 MHz	
				8	24 MHz	
				9	26 MHz	
				10	28 MHz	
				11	30 MHz	
				12	32 MHz	
				13	34 MHz	
utout from	quoncy etarting: 10 M	./IU>		14	36 MHz	
itout fre	quency starting: 10 h			15	38 MHz	
iiput ire	quency enuing: 3 GH	2		16	40 MHz	
				17	42 MHz	
Automat	ic Output Sampling-			18	44 MHz	
	na un Serence VII. Se			19	46 MHz	
Linear				20	48 MHz	
Linear				21	50 MHz	
				22	52 MHz	
Freq. Ind	rement:		MHz	23	54 MHz	
				24	56 MHz	
Points/D	ecade:			25	58 MHz	
				26	60 MHz	
				27	62 MHz	

# VIEW TOTAL CROSSTALK OF NETWORK PARAMETER

**NOTE!** Total Crosstalk View is only available on reloaded result, not for current simulated result.

To view Total Crosstalk View, select

View > Parameter View > Total Crosstalk View.

Or select Total Crosstalk View from the toolbar.

Total Crosstalk View Normal View Mixed Mode Differential Channel View Total Crosstalk View

The crosstalk result is displayed in the curve pane.



- Each curve shows the value of crosstalk from S[i,1] to S[i,n].
- The X axis shows the port number from 1 to n.
- The Y axis represents the S/Y/Z Parameter.
- To view the crosstalk at desired frequency, you can use the scroll bar or enter specific number at the right-bottom corner.

# **CURVE OPERATIONS**

#### Load / Save Isolated Curves in PowerSI

- 1. Right-click in the Isolated Curve pane.
- 2. Select Load from the Context menu.
- 3. Select the curves in the Isolated Curve pane to save the curves.
- 4. Right-click on the selection.
- 5. Select Save from the context menu.

### **View and Set Curve Properties**

- 1. Select one or more matrix elements or one or more isolated curves.
- 2. Select

View > Property

or right-click on the selected curves.

3. Select **Property** from the context menu.

urve Pattern	Property	×
Style:	Pattern: None	Width: 1
Mark: None	Mark Size:	Mark Interval: 1
Sample:		

- 4. You can edit the following properties in the Curve Property dialog:
  - Curve Color
  - Line Pattern
  - Line Style
  - Line Width
  - Marker Size
  - Marker Type
- 5. Click OK to accept the changes. The selected curves are updated in the Curve window.

# **Curve Pane Context Menu**

Right-click in the Curve window. A context menu appears.

	Save Simulation Result	
	Measure	
	Marker	
	Expression Calculator	
	Black Background	
	Embed-Ctrl Visibility	•
	Embed-Ctrl Position	•
	Ctrl Bar Position	•
	BarChart	
4	Auto Tip	
	Show X-axis in log scale	
	Show Y-axis in log scale	
	Hide Annotation	
	Add Annotation	

You can perform the following operations in this menu.

- Add Annotation Add a text string in the Curve window.
- Auto Tip Show / Hide the tip of the objects in the Curve window when moving the mouse.
- **Bar Chart** Toggle the plot style between a bar chart and a continuous line.
- Black / White Background Set the background of the curve window to be black or white.
- Ctrl Bar Position If a sub window is docked, change the position of the docking.
- Embed-Ctrl Position Toggle the sub windows between floating or docking.
- Embed-Ctrl Visibility Set the visibility of the sub windows (for example, the legend bar) in the display area.
- Marker Toggle the horizontal and vertical marker lines.
- Measure Toggle the horizontal and vertical measure lines.
- Show X-axis in Log Scale Toggle the X axis between log scale and linear scale.
- Show Y-axis in Log Scale Toggle the Y axis between log scale and linear scale, available only if the value type is set to Amplitude.

## **Copy Curve**

**Curve Copy** is a simple way to compare the network parameters of different types. The isolated curves are always the same regardless of the parameter matrix type.

- 1. Select one or more matrix elements, or one or more isolated curves.
- 2. Select

Operation > Copy

or right-click.

**3.** Select **Copy** from the context menu. The duplicates of the selected curves are added to the **Iso-lated Curve** pane.

#### **Curve Calculation**

1. Select

Operation > Expression Calculator

or right-click in the curve window.

2. In the context menu, select

**Expression Calculator** 

You can select the displayed curves or constants from the combo box and create a simple expression.

Expression Calcul	ator	×	
Operation		Simple Calculation	
S0[1,1]		▼ S0[1,1] ▼	
	ОК	Cancel	

In the **Expression Calculation mode**, you can enter an expression with the matrix element unique ID or the isolated curve names.

A unique curve name is required for the new curve, and a default name is provided. The matrix elements can be anything that is available; it is not limited to the displayed elements.

3. Click OK. The calculation result is added as a new isolated curve.

eration			
or a dort		Expression	Calculation
rve Expression	L/YO[1,1]	Name	Curve3
rve Expression	L/YO[1,1]	Name	Curve3

# **Expression Customization**

You can re-use an expression in future calculations.

- **1.** Create a curve using Expression Calculation.
- **2.** Select the calculated curve.
- **3.** Right-click on the selection.
- **4.** In the context menu, select

Use Expression

The Expression Manager is displayed.

You can edit the name and contents of the expressions for later user. The symbol **X** represents the curve in the calculation.

5. Click **OK** to save the list of expressions.

Ехр Ту	Exp Name	Exp Content		
Any Cu	Inductance_Open	1/X/Omega		
Any Cu	Inductance_Short	X/Omega		
		-		
<		111		
Add	Delete			
Auu				
			OK	Cancel

Use a Saved Expression

- 1. Select one or more matrix elements or one or more isolated curves.
- **2.** Right-click on the selection.
- **3.** From the context menu select

Calc Curves by Expression

- 4. In the Expression Manager select an expression.
- **5.** Click **OK**. The expression is applied to all the selected curves. The calculation result is shown as new curves.



The validity of the expression depends on the parameter matrix and the port terminations.

# SMITH CHART VIEW OF THE S PARAMETER

Select Smith Chart from the Curve Source combo box;

Smith Chart	-
S	
Z	
Y	
Smith Chart	

or select Smith Chart from the menu

	view = matrix Type = Or	
View	Operation Options	Window Help
	Property	
	View Available Parameters	Normal View
	Parameter View	
	Matrix Type	• S
	Curve View	▶ Z
	Name Display	• Y
	Show/Hide Curves	Smith Chart
	Select Matrix Elements	5, 7:
	Delete Selected Curves	7, 8:
	Curve View Options	D, 9: 0.9 ▶ =12:
-	Toolbar - Main	D12:
4	Toolbar - Curve Explorer	C12: 0.8
¥	Toolbar - Curve Settings	C11:

View > Matrix Type > Smith Chart

## **Overview**

Use the toolbar to view the Smith Chart.

- Enlarge Reduce X / Y-scale buttons are disabled.
- Curve Method Selection combo box is disabled.

( ( ( ( ( ( ( ( ( ( ( ( ( ( ( ( ( ( (	+ \$	\$ 4		XK		Normal View	•	Smith Chart	-	Amplitude	-
here and the second sec			 		ALL						



The Smith Chart in Normal view is shown in the following illustration.

#### **Differential Channel View**

The Smith Chart plot in Differential Channel View is shown in the following illustrations.

- The first set shows **Diff-Diff** and **Comm-Diff**.
- The second set shows **Diff-Comm** and **Comm-Comm**.





# **Manage the Curve View**

The default plot display an unit circle, grid lines and curves. If the unit circle can be seen entirely, the square disappears; otherwise, it appears.

# **Move by Pan**

- 1. Click the button
- **2.** Press the plot.
- **3.** Move to the desired position. Release the mouse button.



# **Zoom In and Out**

Use the mouse wheel in a valid area to **Zoom** in and out of the plot to see the interested area. The grid line density of the Smith Chart automatically adjusts according to the Zoom status.

### Area Select / Zoom Back

Options

- **1**. Click the button
- 2. Select a rectangle in valid area to stand out the interested area.
- 3. The grid line density of the Smith Chart automatically adjusts according to the Zoom status.
- 4. Click the **button to Zoom** back to the last area selected status.

#### Fit

Click the **button** to bring the plot to the default setting.

## **Navigator**

- **1.** Open a dialog.
- 2. Input the Real Min and Real Max values.
- 3. Click OK.

Curve Navigator				×
Real Min:	-0.5	Real Max:	0.5	
Imaginary Min:	-0.3	Imaginary Max:	0.3	
	ОК	Cancel		

1.000j 0.500j 2.000j ∖2.000j 0.200j<sub>/</sub> 0 0.500 00 0.200 1.000 2.000 5:000 -0.200) -5.000j -2.000j -0.500j -1.000j

The plot is redrawn according to the new settings.

#### **Menu Functionality**

- **1.** Move the mouse on a curve.
- 2. Right-click. The menu appears.



- Add Annotation Click Add Annotation to switch the edit status to adding annotation.
- Auto Tip Click Auto Tip to toggle the option of showing tip.
- Black Background Click Black Background to toggle the background of the plot.
- Delete Click Delete to delete the selected curve.
- Embed-Ctrl Visibility / Position Float or resize the legend bar or rearrange the fixed position.
- Hide Curve Click Hide Curve to hide the selected curve.
- **Property** Click **Property** to set up the curve pattern of the selected curve.

#### **Auto-tip**

There are three sorts of tip in Smith Chart view:

- X-Axis
- Y-Axis
- Curve node

The autotip of the Curve node includes:

- Complex Value of the S Matrix Element at this Frequency.
- Frequency.
- Name of the S Matrix Element.
- Normalized Admittance Y.
- Normalized Impedance Z.
- VSWR.

Given the **S matrix** element value as s, the read-out is:

$$z = \frac{1+s}{1-s}$$
$$VSWR = \frac{1+|s|}{1-|s|}$$
$$y = \frac{1-s}{1+s}$$





# Chapter

# **Customize Workflow**

This chapter introduces the customized workflow and takes you through customization process stepby-step.

# LESSON ONE: UNDERSTANDING THE DEFAULT WORKFLOW

The default workflow now includes a customization option.

1. Click:

Customize Workflow

The Customize Workflow section in the Workflow expands and displays the customization options.

2. Click:

Edit current workflow

.

The Current workflow can be customized.

Vorkflow: XtractIM	×	Workflow: XtractIM
Default	*	Default
Manage Workspace	$\bigcirc$	Manage Workspace 📀
Load Workspace		Load Workspace
Load a New/Different	Layout	Load a New/Different Layout
Package Setup	٢	Package Setup
Package Type: Wireb	ond	Package Type: Wirebond
🗙 Circuits		× Circuits
🗙 Stackup		🗙 Stackup
🗙 Solder Ball		🗙 Solder Ball
🗸 Nets		🗸 Nets
Simulation Setup	$\bigcirc$	Simulation Setup
Module: IBIS/RLGC		Module: IBIS/RLGC
Simulation Type: Net	Based	Simulation Type: NetBased
View/Export results	s 🙆	View/Export results
Summary		Summary
SPICE/IBIS Model		SPICE/IBIS Model
RLC Per Net		RIC Per Net
RLC Distributions		RLC Distributions
Segment RLC		Segment RLC
Save Results		Save Results
Load Results		Load Results
Customize Workflow	⊗	Customize Workflow
		Edit current workflow
Expanded		Reload current workflow
		Reset to default workflow
		Load an existing workflow
		Save current workflow
		Save current workflow as
		Import an existing workflow

# LESSON TWO: EDIT WORKFLOW

You can add, rename and change the sequence of the Workflow.

**1.** Click:

Simulation Setup > New

2. Click:

New Scheme

- 3. Change the name from New Step to Extraction Frequency.
- 4. Click Set.
- 5. Click:

Setup > Extraction Frequency

- 6. Click OK.
- 7. Click:

Package Type > Circuits

- 8. Change the name Circuits to a name your prefer (such as Circuit Setup).
- 9. In the Workflow pane, move Nets to:

Package Type > Wirebond

**10.** Click:

Finish and Return

The new Workflow is updated.



# LESSON THREE: SAVE THE WORKFLOW

1. Click:

Customize Workflow > Save Current Workflow

An XtractIM.cfg file is saved in the same directory as XtractIM.exe.

2. Click:

Customize Workflow > Reset to default workflow

The workflow goes to **Default Workflow**.

# **Load Existing Workflow**

- After launching XtractIM, the saved XtractIM.cfg is automatically launched. The customized workflow is loaded.
- **2.** Select:

Customize Workflow > Reset to default workflow

The workflow goes to Default Workflow.

**3.** To substitute the current file, select:

Simulation Setup > Extraction Frequency

or select:

Import an existing workflow \*.cfg file

Workflow: XtractIM	×	Default
Default	*	Manage Workspace 📀
Manage Workspace		✓ Load Workspace
		Load a New/Different Layout
Load a New/Different Layout		🐑 New
		Package Setup 📀
Package Setup		Package Type: Wirebond
<ul> <li>Nets</li> </ul>		Circuits
Package Type: Wirebond		Stackup
🗙 Circuit Setup		Solder Ball
🗙 Stackup		Vets
🗙 Solder Ball		* New
Simulation Setup 🛛 🔿		Simulation Setup (2)
Module: IBIS/RLGC		Module: IBIS/RLGC
Simulation Type: NetBased		Simulation Type: NetBased
Extraction Frequency		Extraction Frequency
View/Export results		View/Export results
Summary		
SPICE/IBIS Model		SPICE/IBIS Model
RLC Per Net		RLC Per Net
RLC Distributions		RLC Distributions
Seament RLC		Segment RLC
Save Results		Save Results
Load Results		✓ Load Results
Customize Workflow		* New
Edit current workflow		new Scheme
Reload current workflow		Finish and Return
Reset to default workflow		
Load an existing workflow		
Save current workflow		
Save current workflow as		
Import an existing workflow		

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