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SPEED2000 TDR/TDT Simulation Tutorial

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1 Introduction

This tutorial demonstrates how to use TDR (Time-Domain Reflectometry)/TDT (Time-Domain Transmission) mode in SPEED2000 to simulate the measurement of TDR/TDT for signal integrity analysis.

The TDR/TDT mode in SPEED2000 enables user to easily check the signal's propagation, reflection and impedance discontinuity by step pulse response. The simulation results can better show voltage and impedance variation with time, helping user to check the quality of signal propagation channel. And the impedance discontinuous position on board can be calculated by the time and signal propagation velocity.

1.1 Overview

SPEED2000 provides the following functions in TDR/TDT mode:

- Create TDR/TDT circuits automatically
- Create TDR/TDT circuits manually
- Calculate impedance at TDR/TDT circuits
- Display TDR/TDT voltages



The TDR/TDT workflow leads user to:

• Setup layout

- Setup TDR/TDT
- Setup other simulation options
- Run simulation
- View simulation results

1.2 Sample Case

The original layout file used in this tutorial is:

- SODIMM_TDR_TDT.spd
- It is located in: <INSTALL_DIR>\SpeedXP\Samples\SPEED2000\TDR-TDT Simulation\Examples_PreSetup\

The completed file (with step by step setup introduced in this tutorial) is also provided and located in:

- <INSTALL_DIR>\SpeedXP\Samples\SPEED2000\TDR-TDT Simulation\Examples_PostSetup\

2 Layout Setup

This chapter describes how to setup layout for TDR/TDT simulation.

2.1 Loading Layout File

- 1. Launch SPEED2000 Generator.
- 2. Select the **TDR/TDT Simulation** workflow.



- 3. Click Load Layout File to load SODIMM_TDR_TDT.spd.
- 4. Click **Select TDR/TDT mode** in the **Workflow** pane to enable TDR/TDT simulation mode.



When enabled, a check mark \checkmark appears next to the workflow step.

2.2 Checking Stackup

1. Click Check Stackup in the Workflow pane.

The Layer Manager -> Stack Up window opens.

- Laver #	Color	Laver Icon	Lawer Name	Thicknoce(Matorial	Conductivity/S	Fill-ip Dielectric	Dermittivity	Loss T 🔶
Layei #	COIOI	Layer Icon	Disco@1	0.02554	material	E Se LOO7	Therecone	Fernice vicy	[0]
			Madium #40	0.03556		5.08+007	1		[0]
			Medium\$40	1				1	0
			Medium\$41	0.017				2,25	0.02
			Signal\$TOP	0.033		5.959e+007		[3.175]	[0.02]
			Medium\$43	0.102				4.1	0.02
			Signal\$SPLIT2	0.033		5.959e+007		[4.1]	[0.02]
			Medium\$45	0.13				4.1	0.02
			Signal\$S3	0.033		5.959e+007		[4.1]	[0.02] =
			Medium\$47	0.559				4.1	0.02
			Signal\$S4	0.033		5.959e+007		[4.1]	[0.02]
			Medium\$49	0.13				4.1	0.02
			Signal\$SPLIT5	0.033		5.959e+007		[4.1]	[0.02]
			Medium\$51	0.102			1	4.1	0.02
			Signal\$BOTTOM	0.033		5.959e+007		[3.175]	[0.02]
			Medium\$53	0.017			1	2.25	0.02
			Medium\$54	1				1	0
		777	Diane02	0.03556		5 801007		E11	[0] V
			111						- • •
Total Thick	necc: 3-33	261e±000 mm					View Mat	erial 1	Import
rocar mick	10331 0102	.010100011111				,	How Had		mpore

2. Check stackup and click **OK** when all settings are complete

2.3 Selecting Nets

1. To setup P/G nets, click **Select Nets** in the **Workflow** pane.



2. Click **Setup P/G nets** from the pop-up menu list.

The P/G nets classification wizard appears and leads you to setup P/G nets step by step.

Comp	onent				
⊞ □					
CONTRACTOR 12 EMA CONTRACTOR 12 EMA					
🗄 🗖 🤣 NewEmptyCktDef					
Filter components with number of pins >= 8 Update					
🗹 Filte	er components with number of pins >= 8 Update				
✓ Filter components with number of pins >= 8					

NOTE!	If the P/G nets are setup already (like the example case in this tutorial), ignore
110 120	this step or just click Skip setup P/G nets.

3 TDR/TDT Single Ended Simulation

This chapter demonstrates how to setup circuit model, generate ports, run simulation and view simulation results for TDR/TDT single ended.

3.1 Setting Up TDR/TDT Circuit Model

1. Select and enable the desired nets in **Net Manager** as the following figure shows.

Net Ma	anager		×
Net:		-	P
	Default Mode	-	<u> </u>
Net Li	st (Sort enabled first)		-
	📿 💋 Unnamed Net(s)		
	PowerNets		_ =
	GroupdNets		-
	DQ1		
	DQ2		
	🗾 DQ3		
	🗾 DQ4		
	DQ5		_
	DQ6		_
Ľ	DQ7		_
			-
			-
N N			-
	TDQ2		
	🗾 TDQ3		
☑	TDQ4		
☑	🗾 🗾 TDQ5		
⊡	TDQ6		_
	TDQ7		_
	📿 🖊 TDQS0n		_
			-
			-
Gene	eral		
✓ Ke	ep shape enabled when the ne de Disabled av Disabled	et is	disat
Laver	Selection Net Manager	_	

2. Click **Setup TDR/TDT circuit model** in the **Workflow** pane. The **Circuit/Linkage Manager** opens.

Circuit/Linkage Manager 🛛 🗙 🗙
- ₽
Model Name 🖉 Ckt Type
Ckt Node 🛆 Pkg Node 🛛 Layer Na
< <u> </u>

3. Click New.

The New window opens.

New ×
Туре
New Circuit Model Definition
 TDR Single Ended
O TDT Single Ended
O TDR Differential
O TDT Differential
O Other Circuit Models
O New Circuit
O New Circuit By Selected Nodes - Pin Based
O New Circuit By Selected Nodes - Net Based
OK Cancel

- 4. Select **TDR Single Ended**.
- 5. Click **OK**.

The TDR Single Ended window opens.

Т	DR Single Ended		×
	SE Internal Resistance:	50	Ohm
	SE Source Amplitude:	0.4	v
	Delay:	0	ps
	Rise Time(0-100%):	30	ps
		ОК Са	ncel

- 6. Set the parameters for TDR single-ended as desired.
- 7. Click **OK**.

The **New Definition** window opens, displaying the detailed information of the newly created circuit model definition.

New Definition				- 🗆 X
Definition Type Partial Circuit	O Sub-circuit	O Model	Partial Circuit Type • SpeedXP	O HSPICE
Name : TDR_SE_1			Local Parameters : Name Value	Global Parameter
External Nodes : pos gnd			td Op tr 30p v0 0.4	
Definition :			New Edi	Delete
rp pos 1 z0 vp 1 gnd PULSE (0 v0 td tr tr 1)			Model File Type: File Name : Component Name: Edit IBIS Header/Footer Info : + ExtNode = pos gnd + td = 0p + td = 0p	Delete IBIS
			ОК	Cancel

The TDR source is a voltage source with step waveform. By default:

- SE Internal Resistance 50ohm
- SE Source Amplitude 0.4v
- Delay Ops
- **Rise Time** 30ps
- 8. Click **OK** to quit the **New Definition** window when all settings are complete.

9. Repeat step 3 to 8 to create TDT single ended circuit model definition. Remember to select **TDT Single Ended** in the **New** window.

New ×			
Туре			
• New Circuit Model Definition			
O TDR Single Ended			
 TDT Single Ended 			
O TDR Differential			
O TDT Differential			
O Other Circuit Models			
O New Circuit			
O New Circuit By Selected Nodes - Pin Based			
O New Circuit By Selected Nodes - Net Based			
OK Cancel			

The newly created circuit model definitions can be viewed in Circuit/Linkage Manager.

Circuit/Linkage Manager	×
	- 🔎
Model Name 🔺	Ckt Type
TDR_SE_1	TDR_SE TDT_SE
New Del Edit L	.oad Filter 🔽

3.2 Generating TDR/TDT Ports Automatically

1. Right-click **TDR_SE_1** and click **Create TDR Circuit** from the pop-up menu list.

55 60 65 7 Circuit/Linkage Mana	ager ×
Switch to Circuit View Expand All Circuit Definitions Collapse All Circuit Definitions	SE_1 TDR_SE
Create TDR Circuit Circuit Voltage View Current View	
Close Linkage Window Close Definition Window Tab Linkage Window and Definition Window	Edit Load Filter 🔽
Assign Capacitor Models Assign Component Tags	

The Auto Generate TDR Circuits window opens.

Auto Generate TDR Circuits 🗙 🗙					
	Circuit Model: TDR_SE_1				
	Reference circuit:				
	Layer	Circuit Name	Circuit Model		
	Signal\$TOP	C1	2PORT_CAP-10		
	Signal\$BOTTOM	C10	2PORT_CAP-10		
	Signal\$BOTTOM	C11 C12	2PORT_CAP-10		
	Signal\$BOTTOM	C12	2PORT_CAP-10		
	Signal\$BOTTOM	C14	2PORT CAP-10		
	Reference Net: GroundNets Pin Groups: X				
	Reference Pins:				
	OUse Pin Groups	~			
	🔲 Search Distar	nce for Signal net	mm		
	O Use Reference (tell			
	O Use Reference Node				
	Generate Circuits Close				

- 2. Set the parameters as following:
 - Reference circuit: J1
 - Target Layer: Signal\$TOP

Auto Generate TDR Circuits 🗙 🗙					
Circuit Model: TDR_S	Circuit Model: TDR SE 1				
Reference circuit:					
Layer	Circuit Name	Circuit Model			
Signal\$TOP	SPD1	9PIN_SPD-LCC			
Signal\$BOTTOM	T51	9PIN_SPD-LCC			
Signal\$BOTTOM	J1	DDR3_SODIMM			
Signal\$TOP	UO	DDR3_X16_96B			
Signal\$TOP	U1	DDR3_X16_96B			
Signal\$TOP	U2	DDR3 X16 96B	¥		
Reference Net: Sig All	Signal\$TOP Reference Net: Signal\$BOTTOM All Layers				
Reference Pins:					
OUse Pin Groups					
Search Dista	nce for Signal net	mm			
OUse Reference (Cell: (0,0)				
O Use Reference f	Node				
Generate Circuits Close					

Description of Auto Generate TDR Circuits Window

- Target Layer Select the layer pins
- **Reference Net** List all the enabled nets in the GroundNets group as well as GroundNets which include all the ground nets:
 - The default selection is GroundNets. If GroundNets is selected, all ground nets in the list serve as reference nets. The Negative Terminals are the pins of these reference nets in circuit generation.
 - If an individual ground net (not the group name GroundNets) is selected, circuits are generated in each cell or cell group for signal nets, power nets and other ground nets. The negative terminals are the pins of the selected reference net.
- **Pin Groups** Divide the pins into rectangular cells from which the circuits will be generated
 - Left number Columns of cells
 - Right number Rows of cells
 - Default value 1x1
- **Reference Pins** Rules to determine the negative nodes in the automatic circuit generation. Three options are available:
 - Use Pin Groups

Circuits are generated for each pin of the Power, Ground and Signal nets. If there is no pin for the reference net, the neighbor cells are searched until the nearest ground pin is found. The nearest ground pin serves as negative terminals for the cell, as shown in the example. The aim is that the same reference pins should be used in as few cells as possible. This approach is called Use Pin Groups.



- Use Reference Cell
- Use Reference Node
- 3. Click the Generate Circuits button.

The TDR circuits on top layer are automatically generated.

- 4. To generate TDR circuits on bottom layer, set the parameters as following:
 - Reference circuit: J1
 - Target Layer: Signal\$BOTTOM

A	Auto Generate TDR Circuits				
	Circuit Model: TDR_SE_1				
	Reference circuit:				
	Layer	Circuit Name	Circuit Model		
	Signal\$TOP	SPD1	9PIN_SPD-LCC		
	Signal\$BOTTOM	T51	9PIN_SPD-LCC		
	Signal\$BOTTOM	31	DDR3_SODIMM		
	Signal\$TOP	U0	DDR3_X16_96B		
	Signal\$TOP	01	DDR3_X16_968		
	Signal\$TOP	02	DDR3 X16 968		
	Target Layer: Sigr	nal\$BOT'(👻			
	Reference Net: Sign	hal\$BOTTOM	Groups: 1 X	1	
	All I	ayers			
	Reference Pins:				
	• Use Pin Groups	~			
	Search Distar	nce for Signal net	mm		
	O Use Reference (
		lada			
	Use Reference Node				
	Generate Circuits Close				

The TDR circuits on bottom layer are automatically generated.

- 5. Click **Close** to quit the **Auto Generate TDR Circuits** window.
- View the newly generated TDR circuits in Circuit/Linkage Manager by selecting Setup > Circuit/Linkage Manager...

Circuit/Linkage Manager 🛛 🗙				
		- P		
	Model Name 🔷 🛆	Ckt Type		
	🖃 🤣 TDR_SE_1	TDR_SE		
🗸 🖂	TDR_TDQ0			
🗸 🖂	TDR_TDQ1			
🗸 🖂	TDR_TDQ2			
🗸 🖂	TDR_TDQ3			
🗸 🖂	TDR_TDQ4			
🗸 🖂	TDR_TDQ5			
🗸 🖂	TDR_TDQ6			
🗸 🖂	TDR_TDQ7			
	🔗 TDT_SE_1	TDT_SE		
		•		
😫 N	ew Del Edit L	.oad Filter 🔽		

7. Right-click **TDT_SE_1** and click **Create TDT Circuit** from the pop-up menu list.

5 60 65 7 🔺	Circuit/Linkage Manager 🛛 🗙		
		- 9	
	Model Name	🛆 Ckt Type	
	📃 🖃 🂔 TDR_SE	_1 TDR_SE	
)Q0	
		DQ1	
		DQ2	
		DQ3	
Switch to Circuit View		_1 TDT_SE	
Division of All Character De G	- 11.1		
Expand All Circuit Deri	nitions		
Collapse All Circuit Del	initions	it Load Filter 🔽	
Create TDT Circuit			
Circuit Voltage View		e Layer Nam	
Current View			
Close Linkage Window	ı		
Close Definition Windo	W		
Tab Linkage Window a			
Assign Capacitor Mode	Assign Capacitor Models		
Assign Component Ta	gs		

- 8. In the Auto Generate TDT Circuits window, set the parameters like the following:
 - Reference circuit: U0
 - Referent Net: GroundNets

A	Auto Generate TDT Circuits 🗙 🗙				
	Circuit Model: TDT_SE_1				
	Reference circuit:				
	Layer	Circuit Name	Circuit Model		
	Signal\$BOTTOM	RN6	8PORT RES-36		
	Signal\$TOP	SPD1	9PIN SPD-LCC		
	Signal\$BOTTOM	T51	9PIN_SPD-LCC		
	Signal\$BOTTOM	J1	DDR3_SODIMM		
	Signal\$TOP	UO	DDR3_X16_96B		
	Signal\$TOP	U1	DDR3 X16 96B	T	
Target Layer: Signal\$TOP Reference Net: GroundNets Fin Groups: 1					
Reference Pins:					
	⊙ Use Pin Groups ~€				
	📃 Search Distar	nce for Signal net	mm		
	OUse Reference C	Cell: (0,0)			
	O Use Reference Node				
	Generate Circuits Close				

9. Click the Generate Circuits button.

The TDT circuits are automatically generated. The circuits can be viewed in Circuit/Linkage Manager.

Circuit/Linkage Manager 🛛 🗙				
- ₽				
	🕀 🔗 TDR_SE_1	TDR_SE		
🗸 🗚	TDR_TDQ0	_		
🗸 🖂	TDR_TDQ1			
🗸 🖂	TDR_TDQ2			
✓ A	TDR_TDQ3			
✓ 🖂	TDR_TDQ4			
✓ △	TDR_TDQ5			
 ✓ 씜 	TDR_TDQ6			
	TDR_TDQ7			
	TDT_SE_1	TDT_SE		
	TDT DO5			
A	TDT_DO6			
🗸 🖪	TDT_DQ7			
🔀 New Del Edit Load Filter 🍸				

3.3 Generating TDR/TDT Ports Manually

This section introduces how to generate TDR/TDT ports manually if the auto-generated ports do not meet your requirements or you hope to generate ports manually.

1. In Circuit/Linkage Manager, select TDR_SE_1.

Circuit/Linkage Manager 🛛 🗙
Model Name 🛆 Ckt Type
TDR_SE_1 TDR_SE
TDT_SE_1 TDT_SE
New Del Edit Load Filter
Ckt Node 🛆 Pkg Node Layer Na
Link Unlink
.PartialCkt_TDR_SE_1
+ ExtNode = pos gnd + td = 0p
+ tr = 30p + v0 = 0.4 =
+ z0 = 50
rp pos 1 z0
.EndPartialCkt

2. Click New.

The New window opens.

New ×
Туре
O New Circuit Model Definition
⊙ TDR Single Ended
O TDT Single Ended
O TDR Differential
O TDT Differential
O Other Circuit Models
• New Circuit
O New Circuit By Selected Nodes - Pin Based
O New Circuit By Selected Nodes - Net Based
OK Cancel

- 3. Select New Circuit.
- 4. Click **OK**.

The New Circuits window opens.

New Circuits	×
Definition Name :	TDR_SE_1
Circuit Name :	TDR
Start number :	0
End number :	7
	OK Cancel

- 5. Select TDR_SE_1 as the definition name.
- 6. Enter a circuit name (**TDR** in this example).
- 7. Enter the start and end number if you want to generate more than one port (0 and 7 in this example).
- 8. Click OK.

8 new circuits with the name TDR0-TDR7 are generated. The ports can be viewed in **Circuit/Linkage Manager**.

Circuit/Linkage Manager 🛛 🗙					
	▼ P				
	Model Name 👘 🛆	Ckt Type			
	🖃 🤣 TDR_SE_1 🛛	TDR_SE			
Α	TDRO				
Α	TDR1				
Α	TDR2				
Α	TDR3				
Α	TDR4				
Α	TDR5				
Α	TDR6				
A	TDR7				
	🌮 TDT_SE_1	TDT_SE			
😫 New Del Edit Load Filter 🔽					

9. To generate TDT ports manually, select **TDT_SE_1** in **Circuit/Linkage Manager** and repeat step 2 to 8.

All circuits generated can be viewed in Circuit/Linkage Manager.

Circuit/Linkage Manager 🛛 🗙				
▼ ₽				
	Model Name 💫 🛆	Ckt Type		
	📮 🤣 TDR_SE_1	TDR_SE		
Α	TDR0			
Α	TDR1			
Α	TDR2			
Α	TDR3			
	TDR4			
	TDR5			
	TDR6			
A	TDR7			
	E 🐶 TDT_SE_1	TDT_SE		
<u> </u>	TDTO			
	TDT1			
씜	TDT2			
씜	TDT3			
씸	TDT4			
믬	IDI5			
	ID16			
	71017			
New Del Edit Load Filter				

3.3.1 Linking TDR/TDT Circuits to Board Manually

Select the desired circuit in Circuit/Linkage Manager, for example, TDR0.
 The information of the selected circuit node is listed in the Package Linkage Assignment pane.



- 2. Highlight the circuit node you want to link to the board in the **Package Linkage Assignment** pane, for example, **gnd**.
- 3. Right-click the desired node on board and click **Link** from the pop-up menu list.

NOTE! Make sure the package node you want is on the active layer.

4. Repeat step 2 to 3 to link the other circuit node.

When both circuit nodes are successfully linked to package nodes, a green mark \checkmark appears ahead of the circuit, and the linkage information is listed in the **Package Linkage Assignment** pane.



5. Repeat step 1 to 3 to link all circuits to board. A green mark \checkmark ahead of the active icon A shows it is successfully linked.

Circuit/Linkage Manager 🛛 🗙				
			- P	
	Model Name 👘 🛆	Ckt Type	Model	
	📮 🤣 TDR_SE_1	TDR_SE		
🗸 🖪	TDR0			
🗸 🖪	TDR1			
 A 	TDR2			
🗸 🖪	TDR3			
✓ ■	TDR4			
✓	TDR5			
✓	TDR6			
✓ A	TDR7			
	E 🐶 TDT_SE_1	TDT_SE		
⊻⊵	TDTO			
✓ △	TDT1			
✓ 점	TDT2			
⊻₿	TDT3			
⊻₿	TDT4			
Y ≅	TDT5			
온염	TDT6	_		
V A	TDT7			
	Ш		►	
	New Del Ed	lit Load	Filter 🔽	

3.4 Selecting Ports for Simulation

1. Click Select TDR/TDT ports for simulation in the Workflow pane.

The **Setup TDR/TDT** window opens, displaying all available ports. All TDR ports are selected by default.

etup TDR/TDT		□ :
TDR	△ Net	TDT
V TDR_TDQ0	TDQ0	
V TDR_TDQ1	TDQ1	
V TDR_TDQ2	TDQ2	
V TDR_TDQ3	TDQ3	
V TDR_TDQ4	TDQ4	
V TDR_TDQ5	TDQ5	
V TDR_TDQ6	TDQ6	
V TDR_TDQ7	TDQ7	
		OK Cancel

2. Double-click **E** under TDT column to select TDT ports for simulation

Se	Setup TDR/TDT 🗆 🗙					
	TDR 🛆	Net	TDT			
	TDR_TDQ0	TDQ0		E		
	TDR_TDQ1	TDQ1		Vet		
	V TDR_TDQ2	TDQ2	TDT_DQ0)Q0		
	TDR_TDQ3	TDQ3	TDT_DQ1	Q1		
	TDR_TDQ4	TDQ4	TDT_DQ2)Q2		
	TDR_TDQ5	TDQ5	TDT_DQ3	0Q3		
	TDR_TDQ6	TDQ6	TDT_DQ4	DQ4		
	TDR_TDQ7	TDQ7	TDT_DQ5)Q5		
OK Cancel						

A green checkmark \checkmark shows the port is selected. Check the ports as the following figure shows.

TDR	Δ	Net	TDT
V TDR_TDC	20	TDQ0	TDT_DQ0
🗹 TDR_TDC	21	TDQ1	TDT_DQ1
TDR_TDC	22	TDQ2	TDT_DQ2
V TDR_TDC)3	TDQ3	TDT_DQ3
TDR_TDC	24	TDQ4	TDT_DQ4
TDR_TDC) 5	TDQ5	TDT_DQ5
TDR_TDC	<u>}6</u>	TDQ6	TDT_DQ6
V TDR_TDC	27	TDQ7	TDT_DQ7

3. Click **OK** to quit the window.

3.5 Running Simulation

1. Click Generate Mesh in the Workflow pane.

The **Mesh** window opens.

Mesh			×		
Г	Change to	Default			
Mesh_X	84	60			
Mesh_Y	37	60			
	Automatically G	ienerate Mesh			
Package Name: \$Package					
OK Cancel					

2. Click the Automatically Generate Mesh button.

Mesh			×
Г	Change to	Default	
Mesh_X	84	60	
Mesh_Y	37	60	
[] [Automatically (Generate Mesh	
Package Nar	ne: \$Package	•	
	ОК	Cancel	

The values of $Mesh_X$ and $Mesh_Y$ are automatically generated.

- 3. Click **OK** to quit the **Mesh** window.
- 4. Click Assign Simulation Time in the Workflow pane.

The **Transient** window opens.

Transient				×	
Time:	1	[ns 💌		
Timesteps:	576	Time_Ir	nterval:	10	
🗌 Enable id	leal power-grour	nd mode			
Time step:	1.73376	ps			
Enable plane skin effect					
🗹 Enable tr	ansmission line r	netal loss			
🗹 Enable d	ielectric loss and	dispersion			
Enable initial DC analysis					
	[ОК] []	ancel	

- 5. Set the simulation parameters as the above figure shows.
- 6. Click **OK** to quit the **Transient** window.
- Click Save the changes in the Workflow pane. The Save As window opens.

8. Browse to the desired folder and enter a name (for example, **SODIMM_TDR_TDT_1**) if you want to save as a different file.

Save As		?	×
Save in:	🖕 TDR_TDT 🔹 🕥 🎓 📰 •		
My Recent Documents Desktop	SODIMM_TDR_TDT.spd		
My Computer			
	File name: SODIMM_TDR_TDT_1.spd	<u>ave</u>	
My Network	Save as type: SPEED2000 Files (*.spd)	ancel	

9. Click Start Simulation in the Workflow pane.

The Run SPDSIM window opens.

Run SPDSIM	x
Load into SPDSIM and simulation	
Pause 3D displays for maximum efficiency	
O Load into SPDSIM only	
OK Cancel	

10. Click **OK**.

SPDSIM starts to simulate. A blue bar appears to show the progress of simulation.

Running	
Preprocessing	
	33%

NOTE!

Although multiple TDRs are selected while sweeping, SPEED2000 simulates only one of the TDRs and disconnects other TDRs during each simulation.

3.6 Viewing Result

When simulation is complete, a result window appears to show the simulation results.



The results include:

- Impedance at the TDR Port
- Voltage at the TDR Port
- Voltage at the TDT Port
- Other Voltages/Currents Views

A folder (for example, **SODIMM_TDR_TDT_1_result**) with results in is created under the same location of the case.

(TDR-TDT Tutorial\TDR_TDT					
×	Name 🔺	Size	Туре	Date Modified	
~	CODIMM_TDR_TDT_1_result		File Folder	2012-8-1 16:24	
	🛅 Trace_Pad_Library		File Folder	2012-8-1 16:34	
	execution_time.log	18 KB	Text Document	2012-8-1 16:36	
	🗐 memory_time.log	1 KB	Text Document	2012-8-1 16:36	
	🗐 profile_spd.log	126 KB	Text Document	2012-8-1 16:36	
	SODIMM_TDR_TDT.spd	3,355 KB	SPEED2000 Document	2012-7-27 12:51	
	SODIMM_TDR_TDT_1.spd	3,350 KB	SPEED2000 Document	2012-8-1 16:23	
	SODIMM_TDR_TDT_1_spdsim	19 KB	ERR File	2012-8-1 16:23	

4 TDR/TDT Differential Simulation

This chapter demonstrates how to setup circuit model, generate ports, run simulation and view simulation results for TDR/TDT differential.

4.1 Selecting Differential Nets

1. Select and enable the desired differential nets in **Net Manager** as the following figure shows.



2. Right-click the differential nets and select Classify > Detect Diff Pairs and Polarities.

	Enable Selected Nets Disable All Nets Disable All Nets	6 50n 50p 20 21 22 23 24
As PowerNets As GroundNets As Signal Nets P/G nets classification wizard As Power-Ground Pair Not As Power-Ground Pair	Classify P Detect Associated Nets New Delete Rename Import	25 26 27 250n 250p
As Diff Pair Not As Diff Pair Detect Diff Pairs and Polarities Switch Polarity As Alias	Merge Selected Nets Split Open Nets Show Objects of Nets 3D View Walk Through Property	abled when the net i
Not As Alias		1

The differential pairs and polarities are detected automatically.



3. Click **Show Coupled Line** to switch to the coupling mode.

Net M	1anager 🛛 🗙 🗙	:
Net:	- P]
	Default Mode 🔹	
Mak	Default Mode	٦
Nec	Show Coupled Line	
	Show Volt & P/G	1
	🛛 🛛 🖉 GroundNets 🔤	

- 4. Set the parameters as the following:
 - %Coupling: 5
 - Rise Time (ps): 100

let:	-	Show Coupled (
Net List(Sort enabled first)	∆ <mark>™</mark> %Coupling) 🛛 🛛 Rise Time (ps)
🗹 🗾 ΥΤΤ		
🖃 🗹 🛛 🌌 GroundNets		
🗹 🗾 GND		L
r 🗹 🗾 DQS0n	5	100
🕀 🗹 🗾 DQS0p	5	100
r 🗹 🗾 TDQS0n	5	100
🕀 🗹 🛛 🗖 TDQS0p	5	100
🗖 📿 🗾 A0		

NOTE! Do NOT forget to switch to the coupling mode and set the coefficient of Coupling and Rise Time, otherwise it would be considered as single ended during simulation.

4.2 Setting Up TDR/TDT Circuit Model

1. Click Setup TDR/TDT circuit model in the Workflow pane.

The Circuit/Linkage Manager opens.

Circuit/Linkage	Manager	×
		- 🔎
Model	Name 🛛 🔺 Ckt	Туре
4		•
IN I		
Ckt Node 🛆	Pkg Node	Layer Na
4	111	
	u-k-k	
Layer Sele	Circuit/Linka N	let Manager

2. Click New.

The New window opens.

New ×
Туре
New Circuit Model Definition
O TDR Single Ended
O TDT Single Ended
 TDR Differential
O TDT Differential
O Other Circuit Models
O New Circuit
O New Circuit By Selected Nodes - Pin Based
O New Circuit By Selected Nodes - Net Based
OK Cancel

- 3. Select **TDR Differential**.
- 4. Click **OK**.

The TDR Differential window opens.

TDR Differential	×
SE Internal Resistance:	50 Ohm
SE Source Amplitude:	0.2 V
Delay:	0 ps
Rise Time(0-100%):	30 ps
E	OK Cancel

- 5. Set the parameters for TDR differential as desired.
- 6. Click **OK**.

The **New Definition** window opens, displaying the detailed information of the newly created circuit model definition.

New Definition	- 🗆 X
Definition Type O Partial Circuit O Sub-circuit Model Name : TDR_DIFF_1 External Nodes : pos neg gnd Definition :	Partial Circuit Type SpeedXP HSPICE Local Parameters : Global Parameter Name Value td Op tr 30p v0 0.2
rp pos 1 20 vp 1 gnd PULSE (0 v0 td tr tr 1) rn neg 2 20 vn gnd 2 PULSE (0 v0 td tr tr 1)	Model File Type: File Name : Component Name: Edit IBIS Delete IBIS Header/Footer Info : ✓ Read-Only + td = 0p + + 0 + 0 - + 0 - + 0 + 0 + 0 -
	OK

- 7. Click **OK** to quit the **New Definition** window when all settings are complete.
- 8. Repeat step 2 to 7 to create TDT differential circuit model definition. Remember to select **TDT Differential** in the **New** window.

ew	×
Туре	
• New Circuit Model Definition	
O TDR Single Ended	
O TDT Single Ended	
O TDR Differential	
 TDT Differential 	
O Other Circuit Models	
O New Circuit	
O New Circuit By Selected Nodes - Pin Based	
O New Circuit By Selected Nodes - Net Based	ł

The newly created circuit model definitions can be viewed in Circuit/Linkage Manager.

Circuit/	Linkage Manager	×
		- 🔎
	Model Name 💫 🛆	Ckt Type
	TDR_DIFF_1	TDR_DIFF
	TDT_DIFF_1	TDT_DIFF
	111	····· •
😫 New Del Edit Load Filter 🏹		

4.3 Generating TDR/TDT Ports Automatically

1. Right-click **TDR_DIFF_1** and click **Create TDR Circuit** from the pop-up menu list.

55	60 65 🗠 Circuit/Linkage Manage	er 👘	×
			- P
	Model Name	Δ	Ckt Type
	Switch to Circuit View	**F_1 *F_1	TDR_DIFF TDT_DIFF
	Collapse All Circuit Definitions		
	Create TDR Circuit		
	Circuit Voltage View Current View	- - -	oad Filter 🍸
	Close Linkage Window Close Definition Window Tab Linkage Window and Definition Window	e	Layer Na
	Assign Capacitor Models		
	Assign Component Tags		

The Auto Generate TDR Circuits window opens.

Signal\$TOP C1 2PORT_CAP-10 Signal\$BOTTOM C10 2PORT_CAP-10 Signal\$BOTTOM C11 2PORT_CAP-10 Signal\$BOTTOM C12 2PORT_CAP-10 Signal\$BOTTOM C13 2PORT_CAP-10 Signal\$BOTTOM C14 2PORT_CAP-10 Target Layer: Reference Net: GroundNets Reference Pins:		
Signal\$BOTTOM C10 2PORT_CAP-10 Signal\$BOTTOM C11 2PORT_CAP-10 Signal\$BOTTOM C12 2PORT_CAP-10 Signal\$BOTTOM C13 2PORT_CAP-10 Signal\$BOTTOM C14 2PORT_CAP-10 Target Layer:		
Signal\$BOTTOM C11 2PORT_CAP-10 Signal\$BOTTOM C12 2PORT_CAP-10 Signal\$BOTTOM C13 2PORT_CAP-10 Signal\$BOTTOM C14 2PORT CAP-10 Target Layer: Reference Net: GroundNets Pin Groups: X	-	
Signal\$BOTTOM C12 2PORT_CAP-10 Signal\$BOTTOM C13 2PORT_CAP-10 Signal\$BOTTOM C14 2PORT CAP-10 Target Layer: Reference Net: GroundNets Pin Groups: X	-	
Signal\$BOTTOM C13 2PORT_CAP-10 Signal\$BOTTOM C14 2PORT_CAP-10 Target Layer: Reference Net: GroundNets Pin Groups: X	-	
Signal\$BOTTOM C14 2PORT CAP-10 Target Layer: Image: Capering of the second s	•	
🕑 Use Pin Groups 🔍 💭		
Search Distance for Signal net mm		
Use Reference Node		

- 2. Set the parameters as following:
 - Reference circuit: J1
 - Target Layer: Signal\$BOTTOM

Au	Auto Generate TDR Circuits 🗙 🗙				
0	Circuit Model: TDR_SE_1				
F	Reference circuit:				
[Layer	Circuit Name	Circuit Model		
	Signal\$TOP	SPD1	9PIN_SPD-LCC		
	Signal\$BOTTOM	T51	9PIN_SPD-LCC		
	Signal\$BOTTOM	31	DDR3_SODIMM		
	Signal\$TOP U0 DDR3_X16_96B				
	Signal\$TOP U1 DDR3_X16_96B				
	Signal\$TOP UZ DDR3 X16 96B				
1	larget Layer: Sigr	nal\$BOT'[👻			
	Sign	hal\$BOTTOM			
F	Reference Net: Signal\$TOP Pin Groups: 1 X 1				
	All Layers				
l r	Reference Pins:				
	⊙ Use Pin Groups ~€				
	Search Distance for Signal net mm				
	O Use Reference Cell Cell; (0,0)				
l					
	Generate Circuits Close				

The TDR circuits on bottom layer are automatically generated.

3. Click **Close** to quit the **Auto Generate TDR Circuits** window.

4. View the newly generated TDR circuits **Circuit/Linkage Manager** by selecting Setup > Circuit/Linkage Manager...

Circuit/	Linkage Manager	×
		▼
	Model Name 🔼	Ckt Type
	📮 🤣 TDR_DIFF_1	TDR_DIFF
🗸 🖪	DiffTDR_TDQS0p_TDQS0n	
	🛷 TDT_DIFF_1	TDT_DIFF
		•
	New Del Edit Load	Filter 🔽

5. Right-click TDT_DIFF_1 and click Create TDT Circuit from the pop-up menu list.

	13 1 <mark>4 1</mark> 🔺	Circuit/Linkage Ma	nager		×
					- 9
١.		Model Nar	me	🛆 🗹 Ckt Type	
/ \		🖓 TC	R_DIFF_1	TDR_DIF	F
8		J Dif	FTDR_TDQS0p_T	DQS0n	
377 -	Switch to Circuit View		I_DIFF_I		-
	Expand All Circuit Definition	25			
	Collapse All Circuit Definitio	ins			
		113	-111		•
	Create TDT Circuit		Dol Edit		
	Circuit Voltage View				
	Current View		g Node	Layer Name	
	Close Linkage Window				
	Close Definition Window				
	Tab Linkage Window and D	efinition Window			
	Assign Capacitor Models				
	Assign Component Tags				

- 6. In the Auto Generate TDT Circuits window, set the parameters like the following:
 - Reference circuit: U0
 - Referent Net: GroundNets

Signal\$BOTT	Layer Circuit Name Circuit Model					
Signal\$TOP		SPD1	9PIN_SPD-LCC			
Signal\$BOTT	ОМ	TS1	9PIN_SPD-LCC			
Signal\$BOTT	ом	31	DDR3_SODIMM			
Signal\$TOP		UO	DDR3_X16_96B			
Target Layer:	Sign	al\$TOP 👻				
Reference F	Grou Pins GND	IndNets				
• Use Pin G	n Dictary					
⊙ Use Pin G	n Distani	ce for Signal net	mm			
Use Pin G Search Use Refe	n Distani rence G	ce for Signal net [ell Cell: (0,0)	mm			

7. Click the **Generate Circuits** button.

The TDT circuits are automatically generated. The circuits can be viewed in **Circuit/Linkage Manager**.

Circuit/L	.inkage Manager	×
		- P
	Model Name 🛆	Ckt Type
	📮 🤣 TDR_DIFF_1	TDR_DIFF
🗸 🖪	DiffTDR_TDQS0p_TDQS0n	
		TDT_DIFF
🗸 🖂	ⁱ DiffTDT_DQS0p_DQS0n	
	111	•
	New Del Edit Load	Filter 🔽

4.4 Generating TDR/TDT Ports Manually

To generate TDR/TDT differential ports manually, refer to Section 3.3 Generate TDR/TDT Ports Manually.

4.5 Selecting Ports for Simulation

1. Click Select TDR/TDT ports for simulation in the Workflow pane.

The **Setup TDR/TDT** window opens, displaying all available ports. All TDR ports are selected by default.

etup TDR/TDT		□ ×
	Net	TDT
DiffTDR_TDQ50p_TDQ50n	TDQS0n//TDQS0p	
	111	
		K Cancel

2. Double-click 🗉 under TDT column to select TDT ports for simulation

Se	tup	TDR/TD	Т								×
	~	TDR DiffTDR	_TDQ50p_	∆ _TDQ50n	Net TDQ50n//TD	Q50p	TDT				
								TDT DiffTD	∟ T	Net DQS0n DQ	50p
								ОК		Cancel	

A green checkmark \checkmark shows the port is selected. Check the ports as the following figure shows.

Se	etup	TDR/TDT			□ ×
			Net	TDT	
		DiffTDR TDOSOn TDOSOn	TDOS0n//TDOS0p	DiffTDT DOSOD DOSON	
				OK Car	icel

3. Click **OK** to quit the window.

4.6 Running Simulation

 Click Generate Mesh in the Workflow pane. The Mesh window opens.

Mesh			×
Г	Change to	Default	
Mesh_X	84	60	
Mesh_Y	37	60	
	Automatically G	enerate Mesh	
Package Nar	ne: \$Package	1	
	ОК	Cancel	

2. Click the Automatically Generate Mesh button.

Mesh			×
Г	Change to	Default	
Mesh_X	84	60	
Mesh_Y	37	60	
[] [Automatically (Generate Mesh	
Package Nar	ne: \$Packag	e	
	ОК	Cancel	

The values of $Mesh_X$ and $Mesh_Y$ are automatically generated.

- 3. Click **OK** to quit the **Mesh** window.
- 4. Click Assign Simulation Time in the Workflow pane.

The Transient window opens.

Transient		×				
Time:	Ins 💌					
Timesteps:	576 Time_Interval: 10)				
Enable ideal power-ground mode						
Time step:	1.73376 ps					
✓ Enable plane skin effect						
🗹 Enable tr	ransmission line metal loss					
Enable dielectric loss and dispersion						
C Enable initial DC analysis						
	OK Canc	el				

- 5. Set the simulation parameters as the above figure shows.
- 6. Click **OK** to quit the **Transient** window.
- 7. Click Save the changes in the Workflow pane.

The Save As window opens.

8. **Browse** to the desired folder and enter a name (for example, **SODIMM_TDR_TDT_2**) if you want to save as a different file.

Save As		? :	×
Save in:	🔁 TDR_TDT 🔹 😗 📂 🖽•		
My Recent Documents	SODIMM_TDR_TDT_1_result ☐ Trace_Pad_Lbrary		
Desktop			
My Documents			
S	File name: SODIMM_TDR_TDT_2 spd ▼	<u>S</u> ave	
My Network	Save as gype. SPEED2000 Files (".spd)	Jancel	

9. Click Start Simulation in the Workflow pane.

The Run SPDSIM window opens.

Run SPDSIM	×
 ⊙ Load into SPDSIM and simulation ✓ Pause 3D displays for maximum efficiency 	
O Load into SPDSIM only	
OK Cancel	

10. Click OK.

SPDSIM starts to simulate. A blue bar appears to show the progress of simulation.

Running		
Preprocessing		
	33%	

4.7 Viewing Results

When simulation is complete, a result window appears to show the simulation results.



A folder (for example, **SODIMM_TDR_TDT_2_result**) with results in is created under the same location of the case.

TDR-TDT Tutorial\TDR_TDT 🛛 💽 Go				
×	Name 🔺	Size	Туре	Date Modified
~	SODIMM_TDR_TDT_1_result		File Folder	2012-8-1 16:2
	SODIMM_TDR_TDT_2_result		File Folder	2012-8-3 11:3
	C Trace_Pad_Library		File Folder	2012-8-3 11:4
	execution_time.log	3 KB	Text Document	2012-8-3 11:4
	🗐 memory_time.log	1 KB	Text Document	2012-8-3 11:4
	🗐 profile_spd.log	125 KB	Text Document	2012-8-3 11:4
	SODIMM_TDR_TDT.spd	3,355 KB	SPEED2000 Document	2012-7-27 12:
	SODIMM_TDR_TDT_1.spd	3,350 KB	SPEED2000 Document	2012-8-1 16:2
	SODIMM_TDR_TDT_1_spdsim.err	19 KB	ERR File	2012-8-1 17:2
	In the solution of the second	3,332 KB	SPEED2000 Document	2012-8-3 11:3