cadence

SPEED2000 TDR/TDT Simulation Tutorial

Product Version 16.6
July 2013

Document Updated on: June 6, 2013

Cadence Design Systems, Inc. (Cadence), 2655 Seely Ave., San Jose, CA 95134, USA.

Table of Contents

1 Introduction

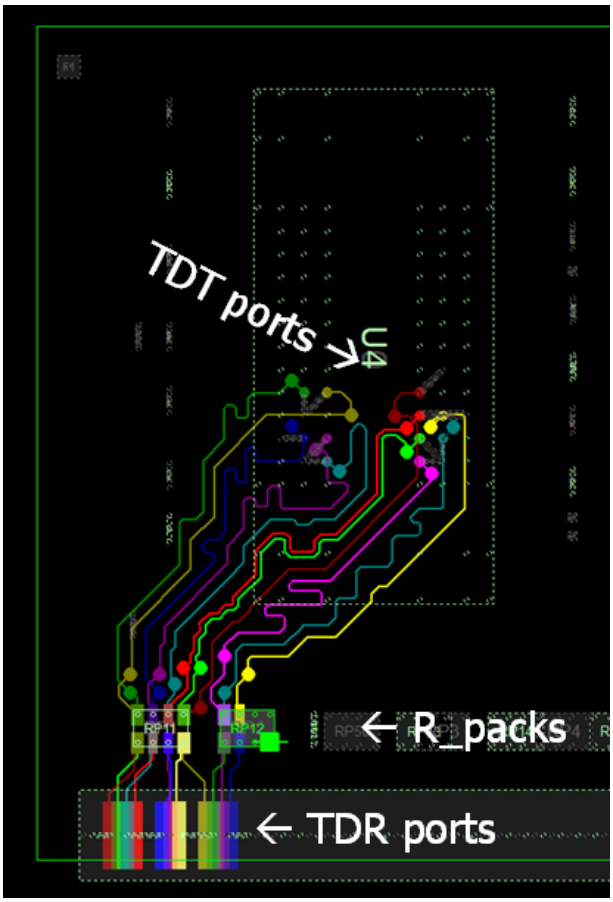
This tutorial demonstrates how to use TDR (Time-Domain Reflectometry)/TDT (Time-Domain Transmission) mode in SPEED2000 to simulate the measurement of TDR/TDT for signal integrity analysis.

The TDR/TDT mode in SPEED2000 enables user to easily check the signal's propagation, reflection and impedance discontinuity by step pulse response. The simulation results can better show voltage and impedance variation with time, helping user to check the quality of signal propagation channel. And the impedance discontinuous position on board can be calculated by the time and signal propagation velocity.

1.1 Overview

SPEED2000 provides the following functions in TDR/TDT mode:

- Create TDR/TDT circuits automatically
- Create TDR/TDT circuits manually
- Calculate impedance at TDR/TDT circuits
- Display TDR/TDT voltages



The TDR/TDT workflow leads user to:

- Setup layout

- Setup TDR/TDT
- Setup other simulation options
- Run simulation
- View simulation results

1.2 Sample Case

The original layout file used in this tutorial is:

- SODIMM_TDR_TDT.spd
  - It is located in: <INSTALL_DIR>\SpeedXP\Samples\SPEED2000\TDR-TDT Simulation\Examples_PreSetup\

The completed file (with step by step setup introduced in this tutorial) is also provided and located in:

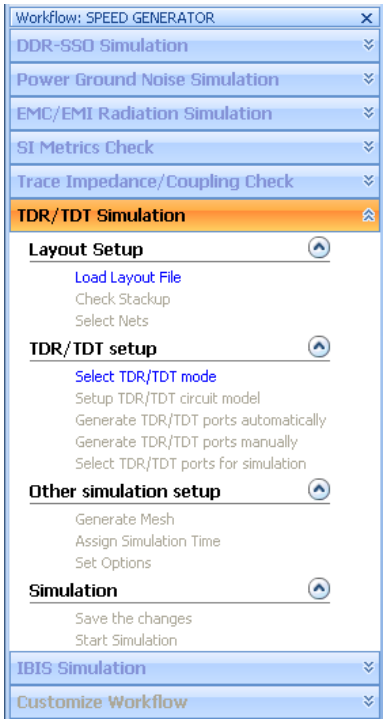
- <INSTALL_DIR>\SpeedXP\Samples\SPEED2000\TDR-TDT Simulation\Examples_PostSetup\

2 Layout Setup

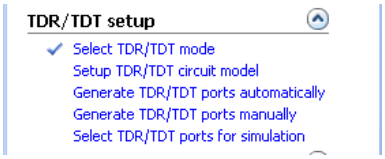
This chapter describes how to setup layout for TDR/TDT simulation.

2.1 Loading Layout File

1. Launch **SPEED2000 Generator.**
2. Select the **TDR/TDT Simulation** workflow.



3. Click **Load Layout File** to load SODIMM_TDR_TDT.spd.
4. Click **Select TDR/TDT mode** in the **Workflow** pane to enable TDR/TDT simulation mode.

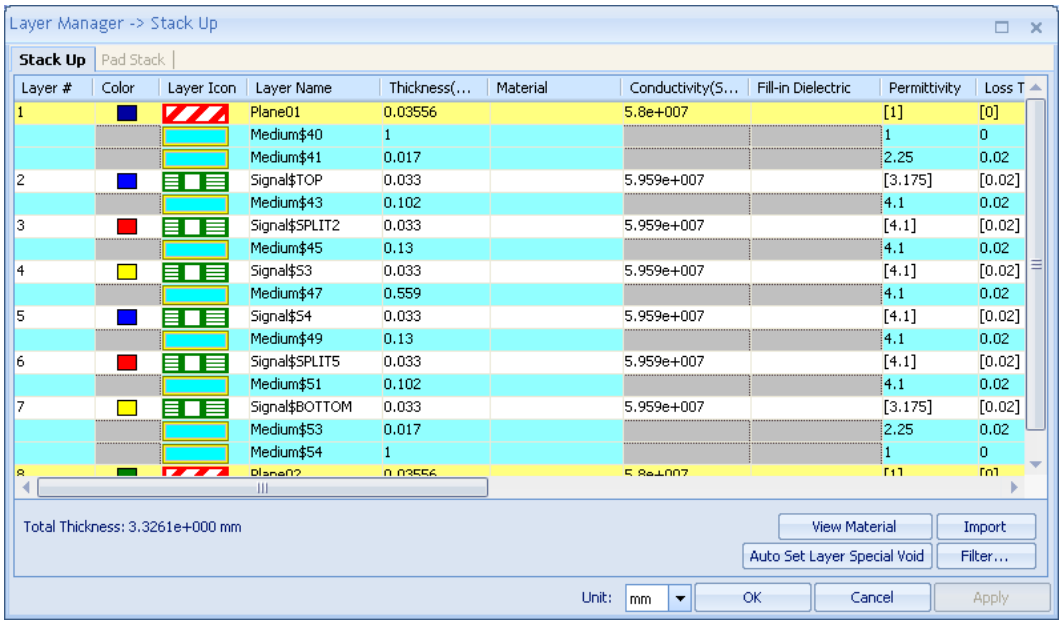


When enabled, a check mark ✓ appears next to the workflow step.

2.2 Checking Stackup

1. Click **Check Stackup** in the **Workflow** pane.

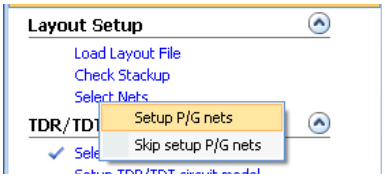
   The **Layer Manager -> Stack Up** window opens.



2. Check stackup and click **OK** when all settings are complete

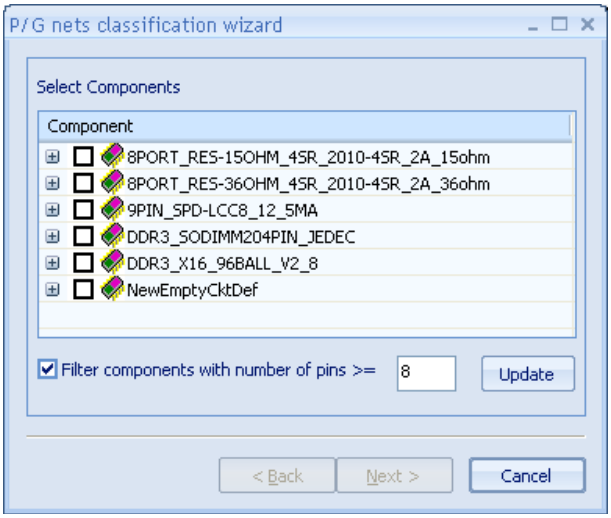
2.3 Selecting Nets

1. To setup P/G nets, click **Select Nets** in the **Workflow** pane.



2. Click **Setup P/G nets** from the pop-up menu list.

   The **P/G nets classification wizard** appears and leads you to setup P/G nets step by step.



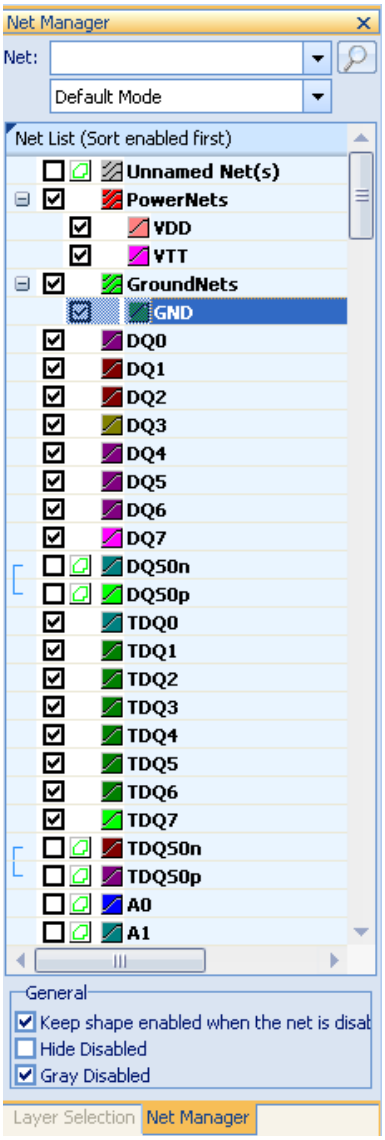
NOTE!	If the P/G nets are setup already (like the example case in this tutorial), ignore this step or just click **Skip setup P/G nets**.

3 TDR/TDT Single Ended Simulation

This chapter demonstrates how to setup circuit model, generate ports, run simulation and view simulation results for TDR/TDT single ended.

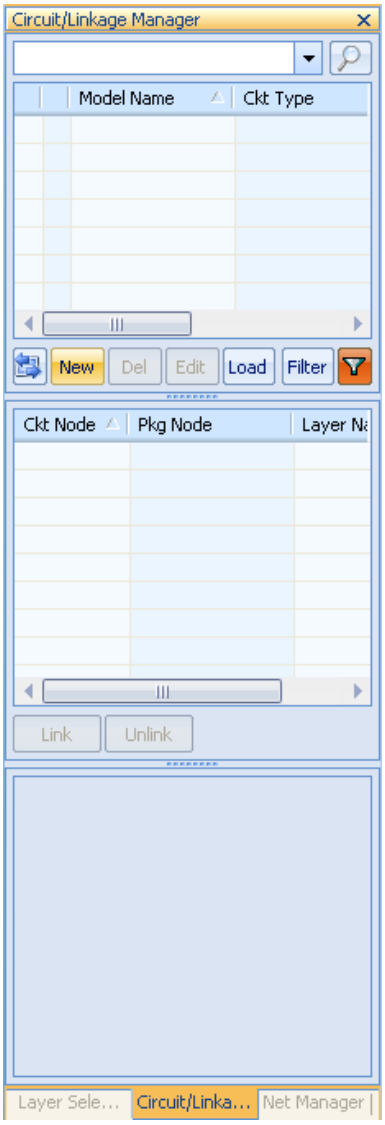
3.1 Setting Up TDR/TDT Circuit Model

1. Select and enable the desired nets in **Net Manager** as the following figure shows.



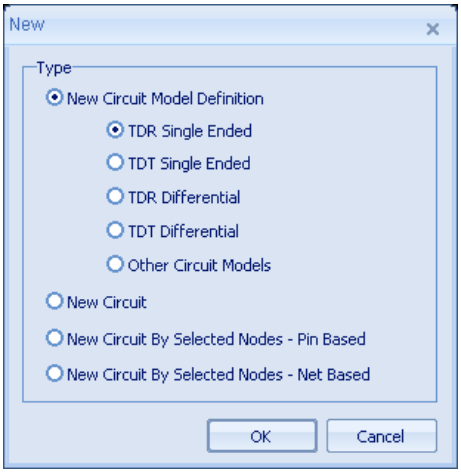
2. Click **Setup TDR/TDT circuit model** in the **Workflow** pane.

   The **Circuit/Linkage Manager** opens.



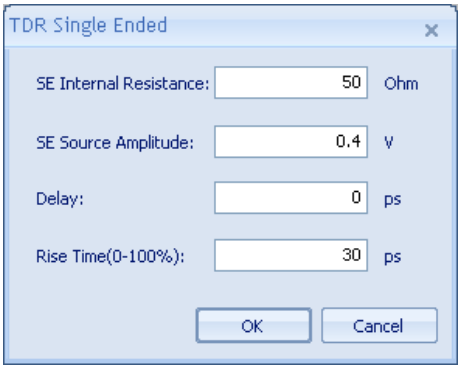
3. Click **New**.

   The **New** window opens.



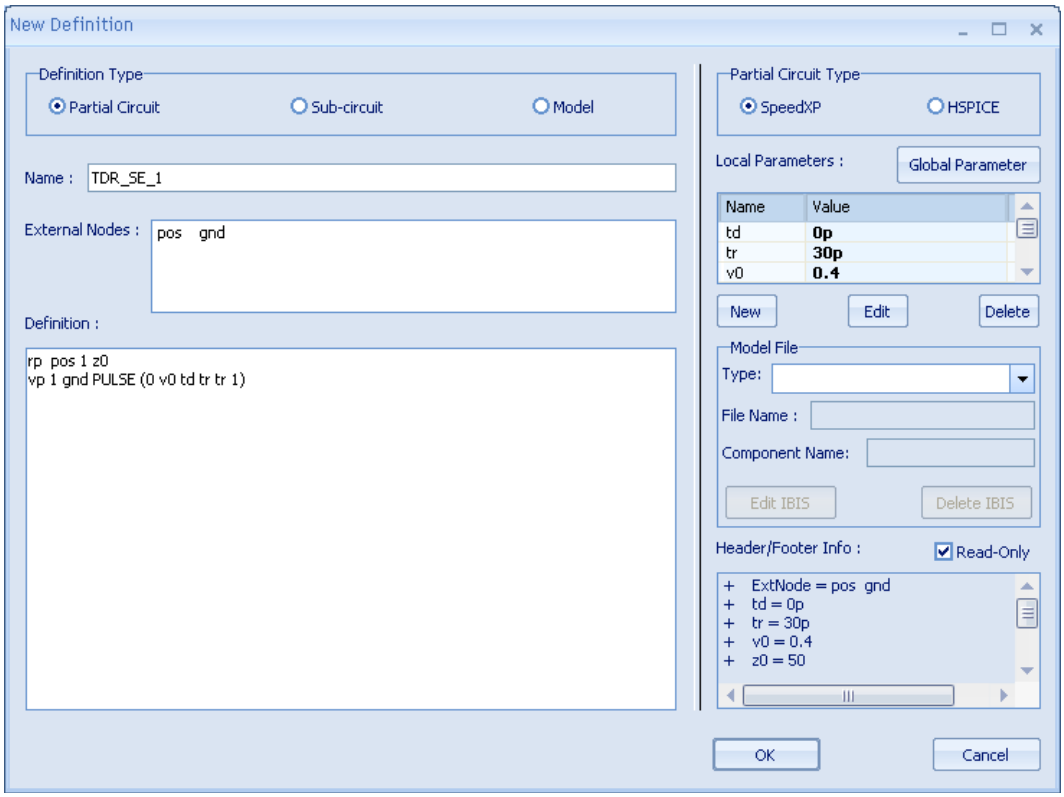
4. Select **TDR Single Ended**.
5. Click **OK**.

   The **TDR Single Ended** window opens.



6. Set the parameters for TDR single-ended as desired.
7. Click **OK**.

   The **New Definition** window opens, displaying the detailed information of the newly created circuit model definition.

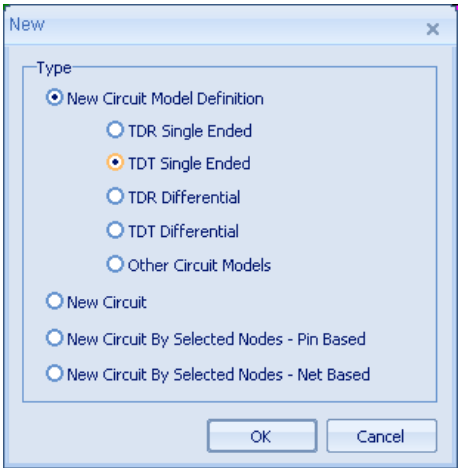


   The TDR source is a voltage source with step waveform. By default:

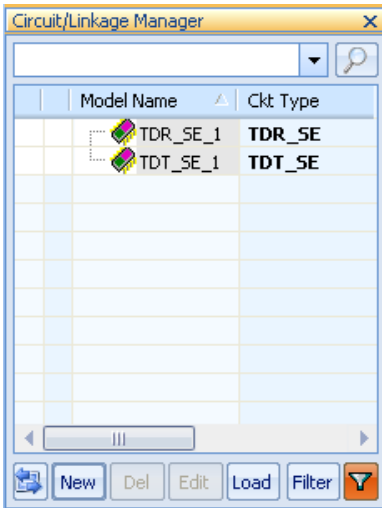
   - **SE Internal Resistance** – 50ohm
   - **SE Source Amplitude** – 0.4v
   - **Delay** – 0ps
   - **Rise Time** – 30ps

8. Click **OK** to quit the **New Definition** window when all settings are complete.

9. Repeat step 3 to 8 to create TDT single ended circuit model definition. Remember to select **TDT Single Ended** in the **New** window.

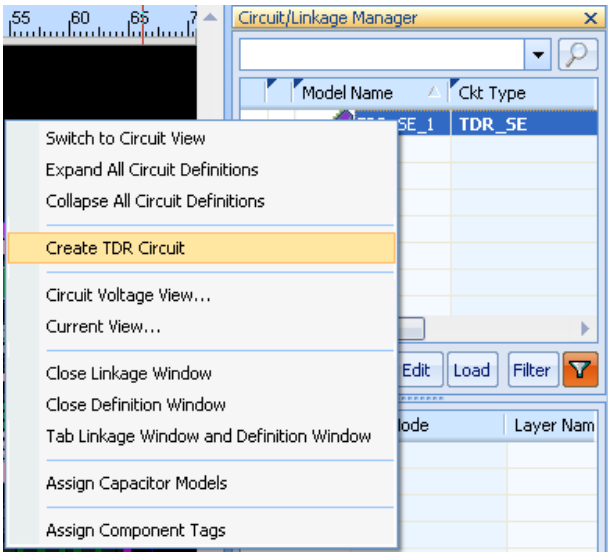


The newly created circuit model definitions can be viewed in **Circuit/Linkage Manager**.

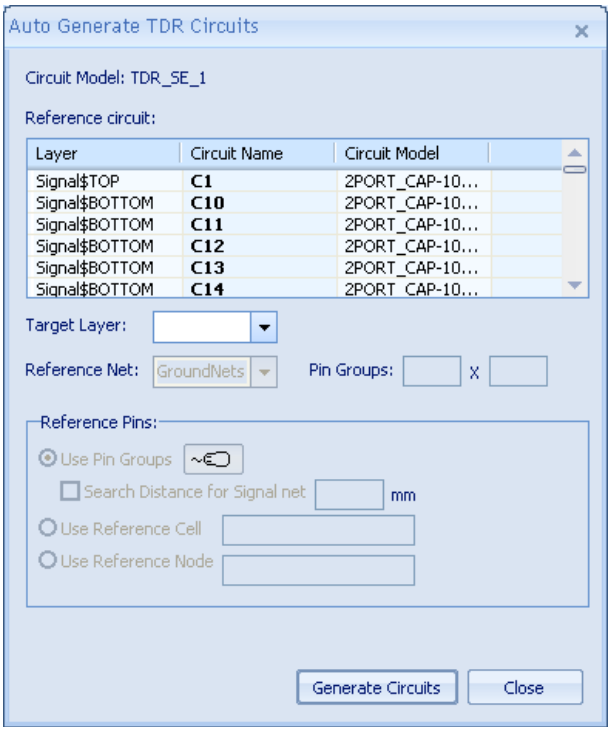


3.2 Generating TDR/TDT Ports Automatically

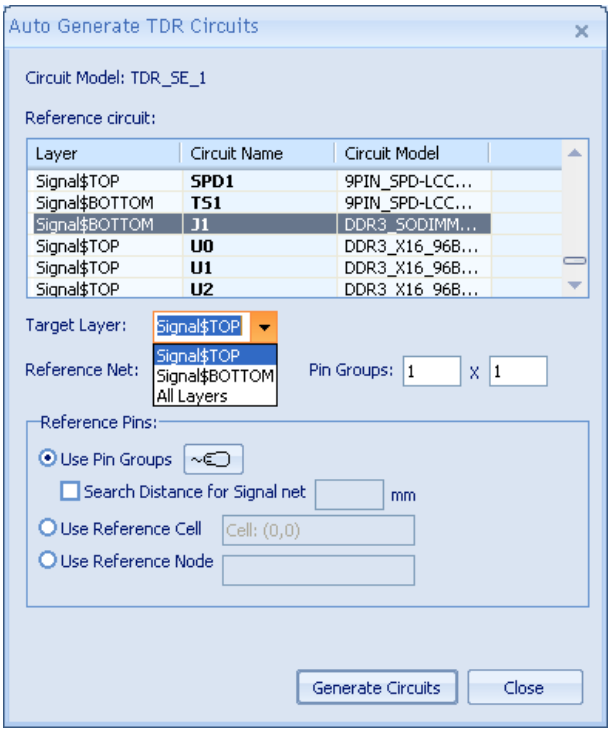
1. Right-click **TDR_SE_1** and click **Create TDR Circuit** from the pop-up menu list.



The **Auto Generate TDR Circuits** window opens.

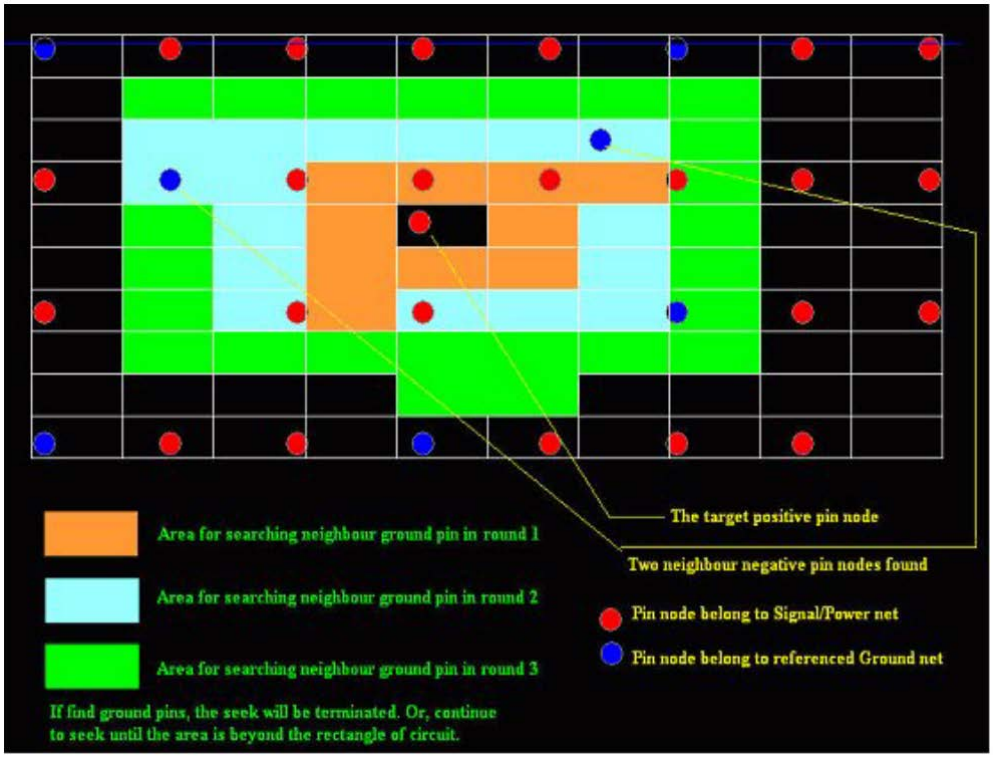


2. Set the parameters as following:
   - Reference circuit: **J1**
   - Target Layer: **Signal$TOP**



Description of Auto Generate TDR Circuits Window

- **Target Layer** – Select the layer pins
- **Reference Net** – List all the enabled nets in the GroundNets group as well as GroundNets which include all the ground nets:
  - The default selection is GroundNets. If GroundNets is selected, all ground nets in the list serve as reference nets. The Negative Terminals are the pins of these reference nets in circuit generation.
  - If an individual ground net (not the group name GroundNets) is selected, circuits are generated in each cell or cell group for signal nets, power nets and other ground nets. The negative terminals are the pins of the selected reference net.
- **Pin Groups** – Divide the pins into rectangular cells from which the circuits will be generated
  - Left number – Columns of cells
  - Right number – Rows of cells
  - Default value – 1x1
- **Reference Pins** – Rules to determine the negative nodes in the automatic circuit generation. Three options are available:
  - Use Pin Groups
    Circuits are generated for each pin of the Power, Ground and Signal nets. If there is no pin for the reference net, the neighbor cells are searched until the nearest ground pin is found. The nearest ground pin serves as negative terminals for the cell, as shown in the example. The aim is that the same reference pins should be used in as few cells as possible. This approach is called Use Pin Groups.

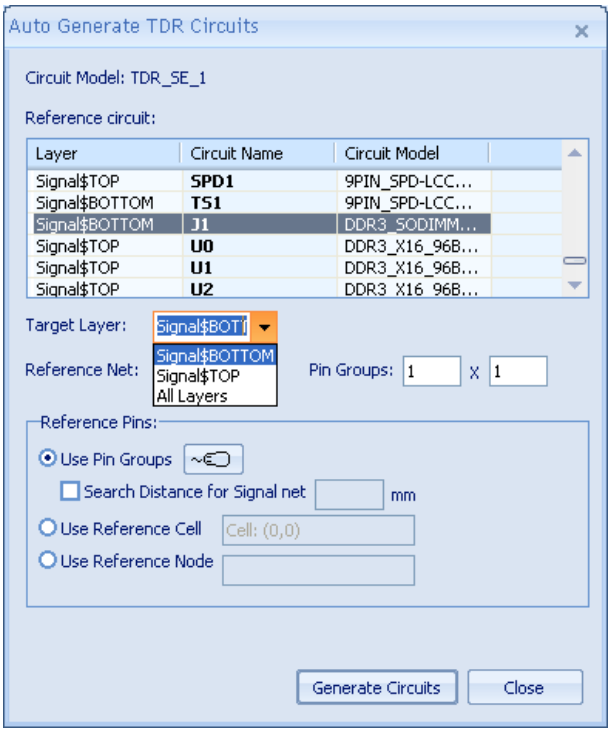


- Use Reference Cell
- Use Reference Node

3. Click the **Generate Circuits** button.

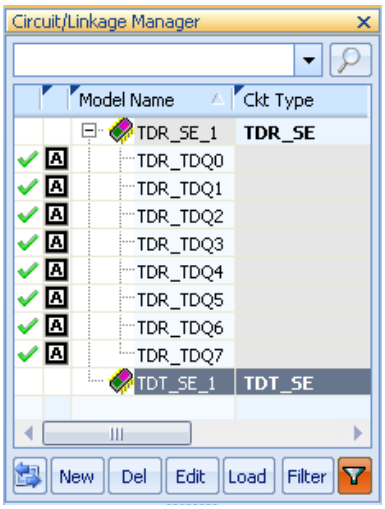
   The TDR circuits on top layer are automatically generated.

4. To generate TDR circuits on bottom layer, set the parameters as following:
   - Reference circuit: **J1**
   - Target Layer: **Signal$BOTTOM**

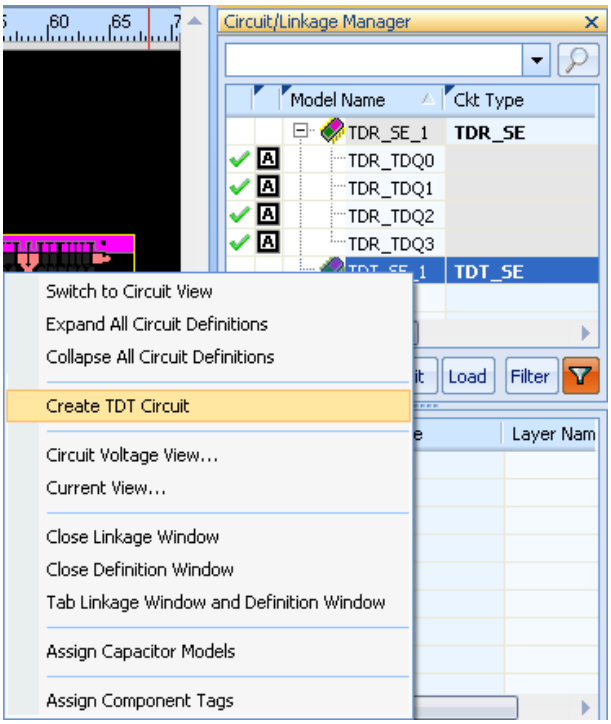


The TDR circuits on bottom layer are automatically generated.

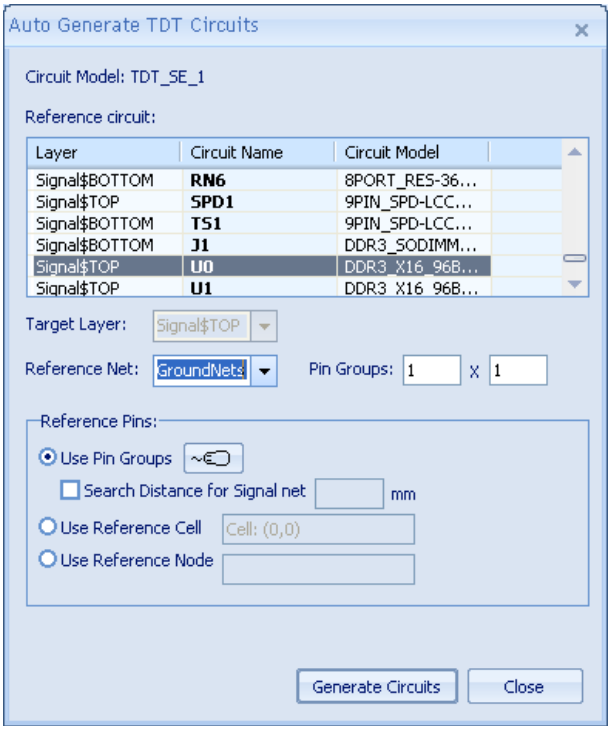
5. Click **Close** to quit the **Auto Generate TDR Circuits** window.
6. View the newly generated TDR circuits in **Circuit/Linkage Manager** by selecting Setup > Circuit/Linkage Manager…



7. Right-click **TDT_SE_1** and click **Create TDT Circuit** from the pop-up menu list.

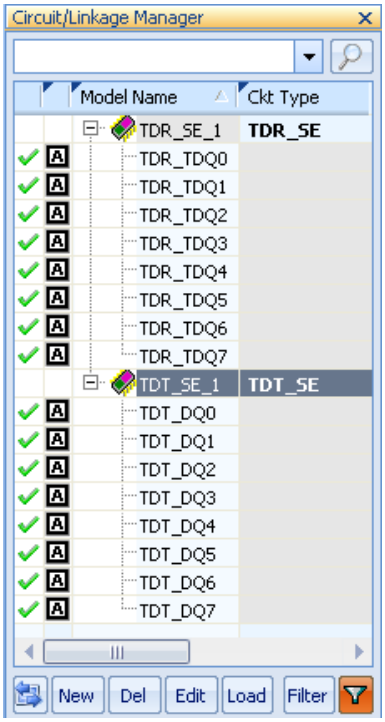


8. In the **Auto Generate TDT Circuits** window, set the parameters like the following:
   - Reference circuit: **U0**
   - Referent Net: **GroundNets**



9. Click the **Generate Circuits** button.

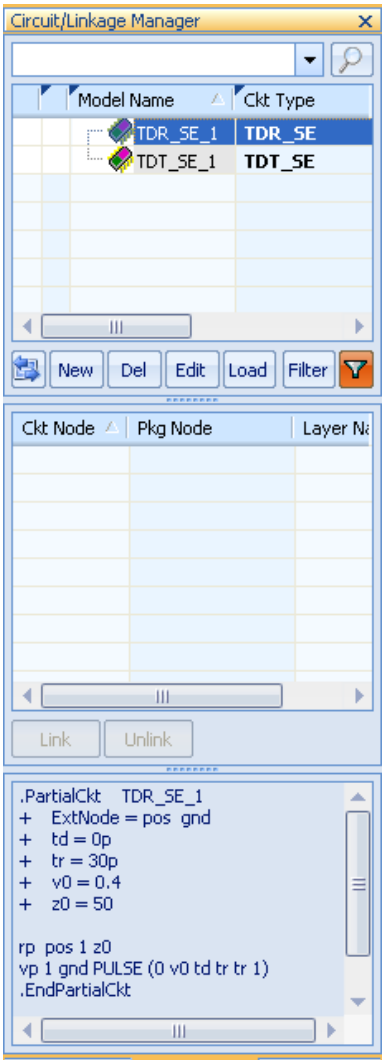
   The TDT circuits are automatically generated. The circuits can be viewed in **Circuit/Linkage Manager**.



3.3 Generating TDR/TDT Ports Manually

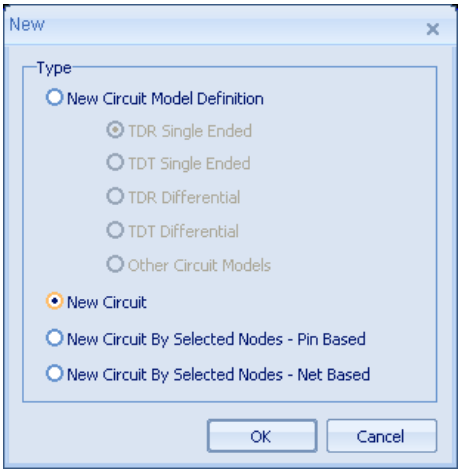
This section introduces how to generate TDR/TDT ports manually if the auto-generated ports do not meet your requirements or you hope to generate ports manually.

1. In **Circuit/Linkage Manager**, select **TDR_SE_1**.



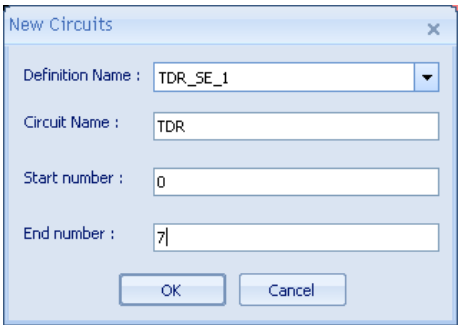
2. Click **New**.

   The **New** window opens.



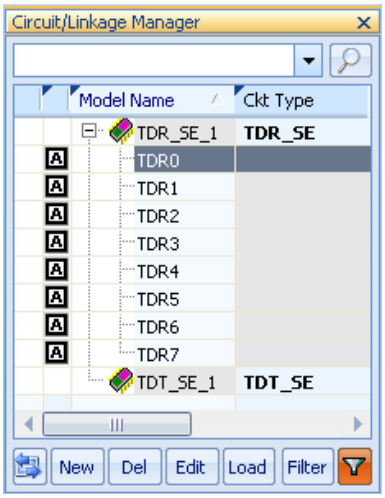
3. Select **New Circuit**.
4. Click **OK**.

The **New Circuits** window opens.



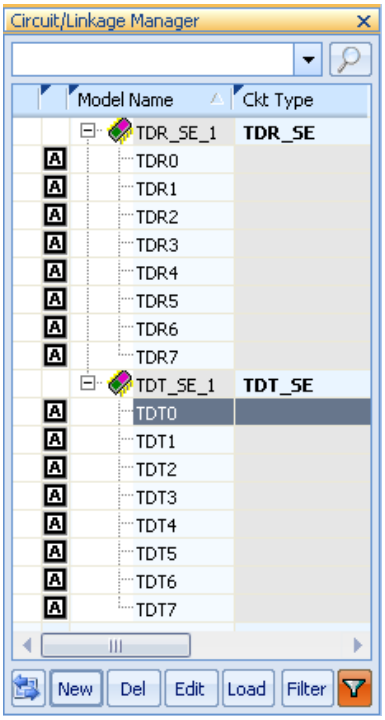
5. Select TDR_SE_1 as the definition name.
6. Enter a circuit name (**TDR** in this example).
7. Enter the start and end number if you want to generate more than one port (**0** and **7** in this example).
8. Click **OK**.

   8 new circuits with the name TDR0-TDR7 are generated. The ports can be viewed in **Circuit/Linkage Manager**.



9. To generate TDT ports manually, select **TDT_SE_1** in **Circuit/Linkage Manager** and repeat step 2 to 8.

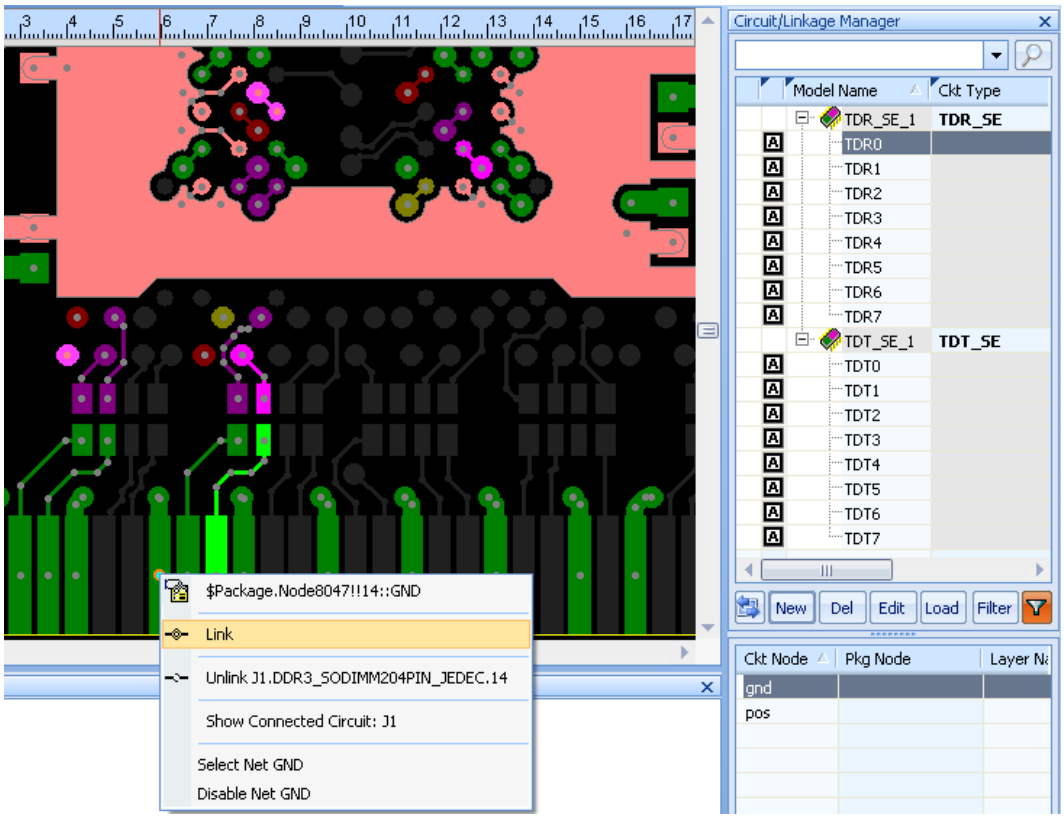
   All circuits generated can be viewed in **Circuit/Linkage Manager**.



3.3.1 Linking TDR/TDT Circuits to Board Manually

1. Select the desired circuit in **Circuit/Linkage Manager**, for example, **TDR0**.

   The information of the selected circuit node is listed in the **Package Linkage Assignment** pane.

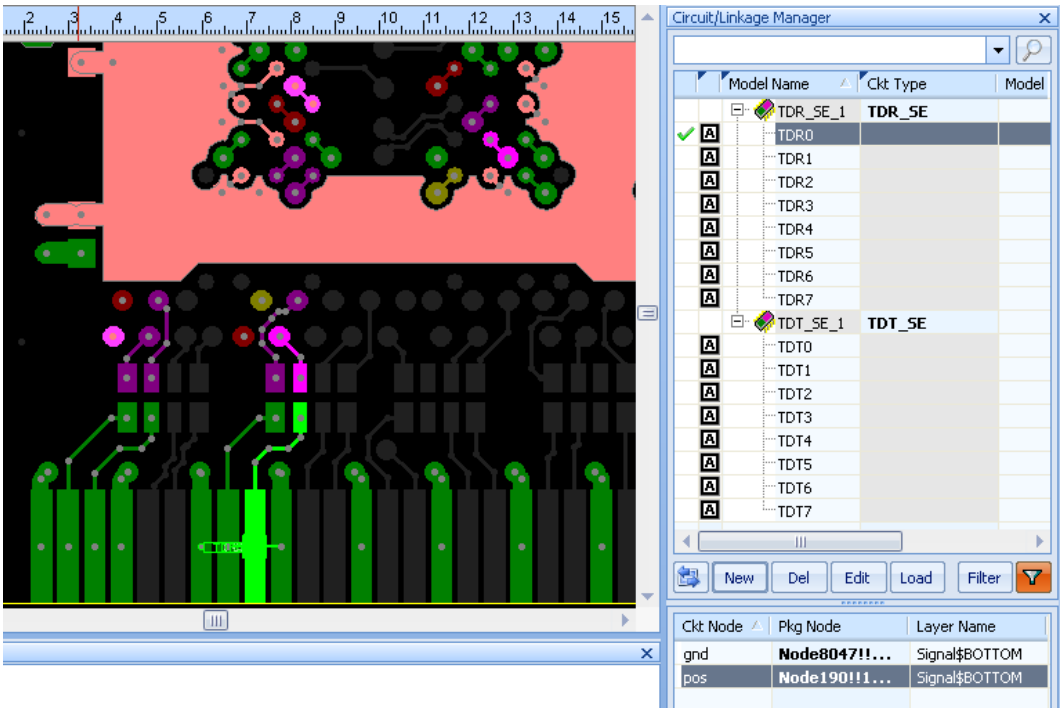


2. Highlight the circuit node you want to link to the board in the **Package Linkage Assignment** pane, for example, **gnd**.
3. Right-click the desired node on board and click **Link** from the pop-up menu list.

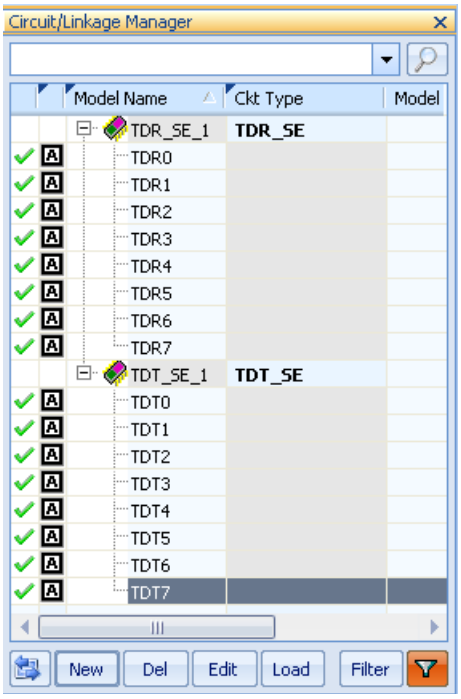
NOTE!	Make sure the package node you want is on the active layer.

4. Repeat step 2 to 3 to link the other circuit node.

   When both circuit nodes are successfully linked to package nodes, a green mark ✔ appears ahead of the circuit, and the linkage information is listed in the **Package Linkage Assignment** pane.



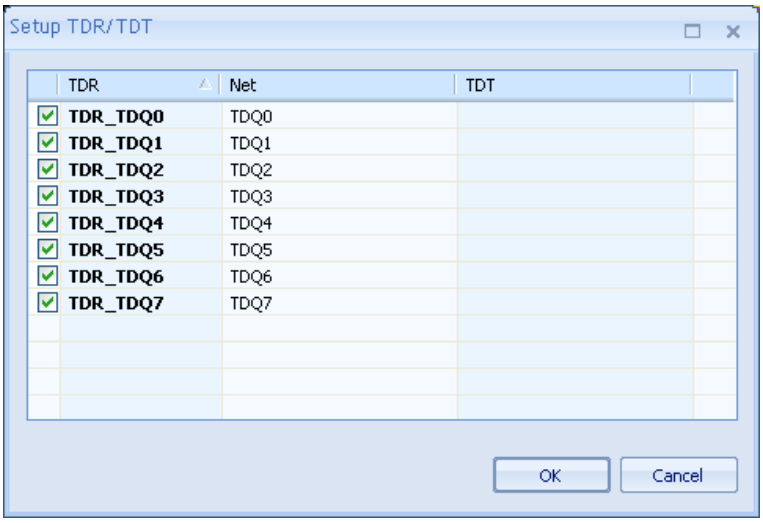
5. Repeat step 1 to 3 to link all circuits to board. A green mark ✔ ahead of the active icon A shows it is successfully linked.



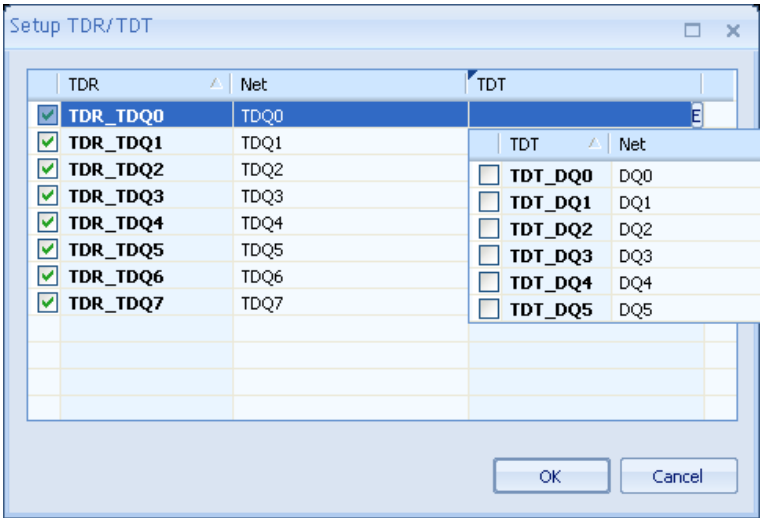
3.4 Selecting Ports for Simulation

1. Click **Select TDR/TDT ports for simulation** in the **Workflow** pane.

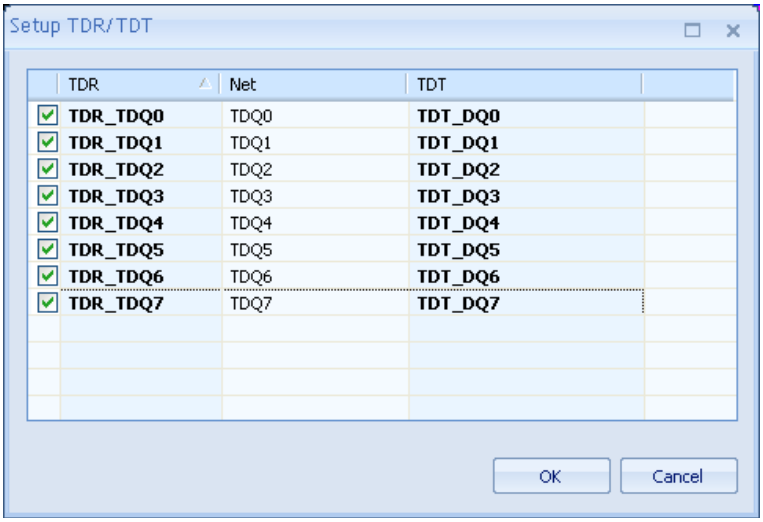
   The **Setup TDR/TDT** window opens, displaying all available ports. All TDR ports are selected by default.



2. Double-click  under TDT column to select TDT ports for simulation



A green checkmark  shows the port is selected. Check the ports as the following figure shows.

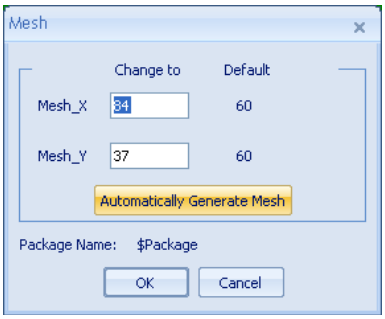


3. Click **OK** to quit the window.

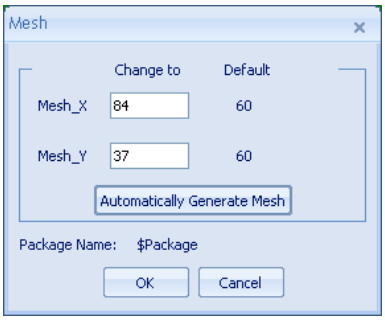
3.5 Running Simulation

1. Click **Generate Mesh** in the **Workflow** pane.

   The **Mesh** window opens.



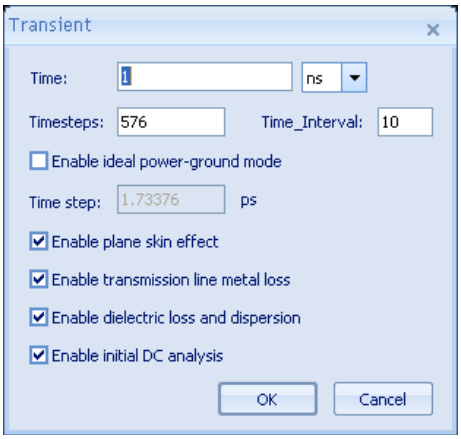
2. Click the **Automatically Generate Mesh** button.



   The values of **Mesh_X** and **Mesh_Y** are automatically generated.

3. Click **OK** to quit the **Mesh** window.
4. Click **Assign Simulation Time** in the **Workflow** pane.

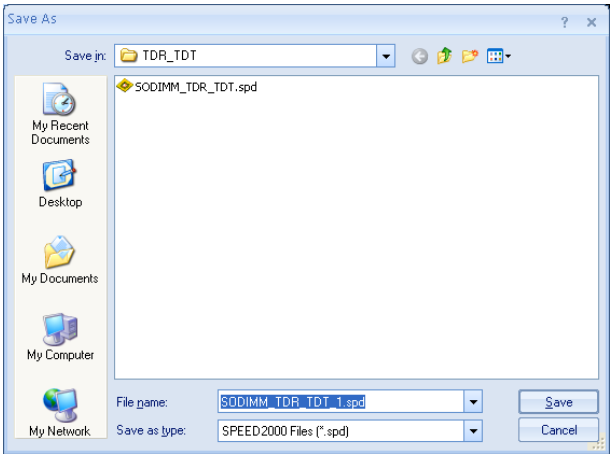
   The **Transient** window opens.



5. Set the simulation parameters as the above figure shows.
6. Click **OK** to quit the **Transient** window.
7. Click **Save the changes** in the **Workflow** pane.

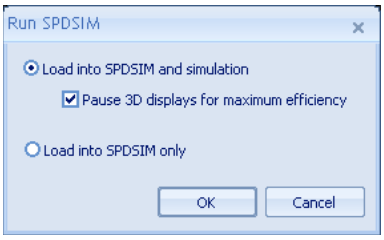
   The **Save As** window opens.

8. Browse to the desired folder and enter a name (for example, **SODIMM_TDR_TDT_1**) if you want to save as a different file.



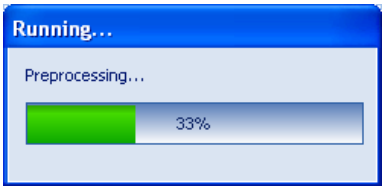
9. Click **Start Simulation** in the **Workflow** pane.

   The **Run SPDSIM** window opens.



10. Click **OK**.

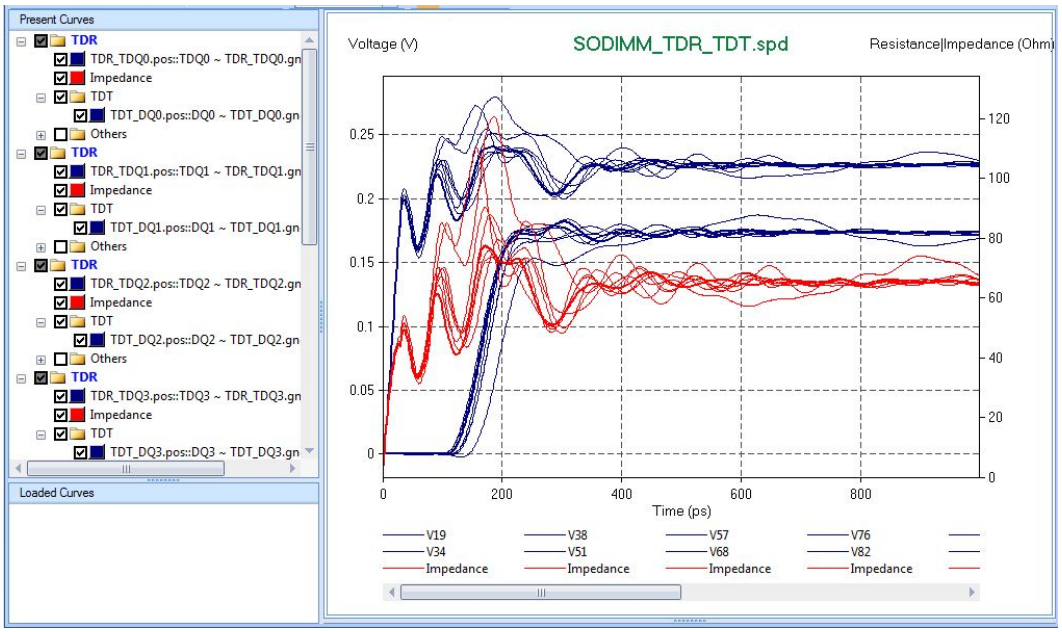
    SPDSIM starts to simulate. A blue bar appears to show the progress of simulation.



NOTE!	Although multiple TDRs are selected while sweeping, SPEED2000 simulates only one of the TDRs and disconnects other TDRs during each simulation.

3.6 Viewing Result

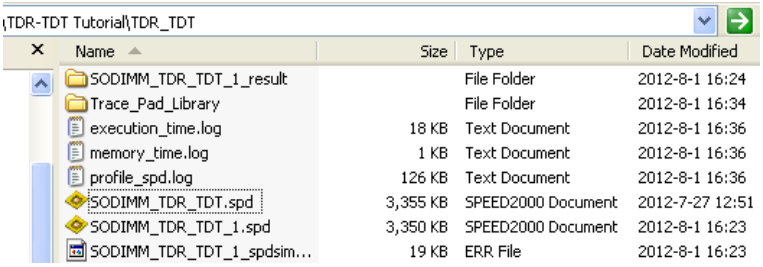
When simulation is complete, a result window appears to show the simulation results.



The results include:

- Impedance at the TDR Port
- Voltage at the TDR Port
- Voltage at the TDT Port
- Other Voltages/Currents Views

A folder (for example, **SODIMM_TDR_TDT_1_result**) with results in is created under the same location of the case.

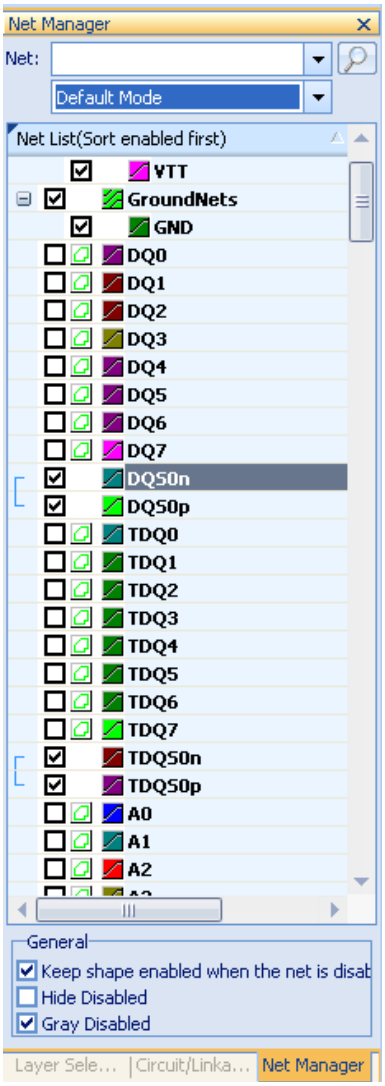


4 TDR/TDT Differential Simulation

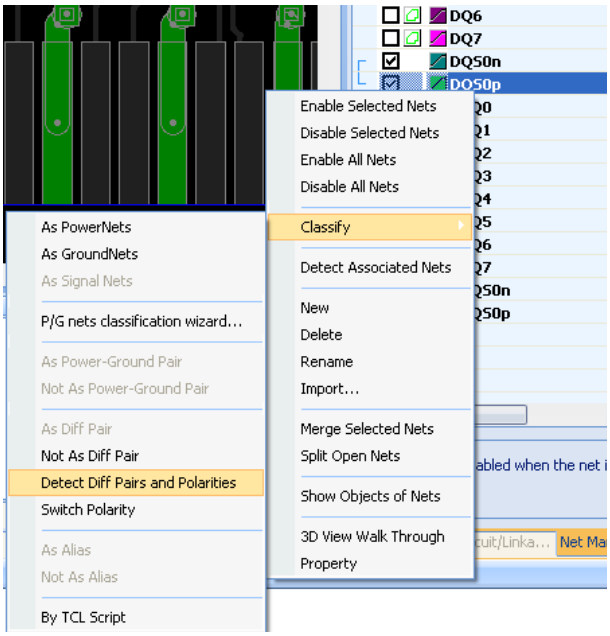
This chapter demonstrates how to setup circuit model, generate ports, run simulation and view simulation results for TDR/TDT differential.

4.1 Selecting Differential Nets

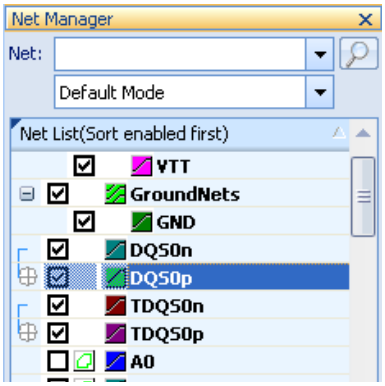
1. Select and enable the desired differential nets in **Net Manager** as the following figure shows.



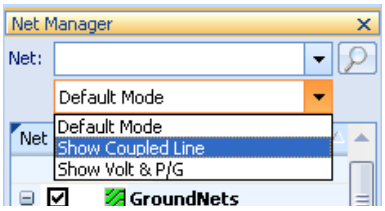
2. Right-click the differential nets and select Classify > Detect Diff Pairs and Polarities.



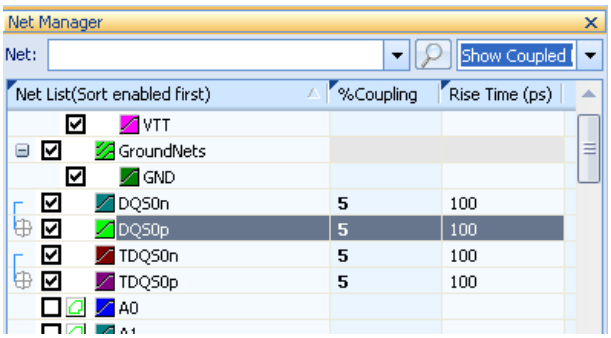
The differential pairs and polarities are detected automatically.



3. Click **Show Coupled Line** to switch to the coupling mode.



4. Set the parameters as the following:
   - %Coupling: **5**
   - Rise Time (ps): **100**

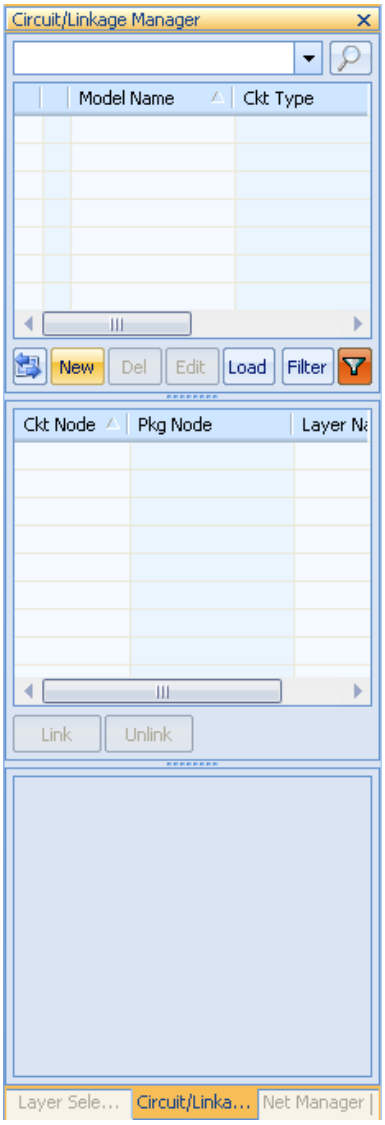


NOTE!	Do NOT forget to switch to the coupling mode and set the coefficient of Coupling and Rise Time, otherwise it would be considered as single ended during simulation.

4.2 Setting Up TDR/TDT Circuit Model

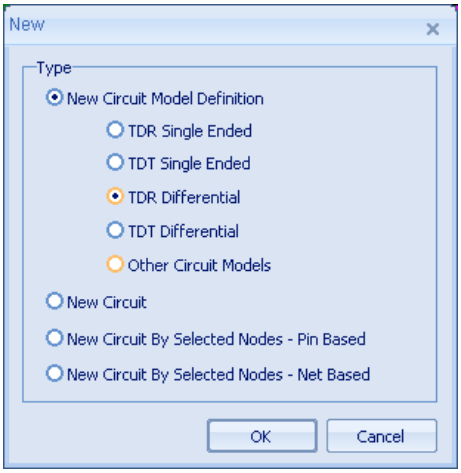
1. Click **Setup TDR/TDT circuit model** in the **Workflow** pane.

   The **Circuit/Linkage Manager** opens.



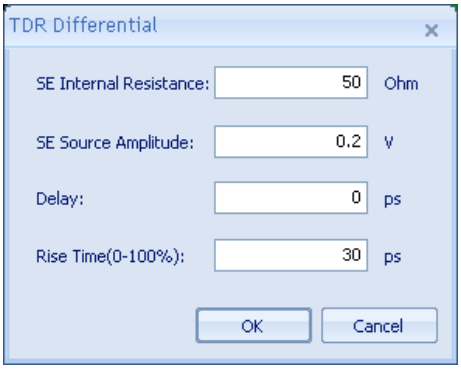
2. Click **New**.

   The **New** window opens.



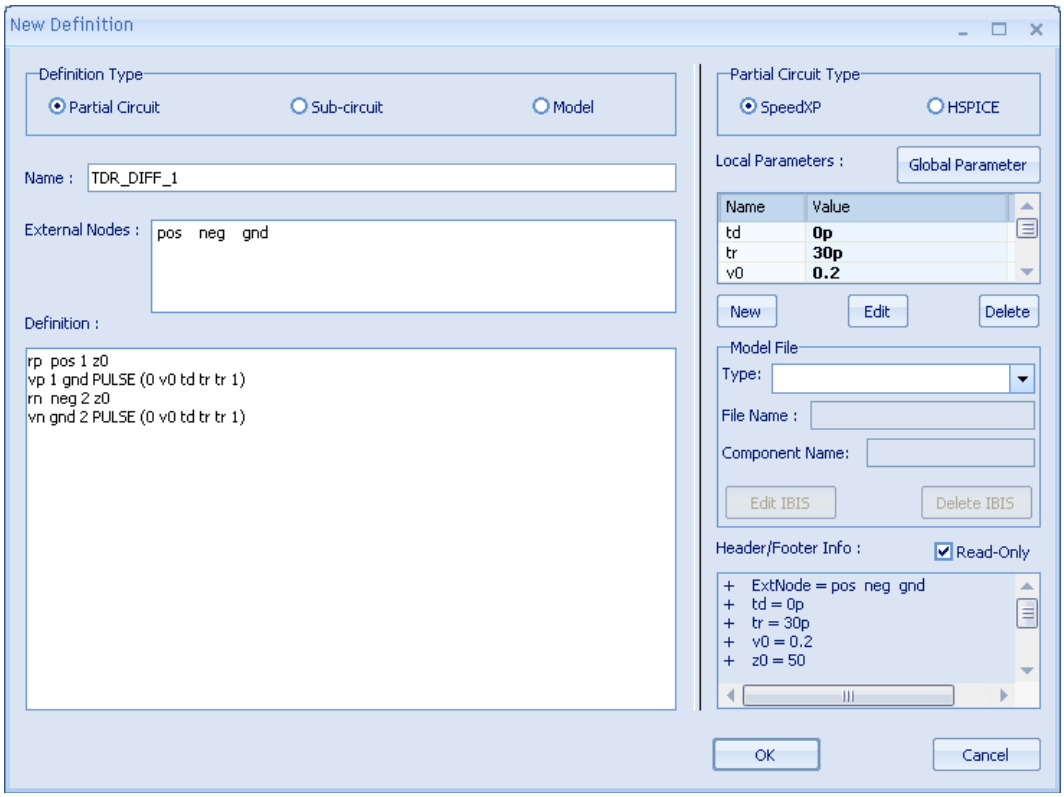
3. Select **TDR Differential**.
4. Click **OK**.

   The **TDR Differential** window opens.

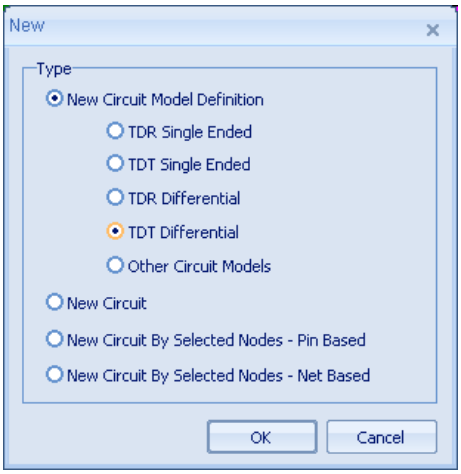


5. Set the parameters for TDR differential as desired.
6. Click **OK**.

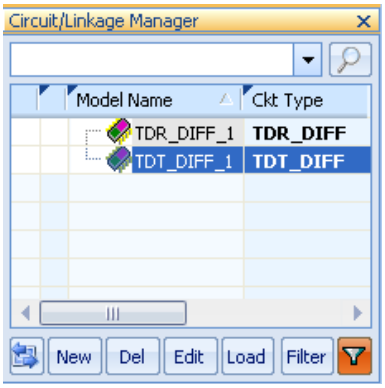
   The **New Definition** window opens, displaying the detailed information of the newly created circuit model definition.



7. Click **OK** to quit the **New Definition** window when all settings are complete.
8. Repeat step 2 to 7 to create TDT differential circuit model definition. Remember to select **TDT Differential** in the **New** window.

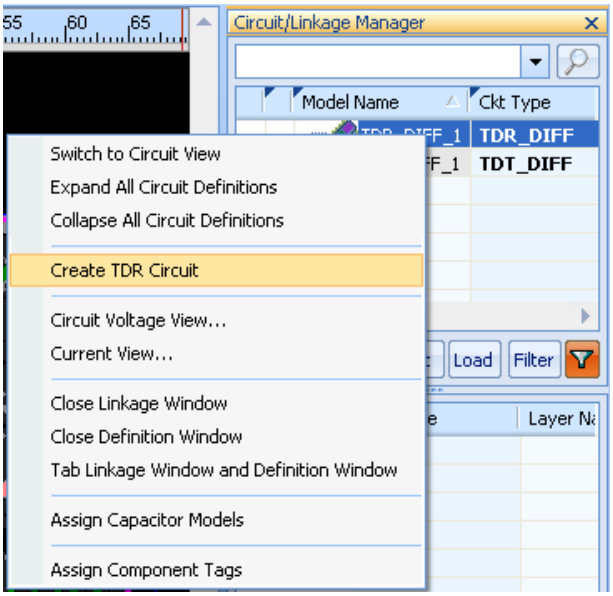


The newly created circuit model definitions can be viewed in **Circuit/Linkage Manager**.

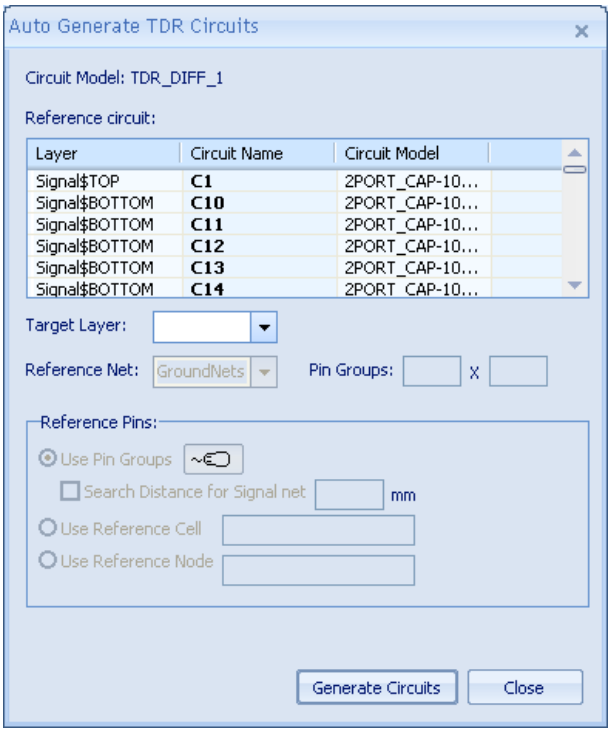


4.3 Generating TDR/TDT Ports Automatically

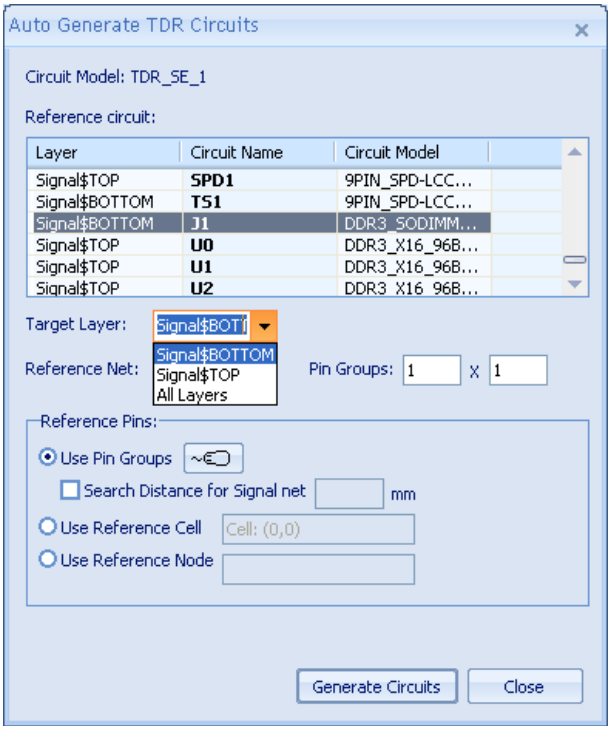
1. Right-click **TDR_DIFF_1** and click **Create TDR Circuit** from the pop-up menu list.



The **Auto Generate TDR Circuits** window opens.



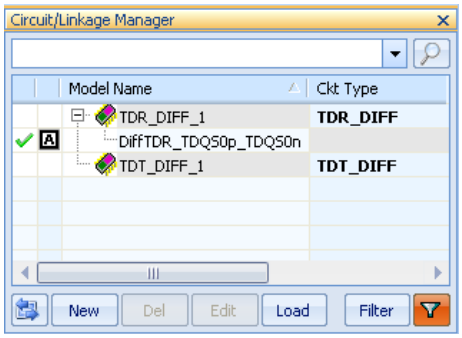
2. Set the parameters as following:
   - Reference circuit: **J1**
   - Target Layer: **Signal$BOTTOM**



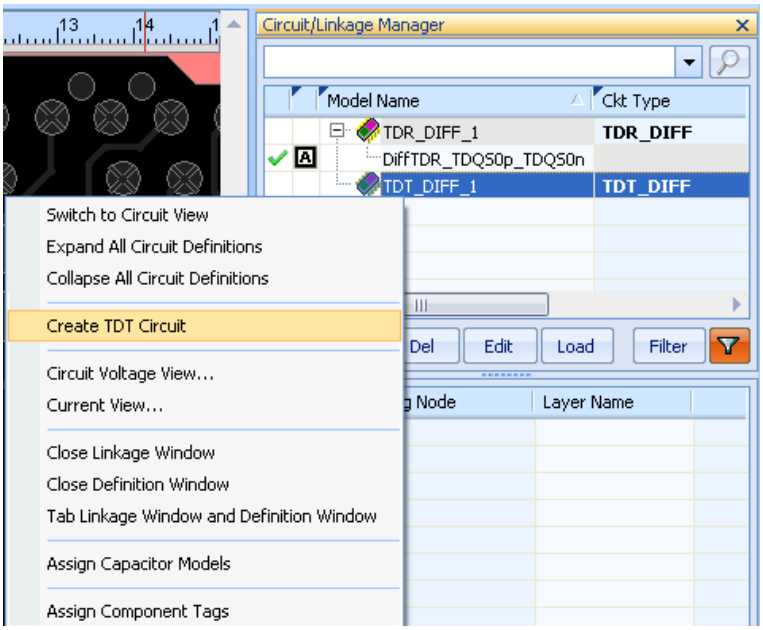
The TDR circuits on bottom layer are automatically generated.

3. Click **Close** to quit the **Auto Generate TDR Circuits** window.

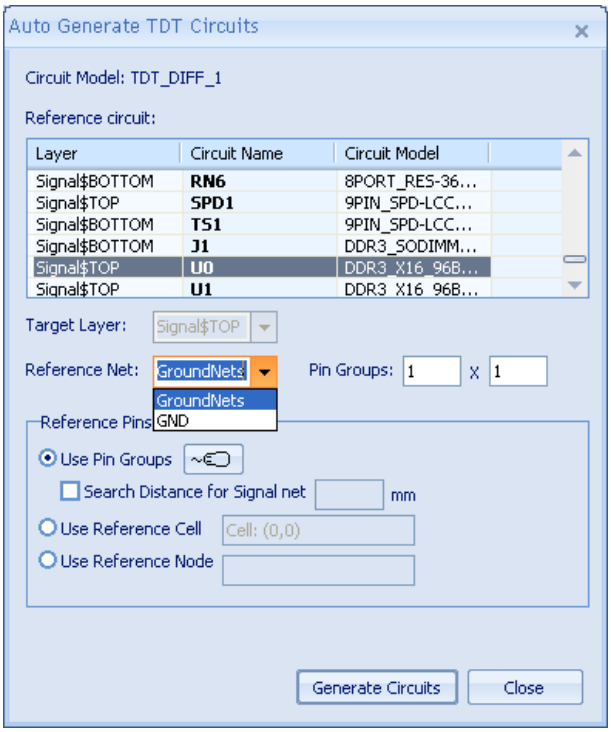
4. View the newly generated TDR circuits **Circuit/Linkage Manager** by selecting Setup > Circuit/Linkage Manager…



5. Right-click **TDT_DIFF_1** and click **Create TDT Circuit** from the pop-up menu list.

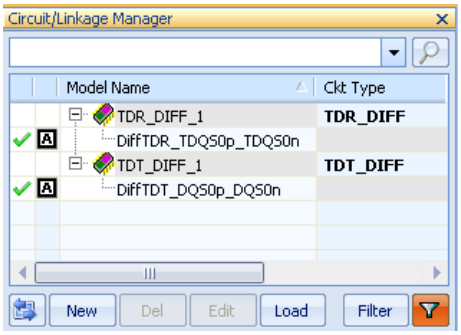


6. In the **Auto Generate TDT Circuits** window, set the parameters like the following:
   - Reference circuit: **U0**
   - Referent Net: **GroundNets**



7. Click the **Generate Circuits** button.

   The TDT circuits are automatically generated. The circuits can be viewed in **Circuit/Linkage Manager**.



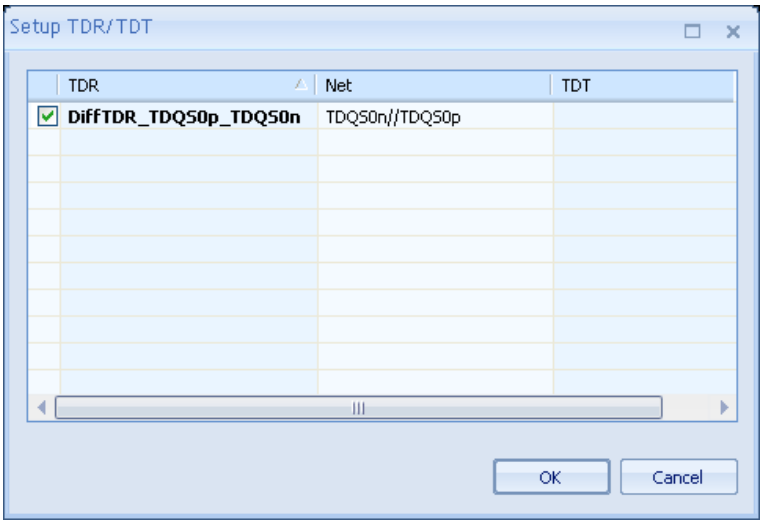
4.4 Generating TDR/TDT Ports Manually

To generate TDR/TDT differential ports manually, refer to Section ***3.3 Generate TDR/TDT Ports Manually***.

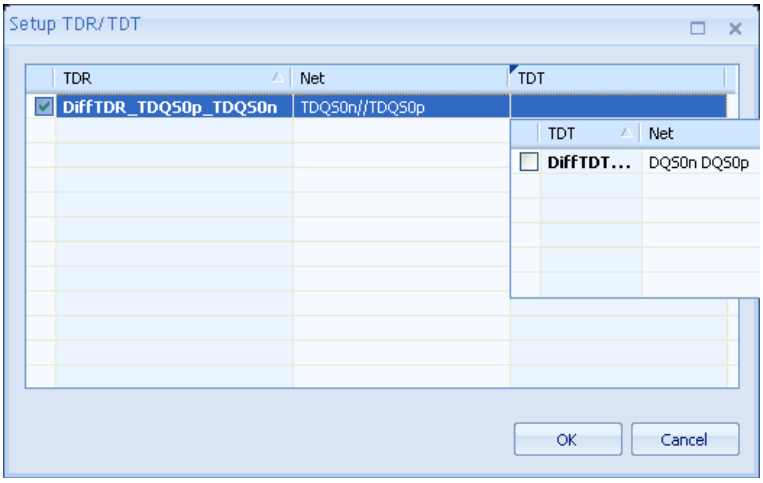
4.5 Selecting Ports for Simulation

1. Click **Select TDR/TDT ports for simulation** in the **Workflow** pane.

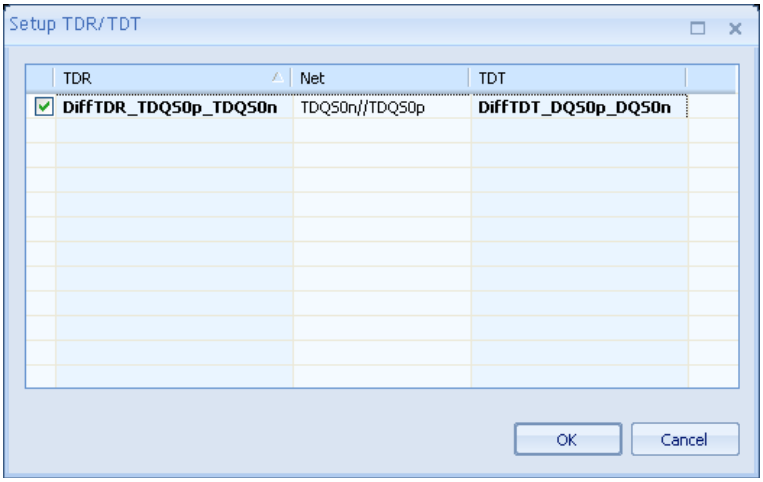
   The **Setup TDR/TDT** window opens, displaying all available ports. All TDR ports are selected by default.



2. Double-click  under TDT column to select TDT ports for simulation



A green checkmark  shows the port is selected. Check the ports as the following figure shows.

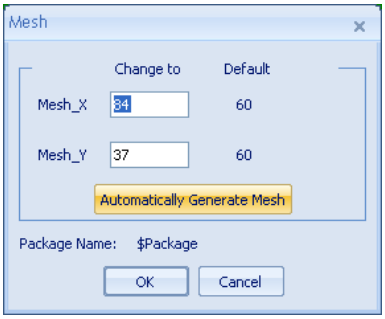


3. Click **OK** to quit the window.

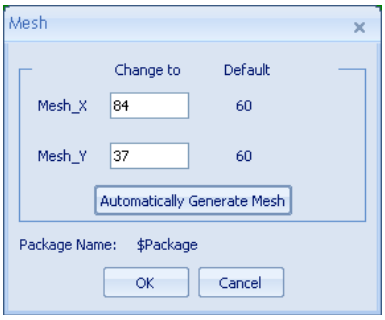
4.6 Running Simulation

1. Click **Generate Mesh** in the **Workflow** pane.

   The **Mesh** window opens.



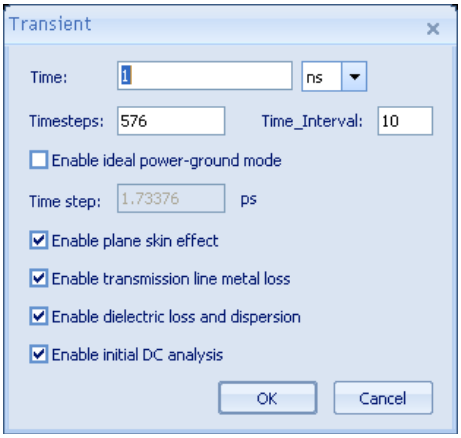
2. Click the **Automatically Generate Mesh** button.



   The values of **Mesh_X** and **Mesh_Y** are automatically generated.

3. Click **OK** to quit the **Mesh** window.
4. Click **Assign Simulation Time** in the **Workflow** pane.

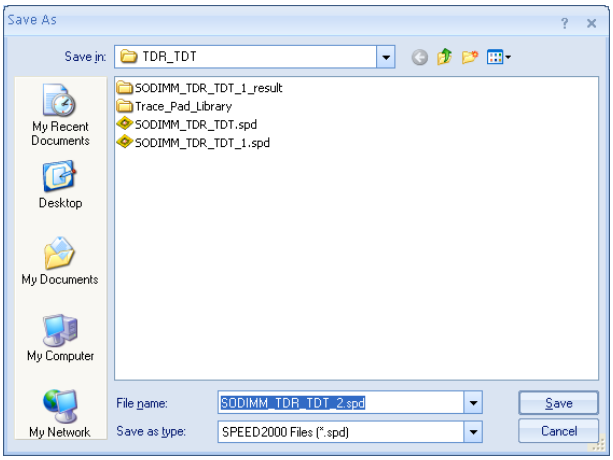
   The **Transient** window opens.



5. Set the simulation parameters as the above figure shows.
6. Click **OK** to quit the **Transient** window.
7. Click **Save the changes** in the **Workflow** pane.

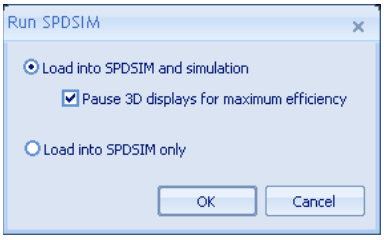
   The **Save As** window opens.

8. **Browse** to the desired folder and enter a name (for example, **SODIMM_TDR_TDT_2**) if you want to save as a different file.



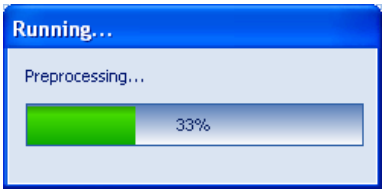
9. **Click Start Simulation** in the **Workflow** pane.

   The **Run SPDSIM** window opens.



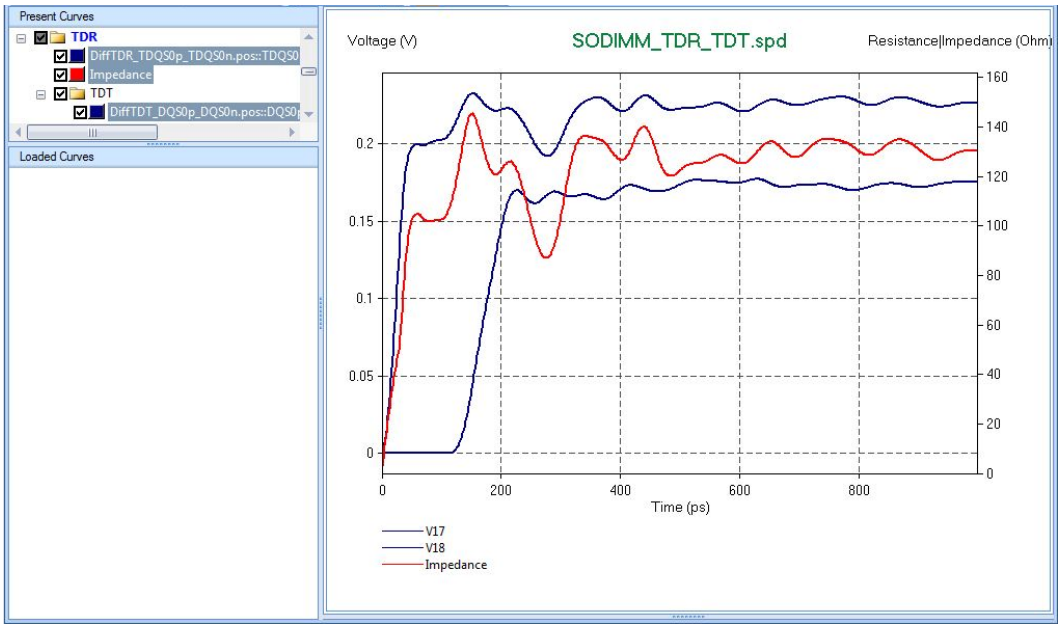
10. Click **OK**.

    SPDSIM starts to simulate. A blue bar appears to show the progress of simulation.



4.7 Viewing Results

When simulation is complete, a result window appears to show the simulation results.



A folder (for example, **SODIMM_TDR_TDT_2_result**) with results in is created under the same location of the case.