SFF Committee documentation may be purchased in hard copy or electronic form. SFF specifications are available at ftp://ftp.seagate.com/sff

SFF Committee

# SFF-8436 Specification

for

# QSFP+ COPPER AND OPTICAL MODULES

Rev 3.1 April 22, 2009

Secretariat: SFF Committee

Abstract: This specification defines the electrical (copper), the optical, and the mechanical characteristics of the pluggable Quad SFP+ Module/direct attach cable plug.

This document provides a common specification for systems manufacturers, system integrators, and suppliers of drives. This is an internal working document of the SFF Committee, an industry ad hoc group. This specification is intended to supersede INF-8438 by adding support for 10Gbps data rates and updates to the mechanical specification

This specification is made available for public review, and written comments are solicited from readers. Comments received by the members will be considered for inclusion in future revisions of this specification.

Support: This specification is supported by the identified member companies of the SFF Committee.

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## EXPRESSION OF SUPPORT BY MANUFACTURERS

The following member companies of the SFF Committee voted in favor of this industry specification.

tbd

The following member companies of the SFF Committee voted against this industry specification.

tbd

The following member companies of the SFF Committee chose to abstain on this industry specification.

tbd

## Foreword

The development work on this specification was done by the SFF Committee, an industry group. The membership of the committee since its formation in August 1990 has included a mix of companies which are leaders across the industry.

When 2 1/2" diameter disk drives were introduced, there was no commonality on external dimensions e.g. physical size, mounting locations, connector type, and connector location, between vendors.

The first use of these disk drives was in specific applications such as laptop portable computers and system integrators worked individually with vendors to develop the packaging. The result was wide diversity, and incompatibility.

The problems faced by integrators, device suppliers, and component suppliers led to the formation of the SFF Committee as an industry ad hoc group to address the marketing and engineering considerations of the emerging new technology.

During the development of the form factor definitions, other activities were suggested because participants in the SFF Committee faced more problems than the physical form factors of disk drives. In November 1992, the charter was expanded to address any issues of general interest and concern to the storage industry. The SFF Committee became a forum for resolving industry issues that are either not addressed by the standards process or need an immediate solution.

Those companies which have agreed to support a specification are identified in the first pages of each SFF Specification. Industry consensus is not an essential requirement to publish an SFF Specification because it is recognized that in an emerging product area, there is room for more than one approach. By making the documentation on competing proposals available, an integrator can examine the alternatives available and select the product that is felt to be most suitable.

SFF Committee meetings are held during T10 weeks (see www.t10.org), and Specific Subject Working Groups are held at the convenience of the participants. Material presented at SFF Committee meetings becomes public domain, and there are no restrictions on the open mailing of material presented at committee meetings.

Most of the specifications developed by the SFF Committee have either been incorporated into standards or adopted as standards by EIA (Electronic Industries Association), ANSI (American National Standards Institute) and IEC (International Electrotechnical Commission).

If you are interested in participating or wish to follow the activities of the SFF Committee, the signup for membership and/or documentation can be found at:

www.sffcommittee.com/ie/join.html

The complete list of SFF Specifications which have been completed or are currently being worked on by the SFF Committee can be found at:

ftp://ftp.seagate.com/sff/SFF-8000.TXT

If you wish to know more about the SFF Committee, the principles which guide the activities can be found at:

ftp://ftp.seagate.com/sff/SFF-8032.TXT

Suggestions for improvement of this specification will be welcome. They should be sent to the SFF Committee, 14426 Black Walnut Ct, Saratoga, CA 95070.

SFF Committee –

**QSFP+ Copper and Optical Modules**

SFF Committee

**QSFP+ Copper And Optical Modules**

# 1. Scope

In an effort to broaden the applications for storage devices, an ad hoc industry group of companies representing system integrators, peripheral suppliers, and component suppliers decided to address the issues involved.

The SFF Committee was formed in August, 1990 and the first working document was introduced in January, 1991.

## 1.1 Description of Clauses

Clause 1 contains the Scope and Purpose

Clause 2 contains Referenced and Related Standards and SFF Specifications

Clause 3 begins the specification

# 2. References

The SFF Committee activities support the requirements of the storage industry, and it is involved with several standards.

## 2.1 Industry Documents

The following interface standards and specifications are relevant to this Specification.

- INF-8438i QSFP (Quad SFP) Module

## 2.2 SFF Specifications

There are several projects active within the SFF Committee. The complete list of specifications which have been completed or are still being worked on are listed in the specification at ftp://ftp.seagate.com/sff/SFF-8000.TXT

## 2.3 Sources

Those who join the SFF Committee as an Observer or Member receive electronic copies of the minutes and SFF specifications (http://www.sffcommittee.com/ie/join.html).

Copies of ANSI standards may be purchased from the InterNational Committee for Information Technology Standards (http://tinyurl.com/c4psg).

Copies of SFF, ASC T10 (SCSI), T11 (Fibre Channel) and T13 (ATA/SATA) standards and standards still in development are available on the HPE version of CD_Access (http://tinyurl.com/85fts).

## 2.4 Conventions

The American convention of numbering is used i.e., a comma separates the thousands and higher multiples, and a period is used as the decimal point. This is equivalent to the ISO/IEC convention of a space and comma.

| American | French | ISO |
|---|---|---|
| 0.6 | 0,6 | 0.6 |
| 1,000 | 1 000 | 1 000 |
| 1,323,462.9 | 1 323 462,9 | 1 323 462.9 |

# 3 Introduction

This Specification covers the following items:

a) electrical interfaces (including pinouts for data control, status, configuration and test signals) and the electrical connector and recommended host PCB layout requirements.
b) management interfaces encompassing features from the current SFP MSA and includes specific multi-datarate and multi-protocol implementations.
c) optical interfaces (including the optical connector receptacle and mating fiber optic connector plug and recommended breakout cable assembly.) The optical specifications are left to the applicable standards for each protocol.
d) mechanical including package outline with latching detail and optical connector receptacle detail, electrical connector mechanical details for both the Module and host PCB halves, front panel cut-out recommended dimensions and a blocking key solution to prevent damage from XFP modules.
e) thermal requirements (case temperatures)
f) electromagnetic interference (EMI) recommendations(including necessary shielding features to seal the OEM chassis front panel output with and without the QSFP+ module installed in the cage.)
g) electrostatic discharge (ESD) requirements solely to the extent disclosed in the Specification where the sole purpose of such disclosure is to enable products to operate, connect or communicate as defined within the Specifications.

The overall package dimension shall conform to the indicated dimensions and tolerances and the mounting features shall be located such that the products are mechanically interchangeable with the cage and connector system. In addition, the overall dimensions and mounting requirements for the cage and connector system on a circuit board shall be configured such that the products are mechanically and electrically interchangeable and the overall dimensions and insertion requirements for the optical connector and corresponding fiber optic cable plug shall be such that the products are mechanically and optically interchangeable.

The electrical and optical specification shall be compatible with those enumerated in the ITU-T Recommendation G.957 (STM-1, STM-4 and STM-16), Telcordia Technologies GR-253-CORE (OC-3, OC-12, OC-48 and OC-192), Ethernet IEEE 802.3 (Gigabit, 10Gigabit and 40Gigabit Ethernet), Infiniband Architecture Specifications (SDR, DDR and QDR), SFF-8431, or Fibre Channel-PI-3/4 (2GFC, 4GFC, 8GFC) and 10GFC. Electrical and optical specifications may be compatible with standards under development.
.

The Specifications will provide a common solution for combined four-channel ports that support SONET/SDH and/or Ethernet and/or Infiniband and/or Fibre Channel specifications. This specification encompasses design(s) capable of supporting multimode, single mode Modules, passive copper, active copper and active optical cables.

**Table 1 Multimode Fiber Applications**

| | Fiber Type | IEE 802.3 | | | Fibre Channel-FC-PI-2/3/4 | | | | Infiniband | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Distance | Core Diameter MHZ*km | 1GE | 10GE | 40GE | 2GFC | 4GFC | 8GFC | 10GFC | SDR | DDR | QDR |
| 275m | 62.5/200 | X | | | | | | | | | |
| 220m | 62.5/160 | X | | | | | | | | | |
| 26m | 62.5/160 | | X | | | | | | | | |
| 33m | 62.5/200 | | X | | | | | | | | |
| 150m | 62.5/200 | | | | X | | | | | | |
| 75m | 62.5/200 | | | | | | | | X | | |
| 70m | 62.5/200 | | | | | X | | | | | |
| 50m | 62.5/200 | | | | | | | | | X | |
| 21m | 62.5/200 | | | | | | X | | | | |
| 550m | 50/500 | X | | | | | | | | | |

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 500m | 50/400 | X | | | | | | | | | |
| 66m | 50/400 | | X | | | | | | | | |
| 82m | 50/500 | | X | | | | | | | | |
| 2000m | 50/2000 | | X | | | | | | | | |
| 300m | 50/500 | | | | X | | | | | | |
| 150m | 50/500 | | | | | X | | | | | |
| 125m | 50/500 | | | | | | | | X | | |
| 75m | 50/500 | | | | | | | | | X | |
| 50m | 50/500 | | | | | | X | | | | |
| 200m | 50/2000 | | | | X | | | | X | | |
| 380m | 50/2000 | | | | | X | | | | | |
| 150m | 50/2000 | | | | | | X | | | X | |

**Table 2 Singlemode Fiber Applications**

| | | IEEE 802.3 | | | Fibre Channel FC-PI-2/3/4 | | | | Infiniband | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Distance | Fiber type | 1 GE | 10 GE | 40 GE | 2GFC | 4GFC | 8GFC | 10GFC | SDR | DDR | QDR |
| 1.4km | SM | | | | | | X | | | | |
| 2km | SM | | | | | | | | | | |
| 4km | | | | | | X | | | | | |
| 10km | SM | X | X | | X | X | X | | X | X | X |
| 30km | SM | | X | | | | | | | | |
| 40km | SM | | X | | | | | | | | |

An application reference Model, See Figure 1, shows the high-speed data interface between an ASIC (SerDes) and the QSFP+ module. Only one data channel of the interface is shown for simplicity.

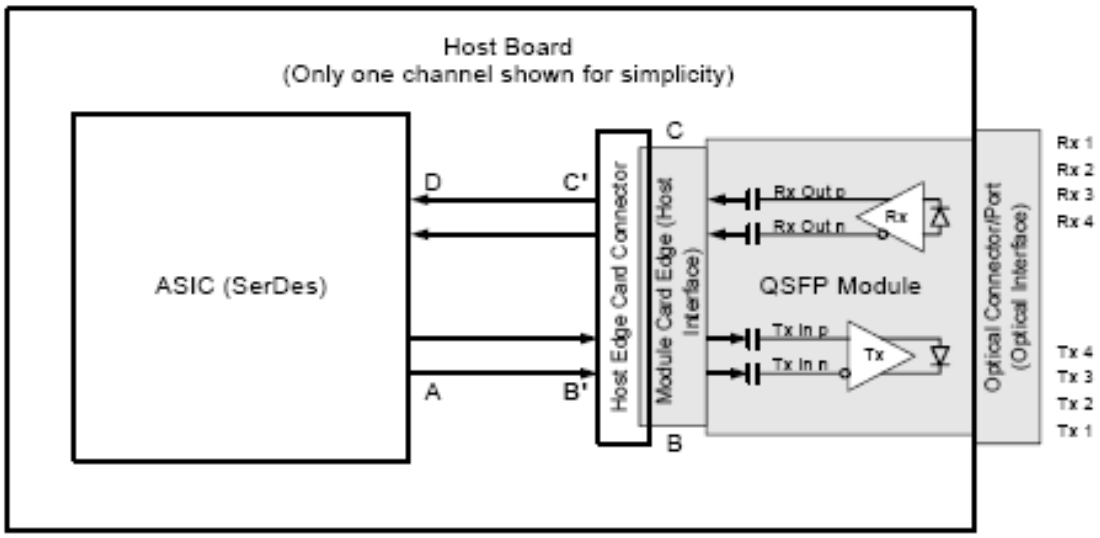



**Figure 1 – Application Reference Model**

QSFP+ compliance and reference points are as follows:

A: Host ASIC transmitter output at ASIC package pin on a DUT board – Reference point

B: Host ASIC transmitter output across the Host Board and Host Edge Card connector at the Module Card Edge interface – Reference point

B’: Host ASIC transmitter output across the Host Board at Host Edge Card Connector – Compliance point

C: QSFP+ receiver output at the Module Card Edge interface – Reference point

C': QSFP+ receiver output at Host Edge Card Connector – Compliance point

D: QSFP+ receiver output at Host ASIC package receiver input pin on a DUT board – Reference point

## 4 Electrical Specification

This clause contains pin definition data for the QSFP+ Module. The pin definition data is generic for gigabit -per-second datacom applications such as Fibre Channel and Gigabit Ethernet and SONET/ATM applications. Compliance Points for high-speed signal electrical measurements are defined in Figure 1. Compliance Points for all other electrical signals are at comparable points at the host edge card connector.

### 4.1 Electrical Connector

Figure 2 shows the signal symbols and contact numbering for the QSFP+ module edge connector. The diagram shows the module PCB edge as a top and bottom view. There are 38 contacts intended for high speed, low speed signals, power and ground connections. Table 3 provides more information about each of the 38 contacts.

For EMI protection the signals to the connector should be shut off when the QSFP+ Module is removed. Standard board layout practices such as connections to Vcc and GND with Vias, use of short and equal-length differential signal lines, use of microstrip-lines and 50 Ohm terminations are recommended. The chassis ground (case common) of the QSFP+ module is isolated from the module's circuit ground, GND, to provide the equipment designer flexibility regarding connections between external electromagnetic interference shields and circuit ground, GND, of the module

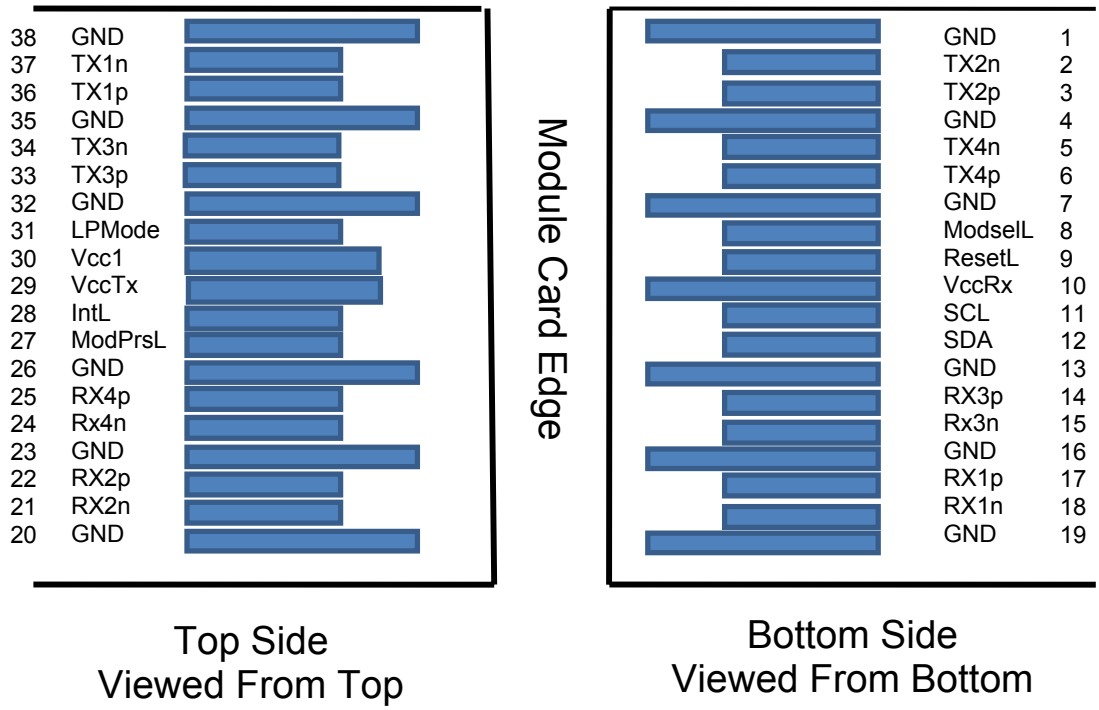



**Figure 2 QSFP+ Module Pad Layout**

**Table 3 Pin Function Definition**
**(See Figure 9 for pad dimensions)**

| Pin | Logic | Symbol | Description | Plug Sequence | Notes |
|---|---|---|---|---|---|
| 1 | | GND | Ground | 1 | 1 |
| 2 | CML-I | Tx2n | Transmitter Inverted Data Input | 3 | |
| 3 | CML-I | Tx2p | Transmitter Non-Inverted Data Input | 3 | |
| 4 | | GND | Ground | 1 | 1 |
| 5 | CML-I | Tx4n | Transmitter Inverted Data Input | 3 | |
| 6 | CML-I | Tx4p | Transmitter Non-Inverted Data Input | 3 | |
| 7 | | GND | Ground | 1 | 1 |
| 8 | LVTTL-I | ModSelL | Module Select | 3 | |
| 9 | LVTTL-I | ResetL | Module Reset | 3 | |
| 10 | | Vcc Rx | +3.3V Power Supply Receiver | 2 | 2 |
| 11 | LVCMOS-I/O | SCL | 2-wire serial interface clock | 3 | |
| 12 | LVCMOS-I/O | SDA | 2-wire serial interface data | 3 | |
| 13 | | GND | Ground | 1 | 1 |
| 14 | CML-O | Rx3p | Receiver Non-Inverted Data Output | 3 | |
| 15 | CML-O | Rx3n | Receiver Inverted Data Output | 3 | |
| 16 | | GND | Ground | 1 | 1 |
| 17 | CML-O | Rx1p | Receiver Non-Inverted Data Output | 3 | |
| 18 | CML-O | Rx1n | Receiver Inverted Data Output | 3 | |
| 19 | | GND | Ground | 1 | 1 |
| 20 | | GND | Ground | 1 | 1 |
| 21 | CML-O | Rx2n | Receiver Inverted Data Output | 3 | |
| 22 | CML-O | Rx2p | Receiver Non-Inverted Data Output | 3 | |
| 23 | | GND | Ground | 1 | 1 |
| 24 | CML-O | Rx4n | Receiver Inverted Data Output | 3 | |
| 25 | CML-O | Rx4p | Receiver Non-Inverted Data Output | 3 | |
| 26 | | GND | Ground | 1 | 1 |
| 27 | LVTTL-O | ModPrsL | Module Present | 3 | |
| 28 | LVTTL-O | IntL | Interrupt | 3 | |
| 29 | | Vcc Tx | +3.3V Power supply transmitter | 2 | 2 |
| 30 | | Vcc1 | +3.3V Power supply | 2 | 2 |
| 31 | LVTTL-I | LPMode | Low Power Mode | 3 | |
| 32 | | GND | Ground | 1 | 1 |
| 33 | CML-I | Tx3p | Transmitter Non-Inverted Data Input | 3 | |
| 34 | CML-I | Tx3n | Transmitter Inverted Data Input | 3 | |
| 35 | | GND | Ground | 1 | 1 |
| 36 | CML-I | Tx1p | Transmitter Non-Inverted Data Input | 3 | |
| 37 | CML-I | Tx1n | Transmitter Inverted Data Input | 3 | |
| 38 | | GND | Ground | 1 | 1 |

Note 1: GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table 6. Recommended host board power supply filtering is shown in Figure 4. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP+ Module module in any combination. The connector pins are each rated for a maximum current of 500 mA.

Figure 3 shows an example of a complete QSFP+ host PCB schematic with connections to SerDes and control ICs.

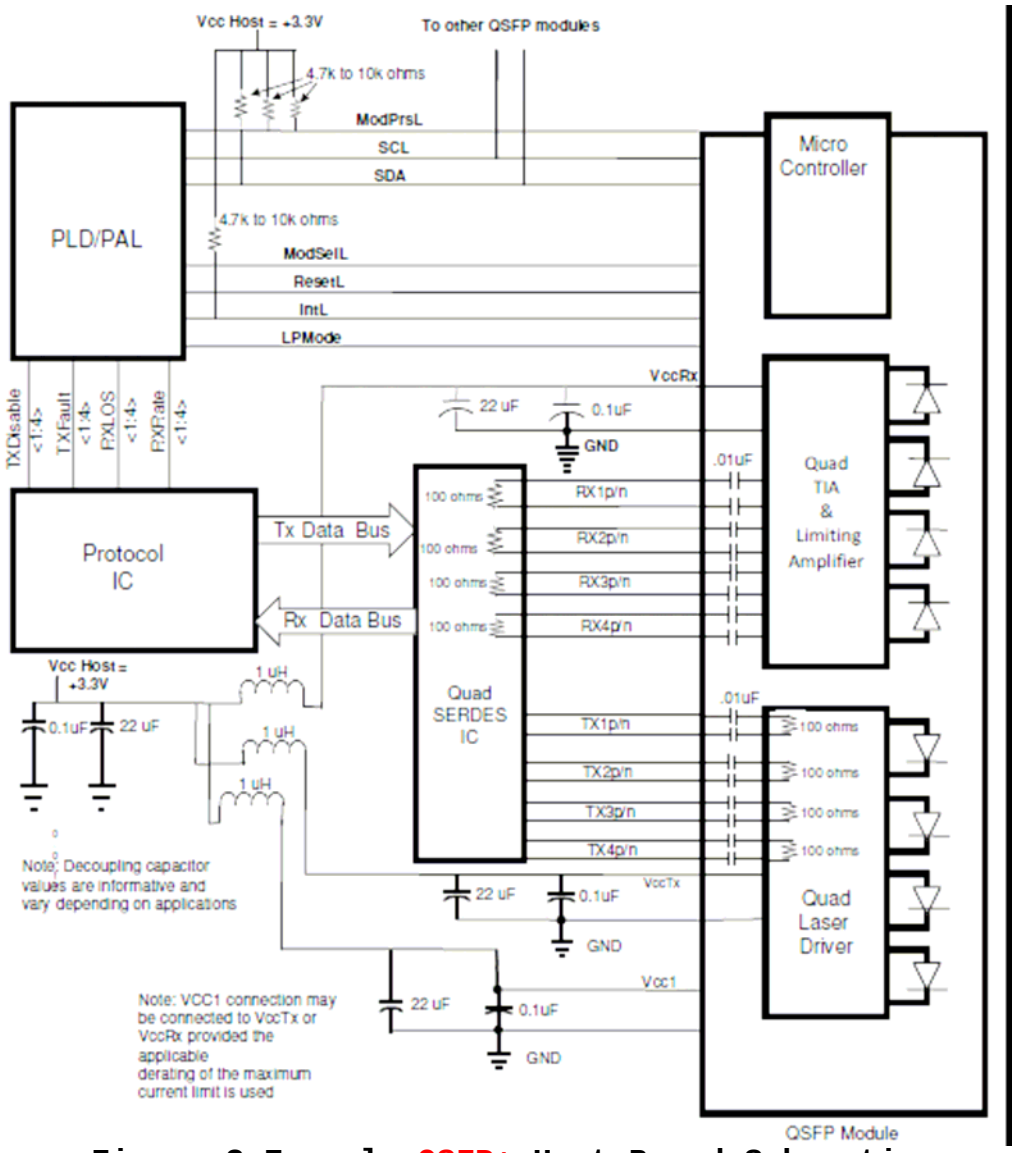



**Figure 3 Example QSFP+ Host Board Schematic**

### 4.1.1 Low Speed Electrical Hardware Pins

In addition to the 2-wire serial interface the module has the following low speed pins for control and status:

- ModSelL
- ResetL
- LPMode
- ModPrsL
- IntL

#### 4.1.1.1 ModSelL

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP+ modules on a single 2-wire interface bus. When the ModSelL is “High”, the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node must be biased to the “High” state in the module.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP+ modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before

communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

#### 4.1.1.2 ResetL

The ResetL pin must be pulled to Vcc in the QSFP+ module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module inidicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

#### 4.1.1.3 LPMode

The LPMode pin shall be pulled up to Vcc in the QSFP+ module. This function is affected by the LPMode pin and the combination of the Power_over-ride and Power_set software control bits (Address A0h, byte 93 bits 0,1).

The module has two modes a low power mode and a high power mode. The high power mode operates in one of the four power classes.

When the module is in a low power mode it has a maximum power consumption of 1.5W. This protects hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

The modules 2-wire serial interface and all laser safety functions must be fully operational in this low power mode. The module shall still support the completion of reset interrupt in this low power mode.

If the Extended Identifier bits (Page 00h, byte 129 bits 6-7) indicate a power consumption greater than 1.5W and the module is in low power mode it must reduce its power consumption to less than 1.5W while still maintaining the functionality above. The exact method of accomplishing low power is not specified, however it is likely that either the Tx or Rx or both will not be operational in this state.

If the Extended Identifier bits (Page 00h, byte 129 bits 6-7) indicate that its power consumption is less than 1.5W then the module shall be fully functional independent of whether it is in low power or high power mode.

The Module should be in low power mode if the LPMode pin is in the high state, or if the Power_ over-ride bit is in the high state and the Power_set bit is also high. The module should be in high power mode if the LPMode pin is in the low state, or the Power_over-ride bit is high and the Power_set bit is low. Note that the default state for the Power_over-ride bit is low.

A truth table for the relevant configurations of the LPMode and the Power_over-ride and Power_set are shown in Table 4.

**Table 4 Power Mode Truth Table**

| LPMode | Power_Overide Bit | Power_set Bit | Module Power Allowed |
|---|---|---|---|
| 1 | 0 | X | Low Power |
| 0 | 0 | X | High Power |
| X | 1 | 1 | Low Power |
| X | 1 | 0 | High Power |

At Power up, the Power_over-ride and Power_set bits shall be set to 0.

#### 4.1.1.4 ModPrsL

ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted “Low” when inserted and deasserted “High” when the module is physically absent from the host connector.

#### 4.1.1.5 IntL

IntL is an output pin. When “Low”, it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface.The IntL pin is an open collector output and must be pulled to host supply voltage on the host board.

### 4.1.2 Low Speed Electrical Specification

Low speed signaling other than SCL and SDA is based on Low Voltage TTL (LVTTL) operating at Vcc. Vcc refers to the generic supply voltages of VccTx, VccRx, Vcc_host or Vcc1. Hosts shall use a pull-up resistor connected to Vcc_host on each of the 2-wire interface SCL (clock), SDA (data), and all low speed status outputs.The SCL and SDA is a hot plug interface that may support a bus topology. During module insertion or removal, the module may implement a pre-charge circuit which prevents corrupting data transfers from other modules that are already using the bus.

- Note 1-Timing diagrams for SCL and SDA are included in Clause 6.2.2.

The QSFP+ low speed electrical specifications are given in Table 5. This specification ensures compatibility between host bus masters and the 2-wire interface.

**Table 5 - Low Speed Control and Sense Signals**

| Parameter | Symbol | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| SCL and SDA | VOL | 0 | 0.4 | V | IOL(max)=3.0mA |
| | VOH | Vcc-0.5 | Vcc+0.3 | V | |
| SCL and SDA | VIL | -0.3 | Vcc*0.3 | V | |
| | VIH | VCC*0.7 | Vcc + 0.5 | V | |
| Capacitance for SCL and SDA I/O pin | Ci | | 14 | pF | |
| Total bus capacitive load for SCL and SDA | Cb | | 100 | pF | 3.0 k Ohms Pullup resistor, max |

| | | | | | |
|---|---|---|---|---|---|
| | | | 200 | pF | 1.6 k Ohms pullup resistor max |
| LPMode, Reset and Mode SelL | VIL | -0.3 | 0.8 | V | \|lin\|</=125 uA for OV<Vin,Vcc |
| | VIH | 2 | VCC+0.3 | V | |
| ModPrsL and IntL | VOL | 0 | 0.4 | V | IOL=2.0mA |
| | VOH | VCC-0.5 | VCC+0.3 | V | |

### 4.1.3 High Speed Electrical Specification

#### 4.1.3.1 Rx(n)(p/n)

Rx(n)(p/n) are QSFP+ module receiver data outputs. Rx(n)(p/n) are AC-coupled 100 Ohm differential lines that should be terminated with 100 Ohm differentially at the Host ASIC(SerDes). The AC coupling is inside the QSFP+ module and not required on the Host board. For operation at 6Gbps and below, when properly terminated, the single-ended voltage swing will be between 170 mV to 800 mV and the differential voltage swing (absolute value) will be between 340 mVpp to 1600 mVpp. For operation above 6Gbps see the appropriate specification for required voltage swings. Note: for 10G Ethernet reference SFF-8431.

Due to the possibility of insertion of classic QSFP+ modules into a host designed for QSFP+ the damage threshold of the host input signal shall be at least 1600 mV peak to peak differential.

Output squelch for loss of optical input signal, hereafter Rx Squelch, is required and shall function as follows. In the event of the optical signal on any channel becoming equal to or less than the level required to assert LOS, then the receiver data output for that channel shall be squelched or disabled. In the squelched or disabled state output impedance levels are maintained while the differential voltage swing shall be less than 50 mVpp.

In normal operation the default case has Rx Squelch active. Rx Squelch can be deactivated using Rx Squelch Disable through the 2-wire serial interface. Rx Squelch Disable is an optional function. For specific details refer to Clause 6.6.5.2.

#### 4.1.3.2 Tx(n)(p/n)

Tx(n)(p/n) are QSFP+ module transmitter data inputs. They are AC-coupled 100 Ohm differential lines with 100 Ohm differential terminations inside the QSFP+ module. The AC coupling is inside the QSFP+ module and not required on the Host board. For operation at 6Gbps and below the inputs will accept single-ended voltage swings between 250 mV to 800 mV and differential voltage swings between 500 mVpp to 1600 mVpp (absolute value). For best EMI results, single-ended swings between 250 mV and 600 mV and differential voltage swings between 500 mVpp to 1200 mVpp (absolute value) are recommended. For operation above 6Gbps see the appropriate specification for required voltage swings. Note: for 10G Ethernet reference SFF-8431. For 40G Ethernet operation reference 802.3ba.

Due to the possibility of insertion of QSFP+ modules into a host designed for classic QSFP+ the damage threshold of the module input signal shall be at least 1600 mV peak to peak differential.

Output squelch, hereafter Tx Squelch, for loss of input signal, hereafter Tx LOS, is an optional function. Where implemented it shall function as follows. In the event of the differential, peak-to-peak electrical signal on any channel becomes equal to or less than 50 mVpp, then the transmitter optical output for that channel shall be squelched or disabled and the associated TxLOS flag set.

Where squelched, the transmitter OMA shall be less than or equal to -26 dBm and when disabled the transmitter power shall be less than or equal to -30 dBm. For applications, e.g. Ethernet, where the transmitter off condition is defined in terms of average power, disabling the transmitter is recommended and for applications, e.g. InfiniBand, where the transmitter off condition is defined in terms of OMA, squelching the transmitter is recommended.

In module operation, where Tx Squelch is implemented, the default case has Tx Squelch active. Tx Squelch can be deactivated using Tx Squelch Disable through the 2-wire serial interface. Tx Squelch Disable is an optional function. For specific details refer to Clause 7.6.5.2.

### *4.2 Power Requirements*

The power supply has three designated pins, Vcc Tx, Vcc1, and Vcc Rx, in the connector. Vcc1 is used to supplement Vcc Tx or Vcc Rx at the discretion of the module vendor. Power is applied concurrently to these pins.

Since different classes of modules exist with pre-defined maximum power consumption limits, it is necessary to avoid exceeding the system power supply limits and cooling capacity when a module is inserted into a system designed to only accommodate lower power modules. It is recommended that the host, through the management interface, identify the power consumption class of the module before allowing the module to go into high power mode.

A host board together with the QSFP+ module(s) forms an integrated power system. The host supplies stable power to the module. The module limits electrical noise coupled back into the host system and limits inrush charge/current during hot plug insertion.

All specifications shall be met at the maximum power supply current. No power sequencing of the power supply is required of the host system since the module sequences the contacts in the order of ground, supply and signals during insertion.

#### 4.2.1 Host Board Power Supply Filtering

The host board should use the power supply filtering shown in Figure 4.

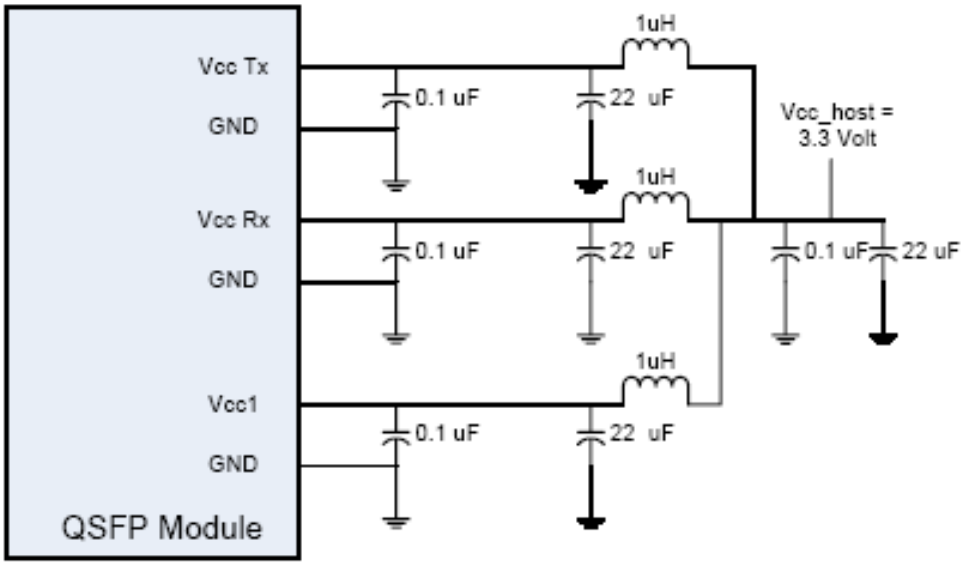



**Figure 4 Recommended Host Board Power Supply Filtering**

Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. Inductors with DC Resistance of less than 0.1 Ohm should be used in order to maintain the required voltage at the Host Edge Card Connector.

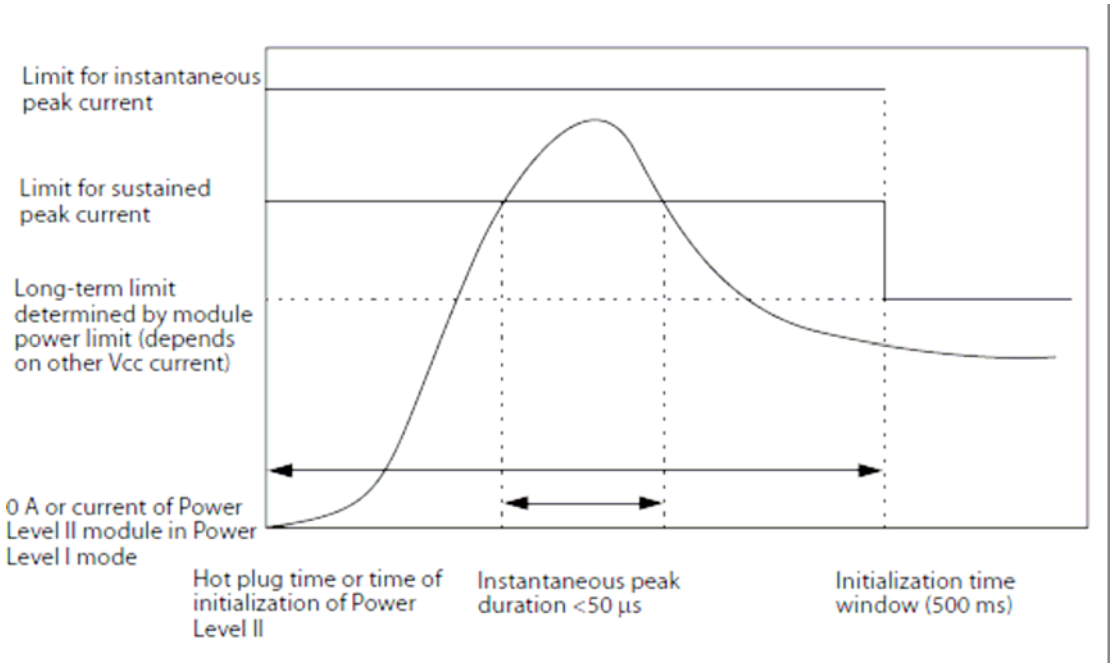
The specification for the power supply is shown in Table 6.

**Table 6 - Power Supply Specification**

| Parameter | MIN | Nominal | Max | Unit | Condition |
|---|---|---|---|---|---|
| Vcc | | 3.3 | | V | Measured at Vcc 1x, Vcc Rx and Vcc1. |
| Vcc set point accuracy | -5 | | 5 | % | Measured at Vcc Tx, Vcc Rx and Vcc1. |
| Power Supply | | | 50 | mV | 1kHz to frequency of |

| | | | | | |
|---|---|---|---|---|---|
| Noise including ripple | | | | | operation measured at Vcc host. |
| Sustained peak current at hot plug with LPMode Pin asserted | | | 495 | mA | |
| Module Maximum Current Inrush with LPMode Pin asserted | | | 600 | mA | |
| Module sustained peak current with LPMode Pin deasserted | | | 750 | mA | |
| Module Maximum Current Inrush with LPMode Pin deasserted | | | 900 | mA | |
| Module Current Ramp Rate | | | 100 | mA/uS | |

These limits separately apply to the current that flows throught each inductor in the power supply filter.




Power levels associated with classifications of modules are shown in Table 7.

**Table 7 - Power Budget Classification**

| Power Level | Max Power (W) |
|---|---|
| 1 | 1.5 |
| 2 | 2 |
| 3 | 2.5 |
| 4 | 3.5 |

In general, the higher power classification level is associated with higher data rates and longer reach. The system designer is responsible for ensuring that the maximum temperature does not exceed the case temperature requirements.

### 4.3 ESD

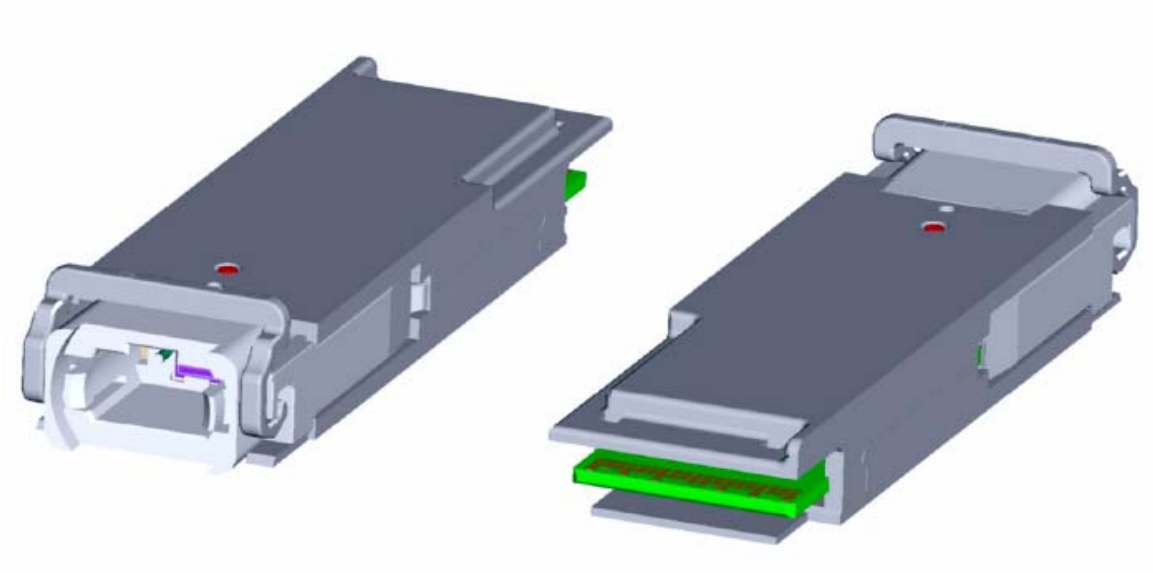
The module shall meet ESD requirements given in EN61000-4-2, criterion B test specification such that when installed in a properly grounded cage and chassis the units are subjected to 15KV air discharges during operation and 8KV direct contact discharges to the case.

The QSFP+ module and host SFI contacts (High Speed Contacts) shall withstand 1000 V electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B.
The QSFP+ module and all host contacts with exception of the SFI contacts (High Speed Contacts) shall withstand 2 kV electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B.
The QSFP+ module shall meet ESD requirements given in EN61000-4-2, criterion B test specification such that units are subjected to 15 kV air discharges during operation and 8 kV direct contact discharges to the case.

## 5 Mechanical and Board Definition

### 5.1 Introduction

The overall Module module defined in this clause is illustrated in Figure 5. All Pluggable mdules and direct attach cable plugs must mate to the connector and cage design defined in this specification. Several cage to bezel options are defined. Both metal spring finger and elastomeric EMI solutions are permitted but must pass customer defined requirements. Heat sink/clip thermal designs are application specific and not specifically defined by this specification, however a general design is given as an example.



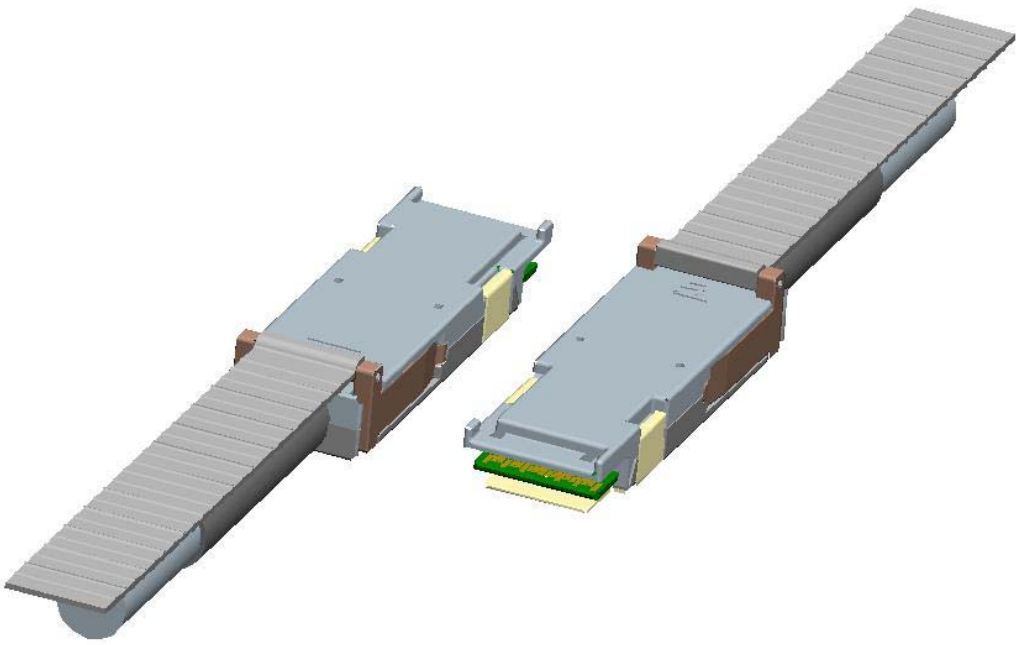


**Figure 5 – QSFP+ pluggable and direct attach module rendering**

## 5.2 QSFP+ Datums and Component Alignment

A listing of the datums for the various components is contained in Table 8. The alignments of some of the datums are noted. The relationship of the Module, Cage, and Connector relative to the Host Board and Bezel is illustrated in Figure 6 by the location of the key datums of each of the components. In order to reduce the complexity of the drawings, all dimensions are considered centered unless otherwise specified.

**Table 8 – Definition of Datums**

| Datum | Description |
|---|---|
| A | Host Board Top Surface |
| B | Centerline of bezel |
| C | **Distance between Connector terminal thru holes on host board |
| D | *Hard stop on Module |
| E | **Width of Module |
| F | Height of Module housing |
| G | **Width of Module pc board |
| H | Leading edge of signal contact pads on Module pc board |
| J | Top surface of Module pc board |
| K | *Host board thru hole #1 to accept connector guide post |
| L | *Host board thru hole #2 to accept connector guide post |
| M | **Width of bezel cut out |
| N | *Connector alignment pin |
| P | **Width of inside of cage at EMI gasket (when fully compressed) |
| R | Height of inside of cage at EMI gasket (when fully compressed) |
| S | Seating plane of cage on host board |
| T | *Hard stop on cage |
| V | Length of heat sink clip |
| W | Seating surface of the heat sink on the cage |
| X & Y | Host board horizontal and depth datums established by customer's fiducials |
| Z | **Width of heat sink surface that fits into clip |
| AA | **Connector slot width |
| BB | Seating plane of cage on host board |
| CC | Length of boss on heat sink that fits inside of the cage |
| *Datums D, K, L, N and T are aligned when assembled (see figure 6)<br>**Centerlines of datums AA, C, E, G, M, P and Z are aligned on the same vertical axis | |

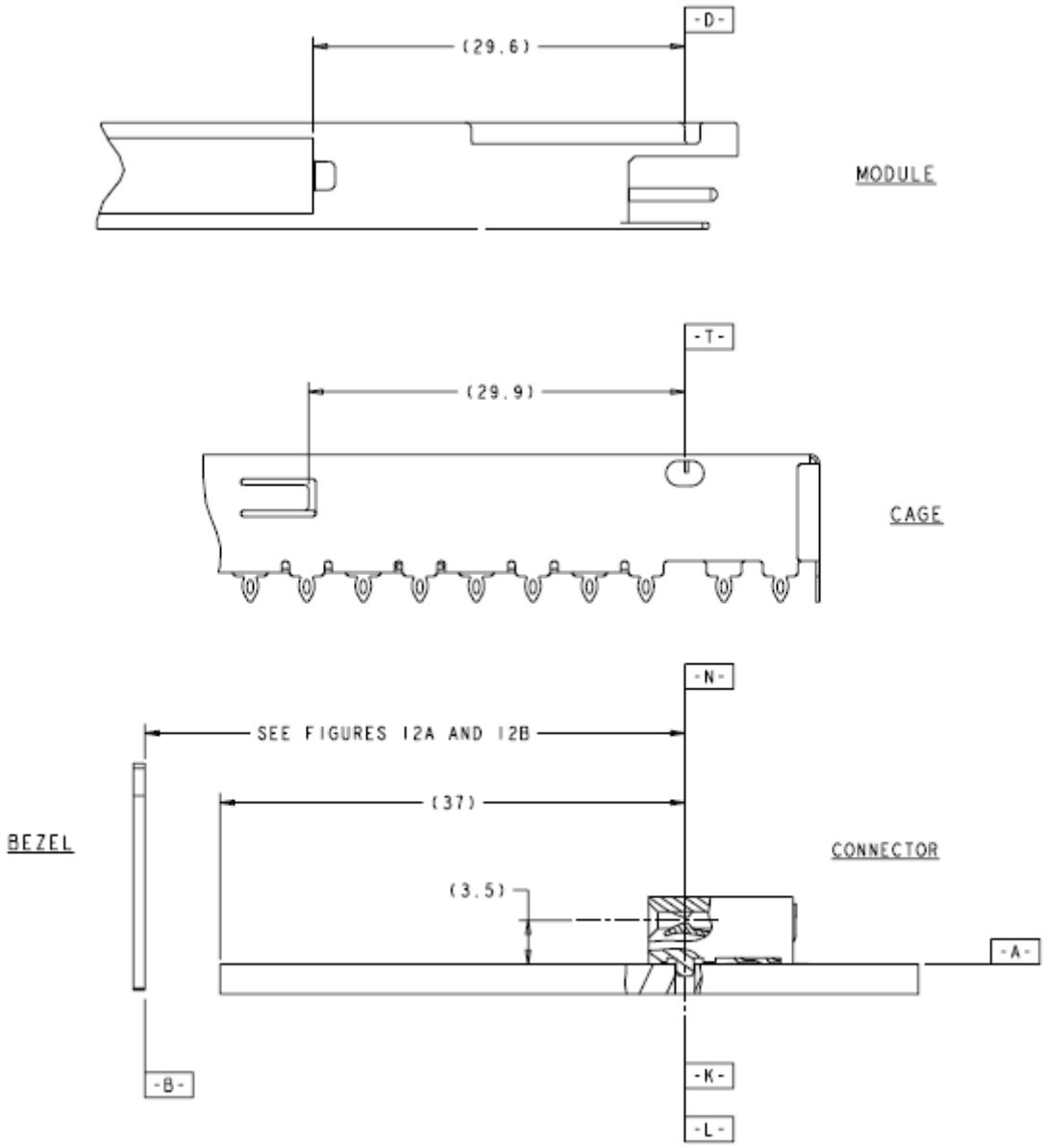



**Figure 6 – QSFP+ Datum Alignment, Depth**

### 5.3 QSFP+ Module Mechanical Package Dimensions

A common mechanical outline is used for all QSFP+ Modules and direct attach cables. The preferred method of removing the module from the cage assembly is by a bail type actuation method. The module shall provide a means to self-lock with the cage upon insertion. The package dimensions for the QSFP+ module are defined in Figure 7 and Figure 8. The dimensions that control the size of the module that extends outside of the cage are listed as maximum dimensions per Note 1 and Note 6 in Figure 7.

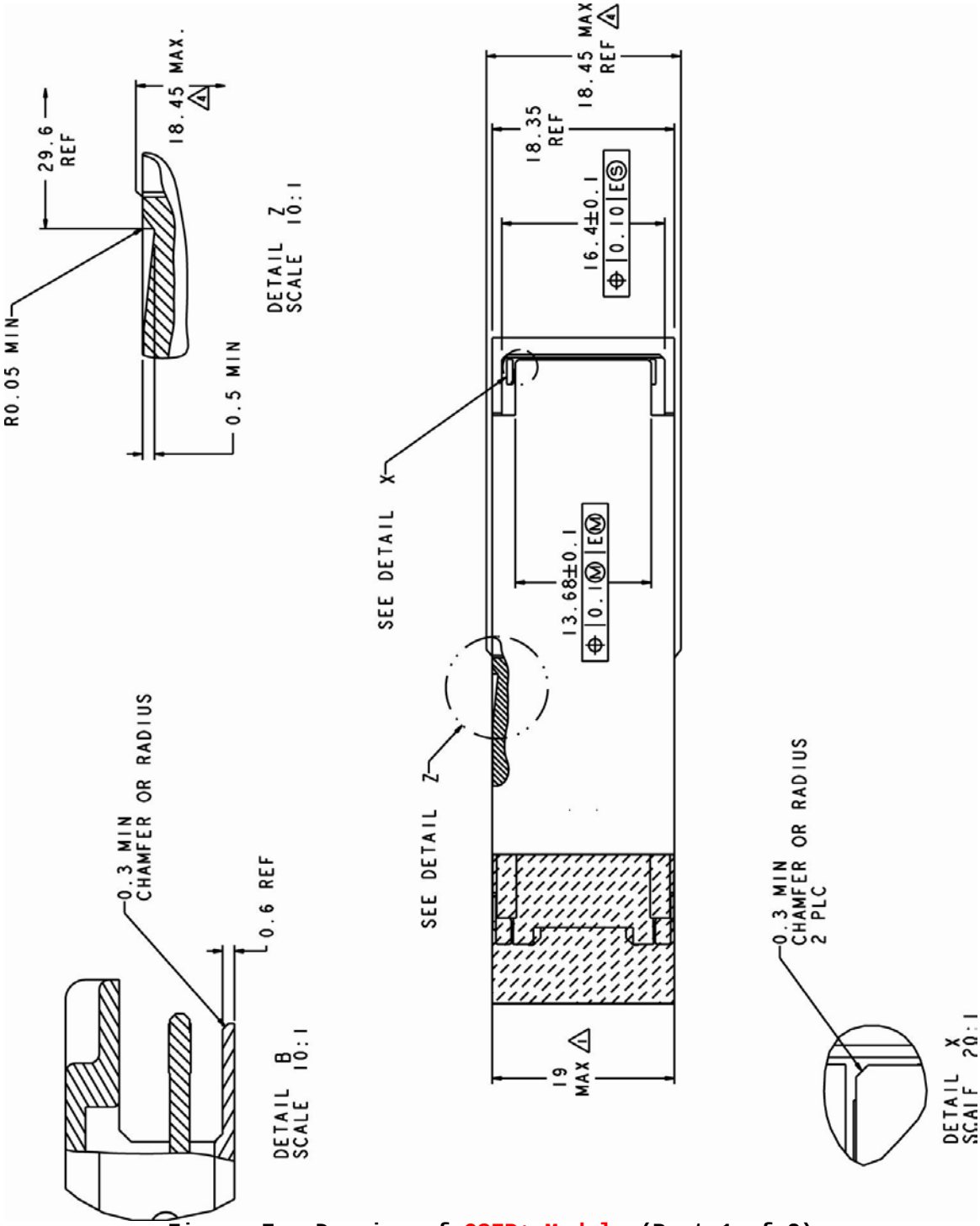



**Figure 7 – Drawing of QSFP+ Module (Part 1 of 2)**

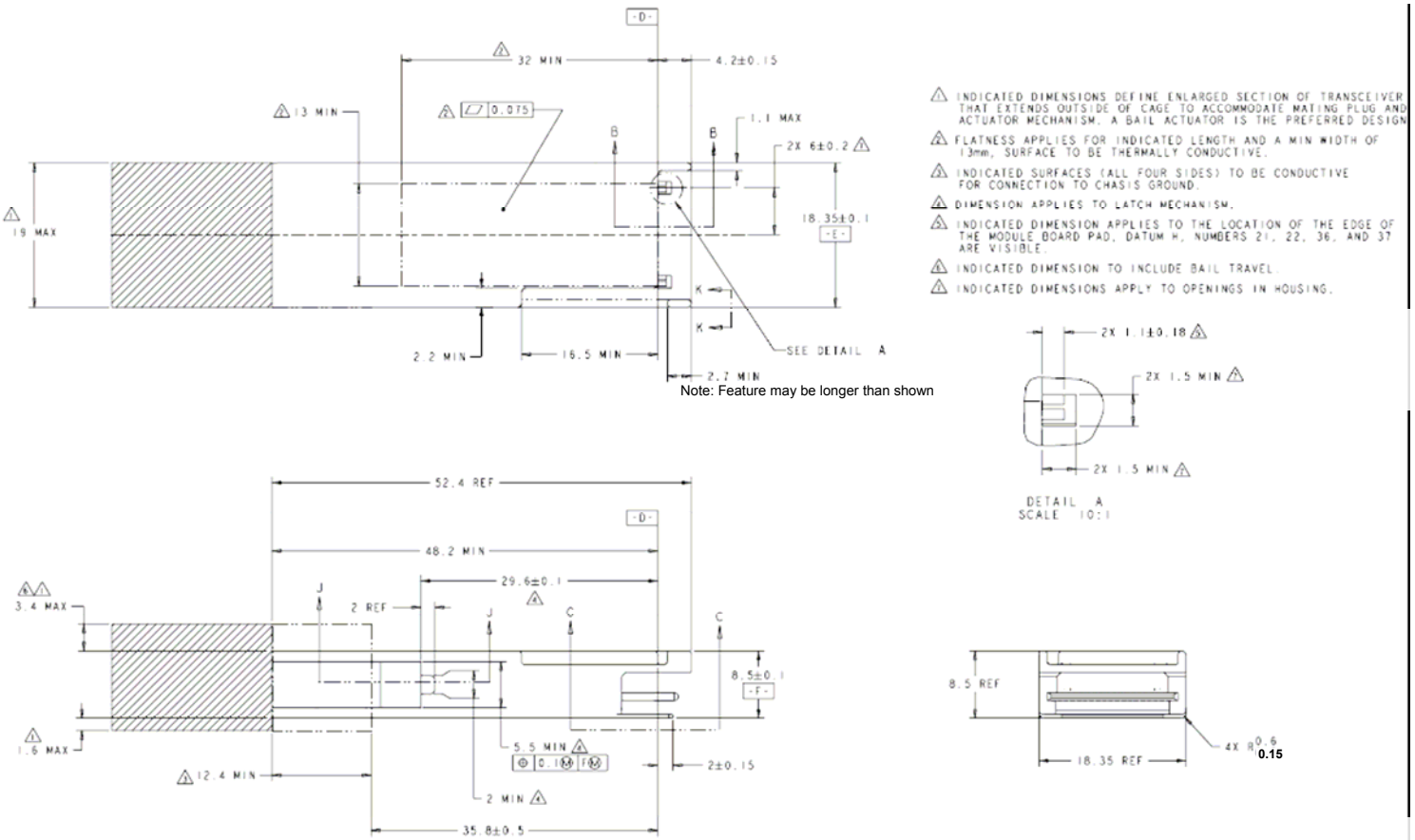



**Figure 7 – Drawing of QSFP+ Module (Part 2 of 2)**

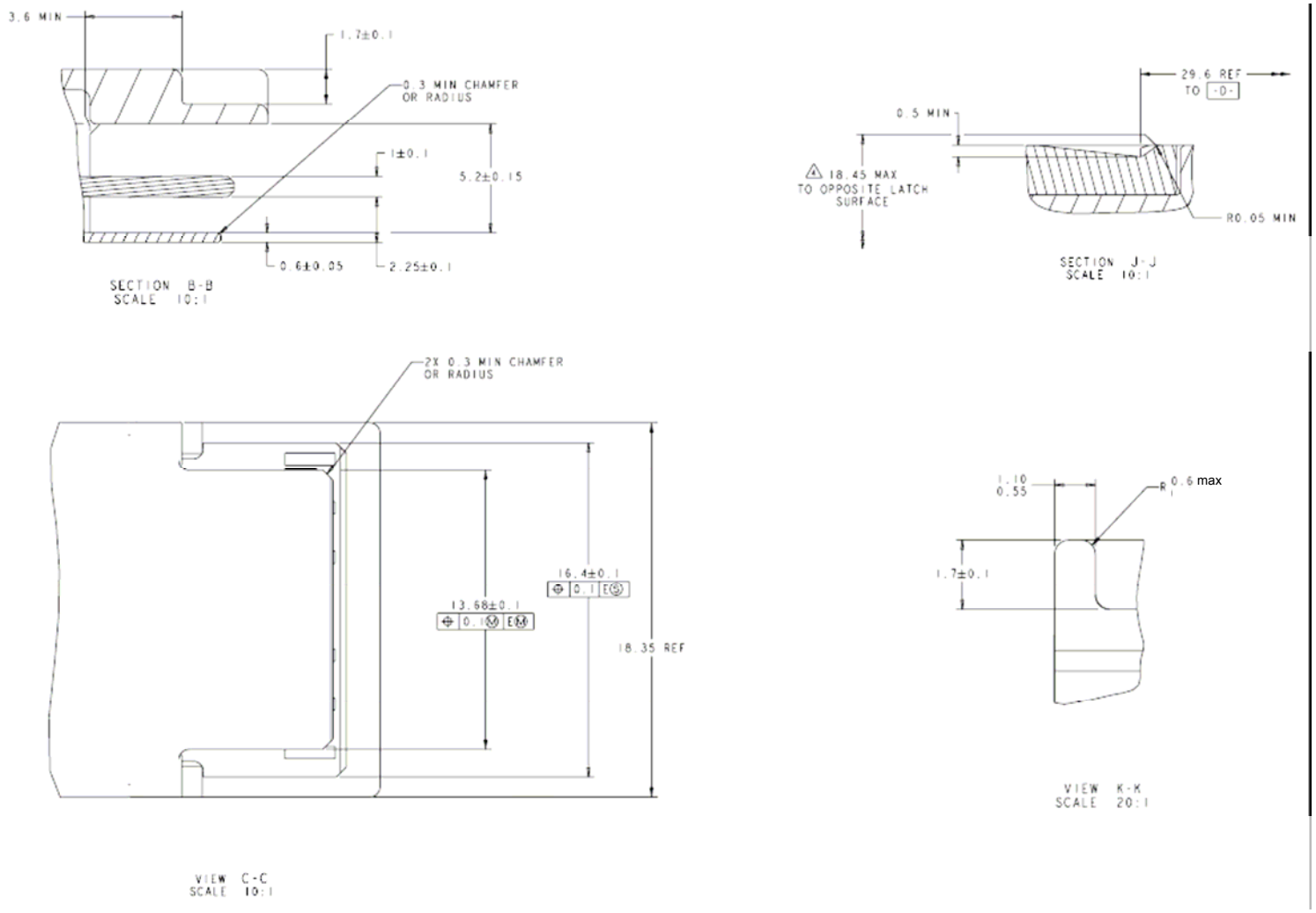



**Figure 8 –QSFP+ Module Tab drawings**

### 5.3.1 Mating of QSFP+ Module PCB to QSFP+ Electrical Connector

The QSFP+ Module contains a printed circuit board that mates with the QSFP+ electrical connector. The pads are designed for a sequenced mating:
First mate – ground contacts
Second mate – power contacts
Third mate – signal contacts
The pattern layout for the QSFP+ Printed Circuit Board is shown in Figure 9.

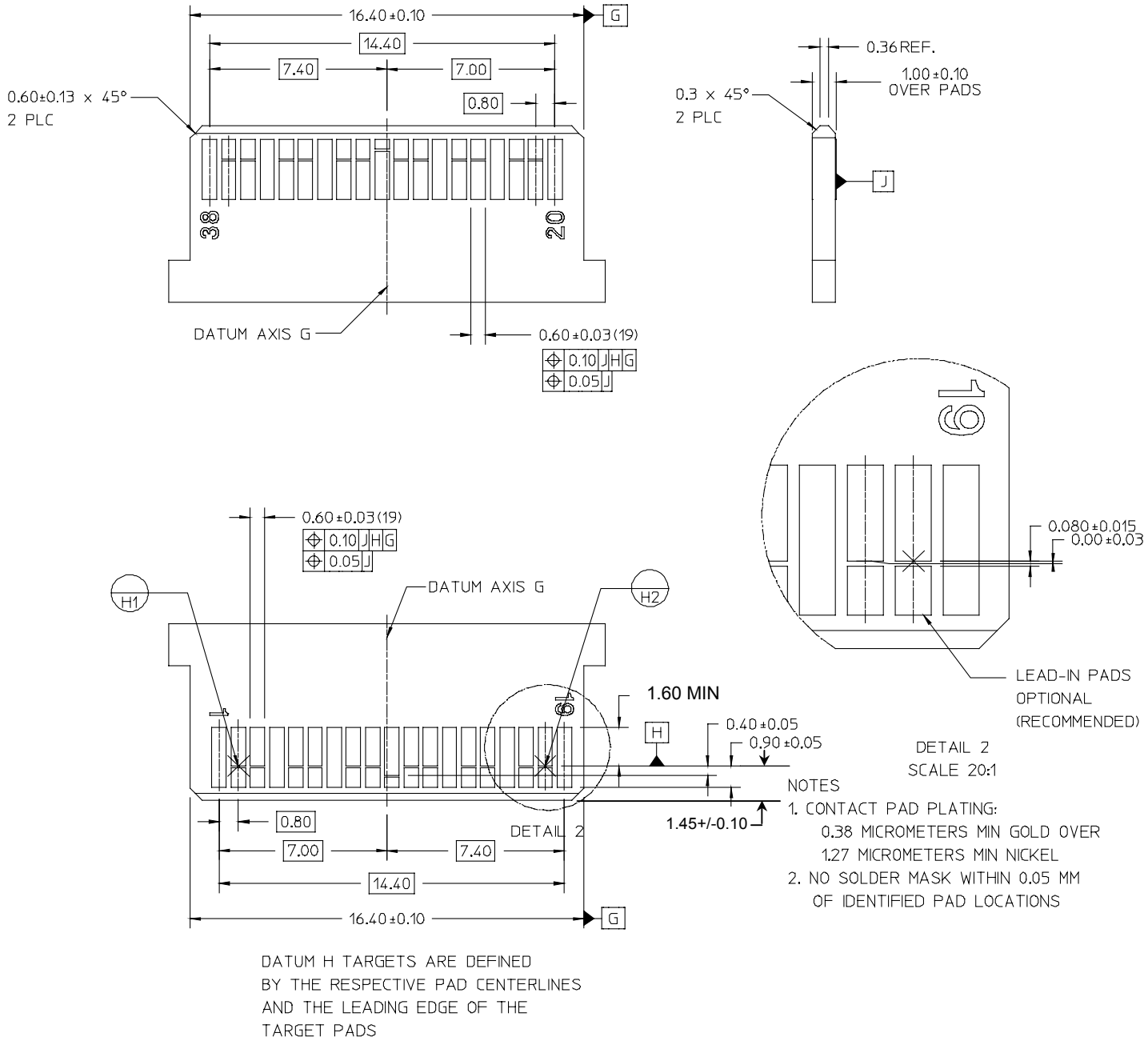
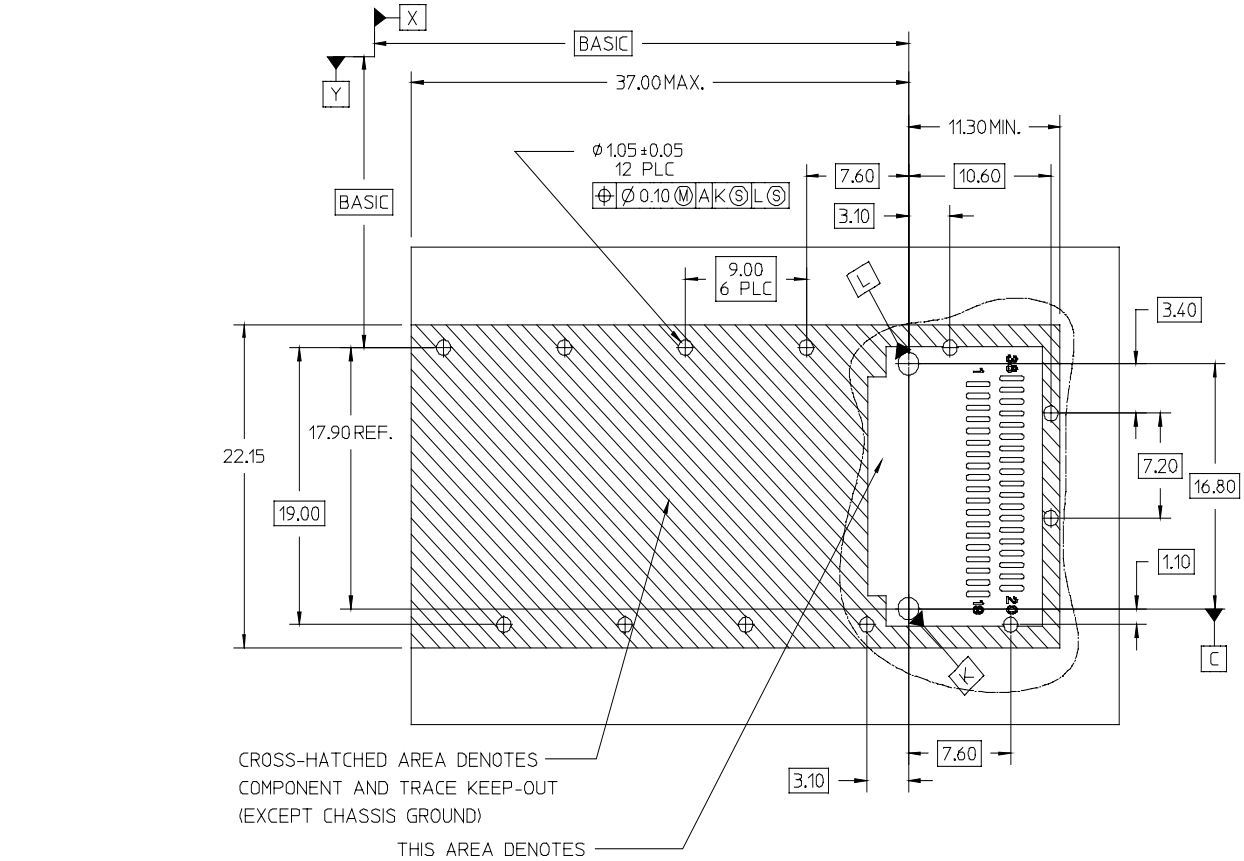



**Figure 9 – Pattern Layout for QSFP+ Printed Circuit Board**

### 5.4 Host PCB Layout

A typical host board mechanical layout for attaching the QSFP+ Connector and Cage System is shown in Figure 10 and Figure 11. Location of the pattern on the host board is application specific. See Clause 5.6 for details on the location of the pattern relative to the bezel. To achieve 10Gbps performance careful attention must be paid to pad dimensions and host board layout.




NOTES
1. DATUM X & Y ARE ESTABLISHED BY THE CUSTOMER"S FIDUCIAL
2. DATUM A IS THE TOP SURFACE OF THE HOST BOARD
3. LOCATION OF THE EDGE OF PCB IS APPLICATION SPECIFIC
4. FINISHED HOLE SIZE

**Figure 10 – QSFP+ Host PCB Mechanical Layout**

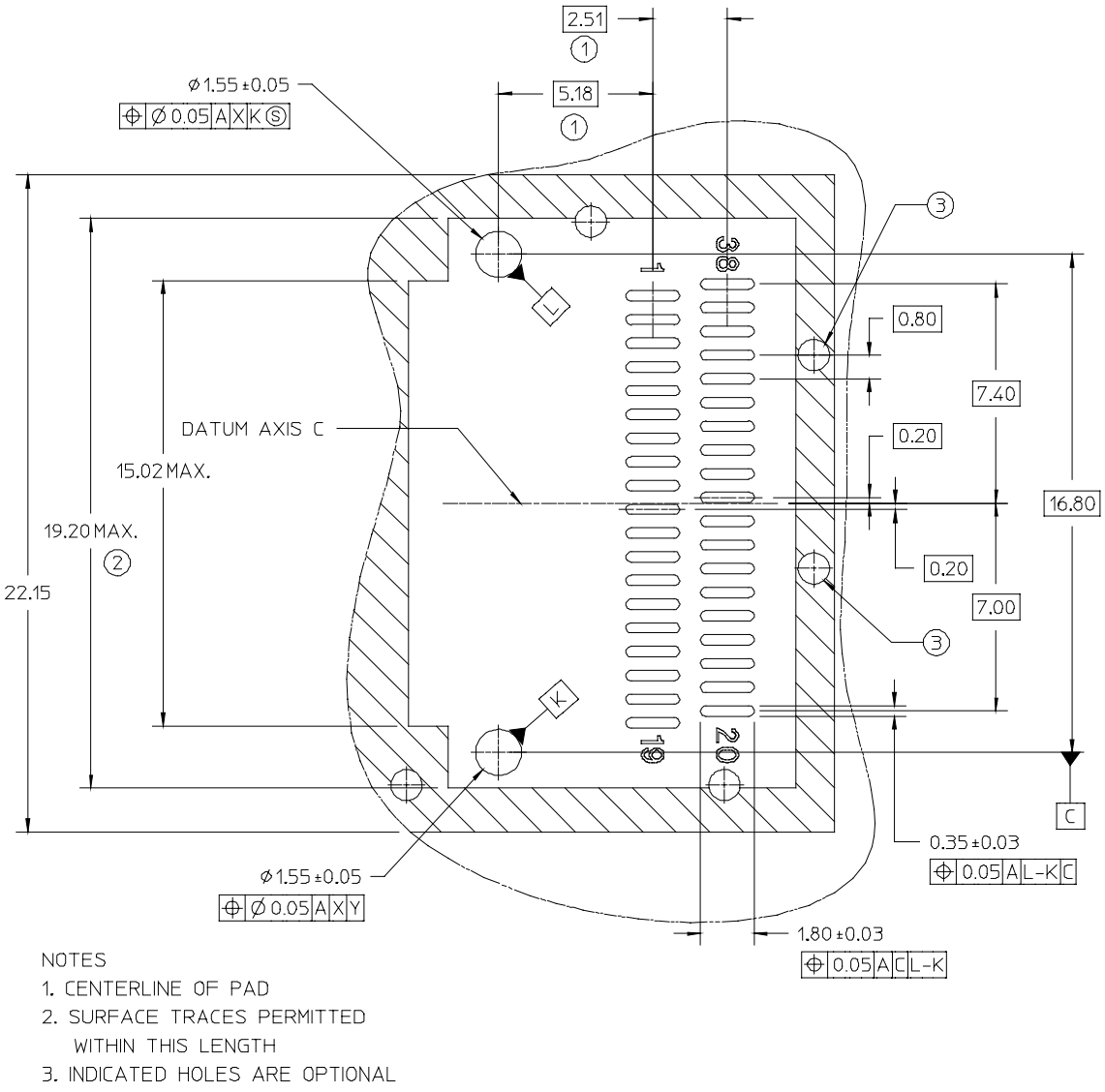



**Figure 11 – QSFP+ Host PCB Mechanical Layout, Detail Z**

### 5.4.1 Insertion, Extraction and Retention Forces for QSFP+ Modules

The requirement for insertion forces, extraction forces and retention forces are specified in Table 9. The QSFP+ cage and module design combinations must ensure excessive force applied to a cable does not damage the QSFP+ cage or host connector. If any part is damaged by excessive force, it should be the cable or media module and not the cage or host connector which is part of the host system.

**Table 9 – Insertion, Extraction and Retention Forces**

| Measurement | Min | Max | Units | Comments |
|---|---|---|---|---|
| QSFP+ Module insertion | 0 | 40 | N | |
| QSFP+ Module extraction | 0 | 30 | N | |
| QSFP+ Module retention | 90 | N/A | N | No damage to module below 90N |
| Cage retention (Latch strength) | 180 | N/A | N | No damage to latch below 180N |
| Cage retention in Host Board | 114 | N/A | N | Force to be applied in a vertical direction, no |

| | | | | |
|---|---|---|---|---|
| | | | | damage to cage |
| Insertion / removal cycles, connector / cage | 100 | N/A | Cyc. | Number of cycles for the connector and cage with multiple Modules. |
| Insertion / removal cycles, QSFP+ Module | 50 | N/A | Cyc. | Number of cycles for an individual module. |

## 5.5 Color Coding and Labeling of QSFP+ Modules

An exposed feature of the QSFP+ Module (a feature or surface extending outside of the bezel) shall be color coded as follows:
Beige for 850nm
Blue for 1310nm
White for 1550nm

Each QSFP+ Module shall be clearly labeled. The complete labeling need not be visible when the QSFP+ Module is installed and the bottom of the device is the recommended location for the label. Labeling shall include:
Appropriate manufacturing and part number identification
Appropriate regulatory compliance labeling
A manufacturing trace ability code

The label should also include clear specification of the external port characteristics such as:
Optical wavelength
Required fiber characteristics
Operating data rate
Interface standards supported
Link length supported

The labeling shall not interfere with the mechanical, thermal or EMI features.

## 5.6 Bezel for Systems Using QSFP+ Modules

Host enclosures that use QSFP+ devices should provide appropriate clearances between the QSFP+ Modules to allow insertion and extraction without the use of special tools and a bezel enclosure with sufficient mechanical strength. The QSFP+ Module insertion slot should be clear of nearby moldings and covers that might block convenient access to the latching mechanisms, the QSFP+ Module, or the cables that plug directly into the cage.

There are two cage designs that are shown for use with systems implementing QSFP+. Devices as described in Clauses 5.6.1 and 5.6.2. The difference between them is that the front of one cage extends into or through the opening in the bezel and the other extends up against the back surface of the bezel. While the cage footprint is the same for both designs, its distance from the inside surface of the host bezel may differ depending on gasket selection. The recommended basic dimension from the inside surface of the bezel to Datum K and Datum L on the Host board may be different between designs and is addressed in Figures 12a and 12b.
These designs align with the two versions for cage assemblies as defined in Section 5.8. The minimum recommended host board thickness for belly-to-belly mounting of the assemblies is different for each bezel version as noted in 5.6.1 and 5.6.2.

The bezel thickness range shall be 0.8 mm to 2.6 mm.

### 5.6.1 Bezel for the Thru Bezel Cage Assembly Version

The front surface of the cage assembly passes through the bezel.
Two EMI solutions may be implemented for this option. If EMI spring fingers are used, they make contact to the inside of the bezel cutouts. If an EMI gasket is used, it makes contact

to the inside surface of the bezel. To accept all cage designs, both bezel surfaces must be conductive and connected to chassis ground.
The minimum recommended host board thickness for belly to belly mounting of the connector and cage assemblies is 2.2mm minimum.

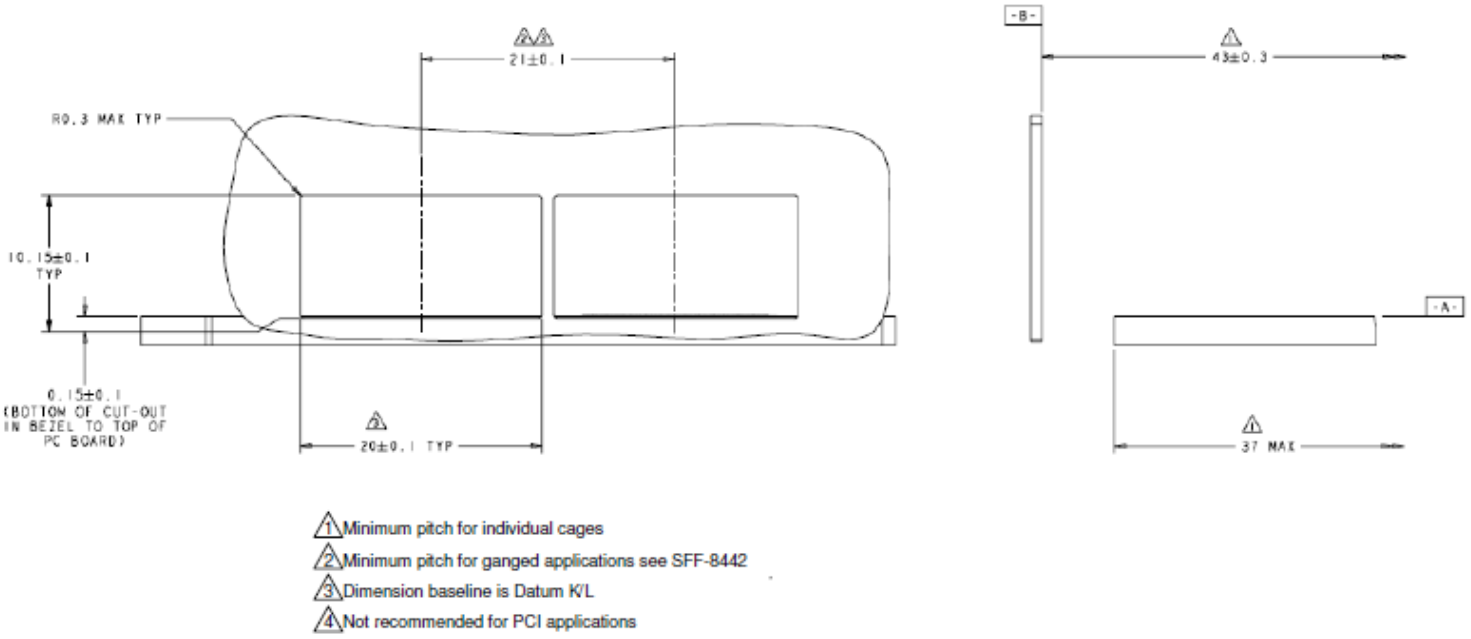



**Figure 12A – Recommended Bezel Design for cages that extend into or thru Bezel**

### 5.6.2 Bezel for the Behind the Bezel Cage Assembly Version

There are many options for a bezel EMI gasket that functions as a seal between the bezel and the front of the cage. The design of the bezel EMI gasket and the materials used for the gasket are application specific. The preferred method is to fasten the gasket to the back of the bezel with a pressure sensitive adhesive.

Assembly of the host board to the bezel will compress the gasket to the recommended range specified by the bezel EMI gasket manufacturer. The surface in the back of the bezel that is in contact with the bezel EMI gasket must be low resistance and connected to chassis ground.
The minimum recommended host board thickness for belly to belly mounting of the connector and cage assemblies is 2.7mm minimum.

The gasket thickness after compression can be calculated as follows:

GT = BKL – 42.80 +/- 0.25mm.

Where:

• GT is gasket thickness in the compressed state.

• BKL is the distance from the back of the bezel to the centerline of Datums K & L. See Figure 10 and Figure 11 (Note: dimension from front of bezel to centerline of Datums K & L must not exceed 48.25mm).

• The 42.80 +/- •0.25mm dimension is the distance from the front of the cage to the hard stop, Datum T. See Figure 16B.

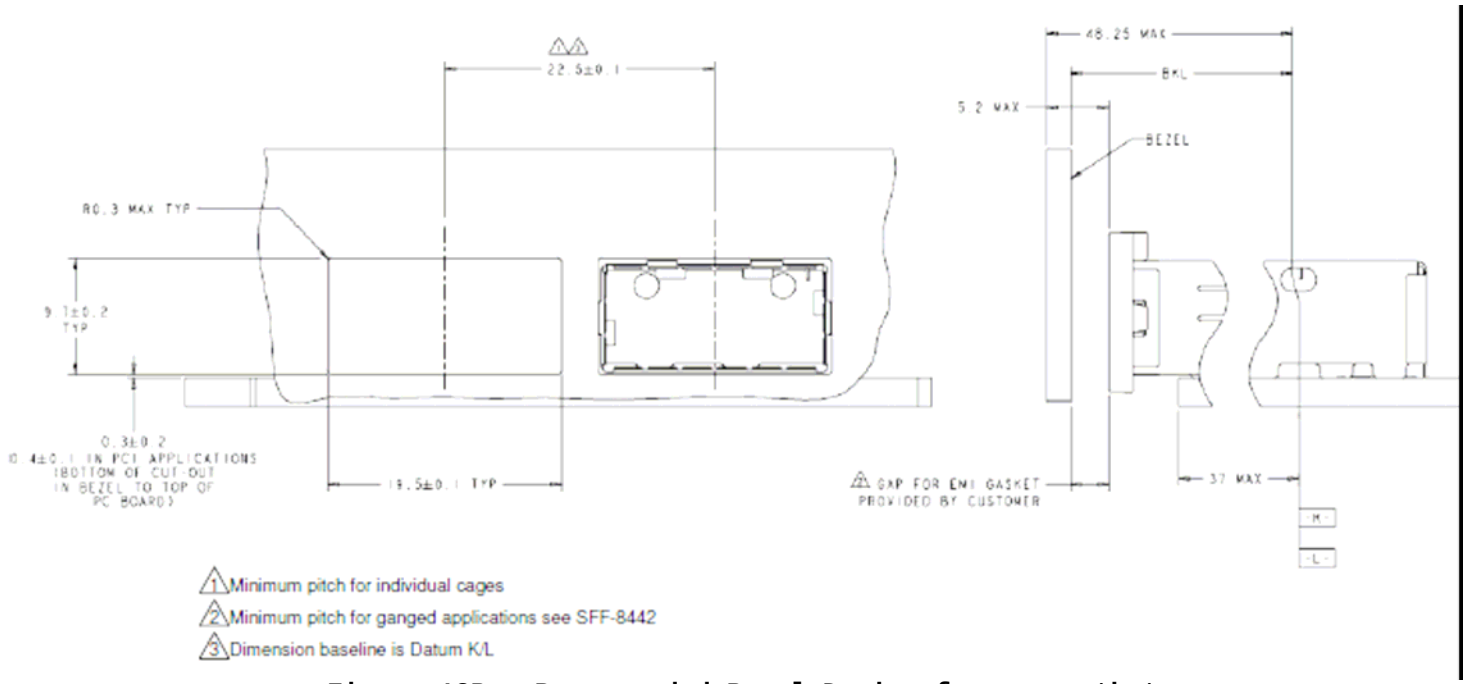



**Figure 12B – Recommended Bezel Design for cages that extend up against the inside surface of the Bezel**

## 5.7 QSFP+ Electrical Connector Mechanical

The QSFP+ Connector is a 38-contact, right angle surface mount connector and is shown in Figure 13. The mechanical specifications for the connector are listed in Table 9 and shown in Figure 14.

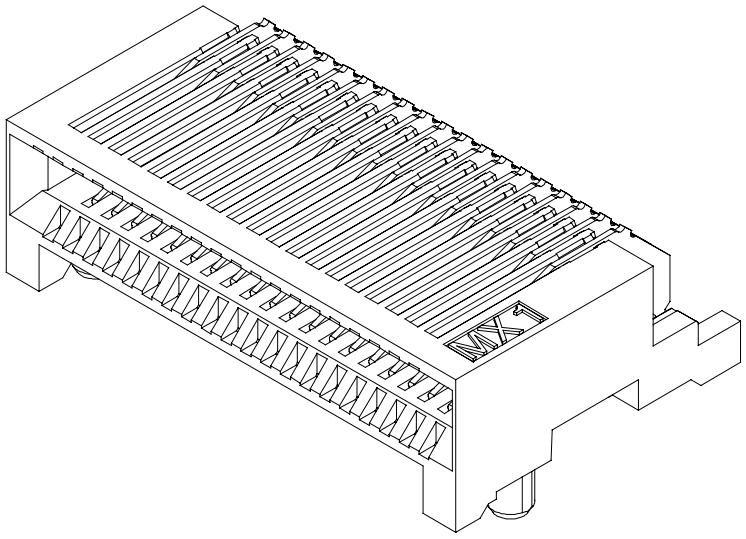


**Figure 13 – QSFP+ Module Electrical Connector Illustration**

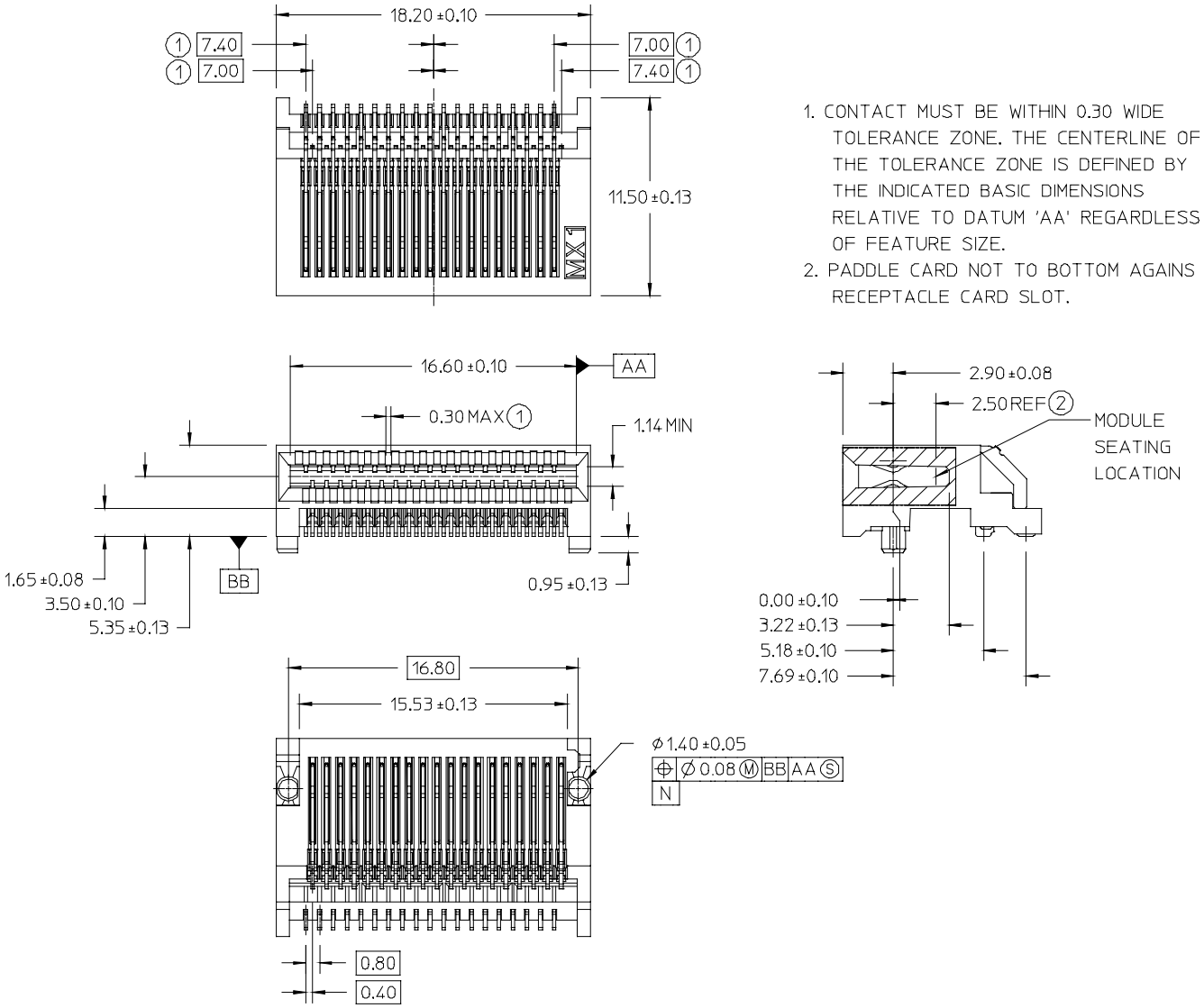



**Figure 14 – QSFP+ Electrical Connector Specification**

## 5.8 Individual QSFP+ Cage Assembly Versions

There are two versions for cage assemblies: a Thru Bezel version that passes through the bezel, and a Behind the Bezel version that does not pass through the bezel. An exploded view of a complete 1-by-1 assembly of a Thru Bezel Cage Assembly is shown schematically in Figure 15.

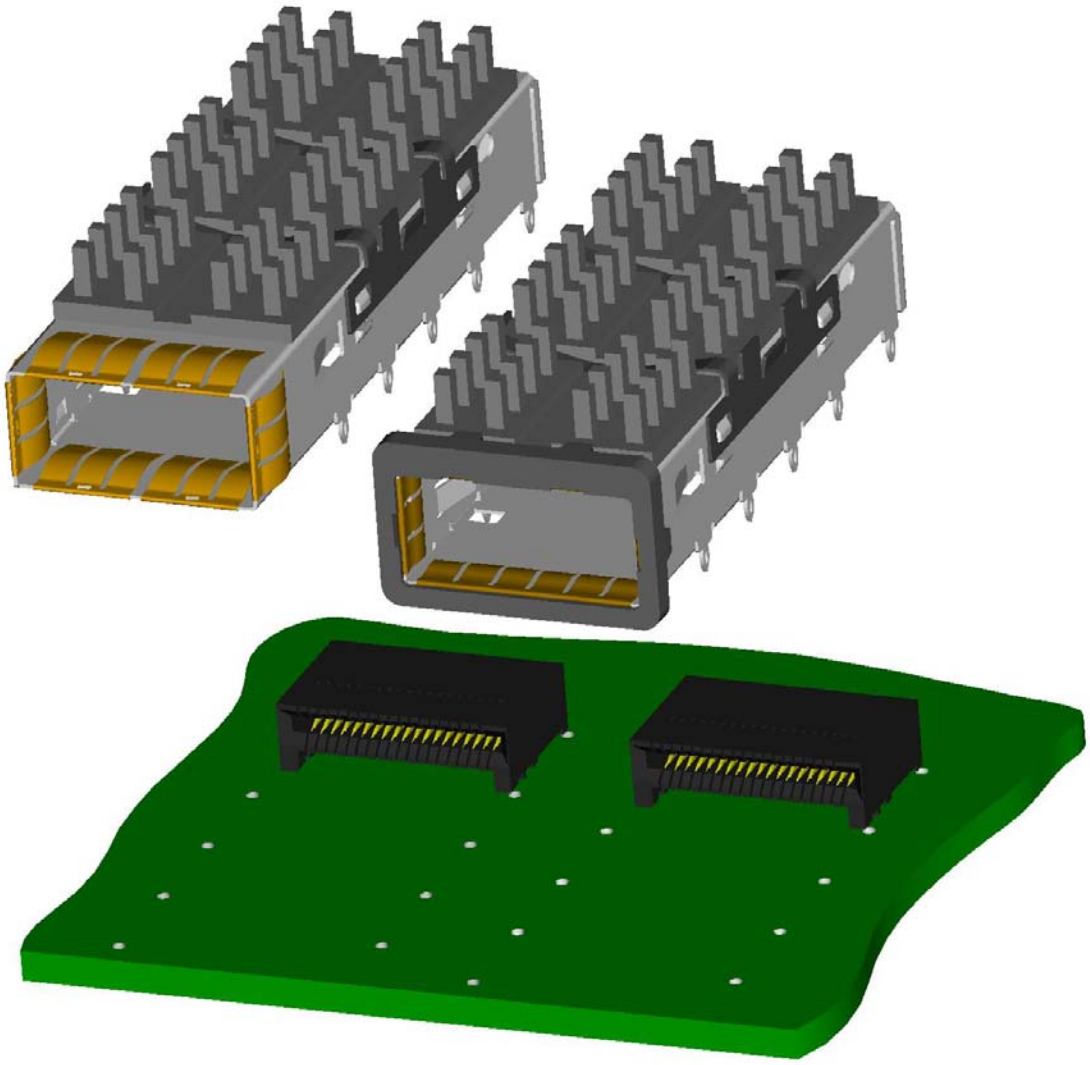


Figure 15 – Thru Bezel Cage and Optional Heat Sink Designs (exploded view)

The detailed drawings for the cage assembly options are shown in Figures 16A and 16B.

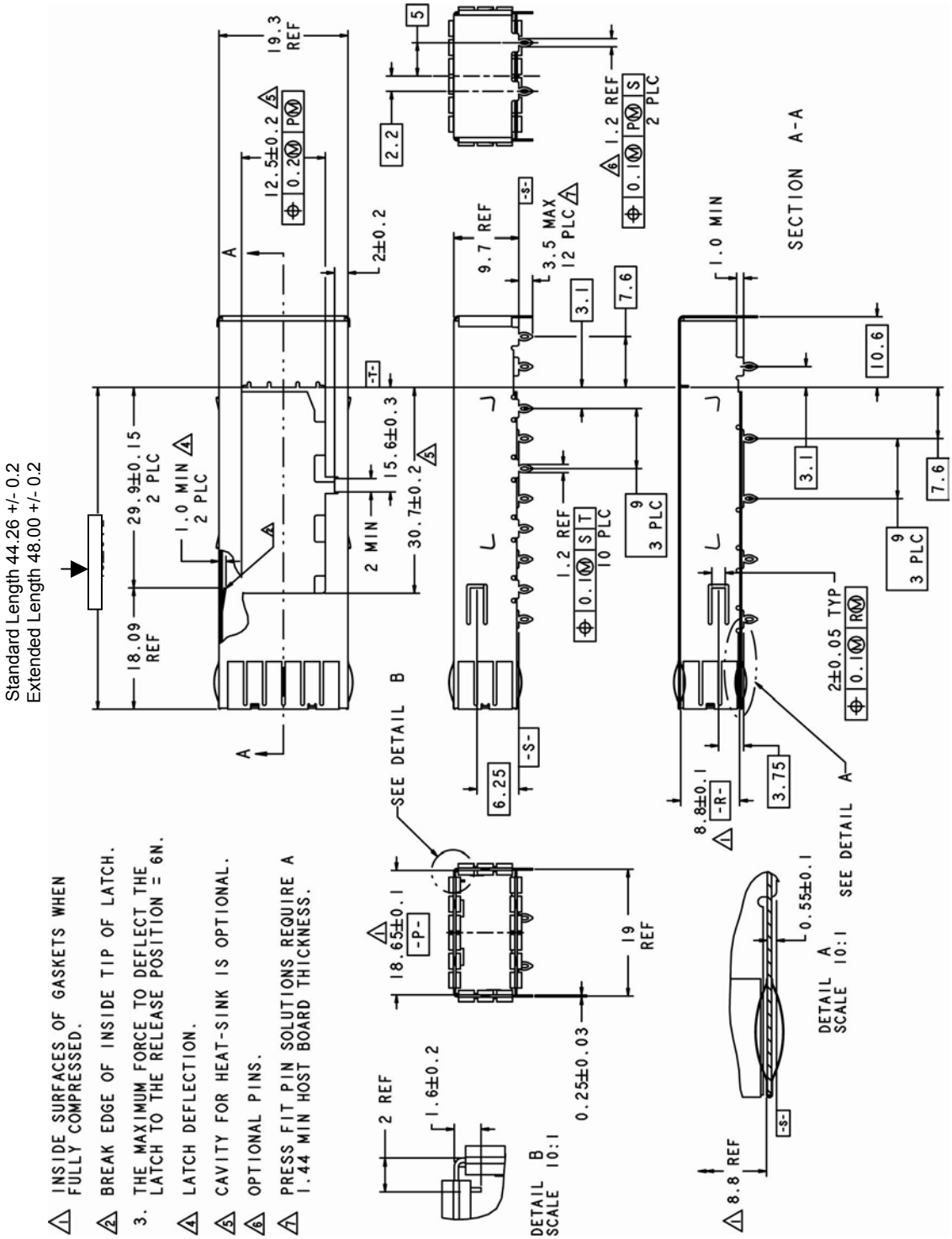



**Figure 16A – 1-by-1 Thru Bezel Cage Design**

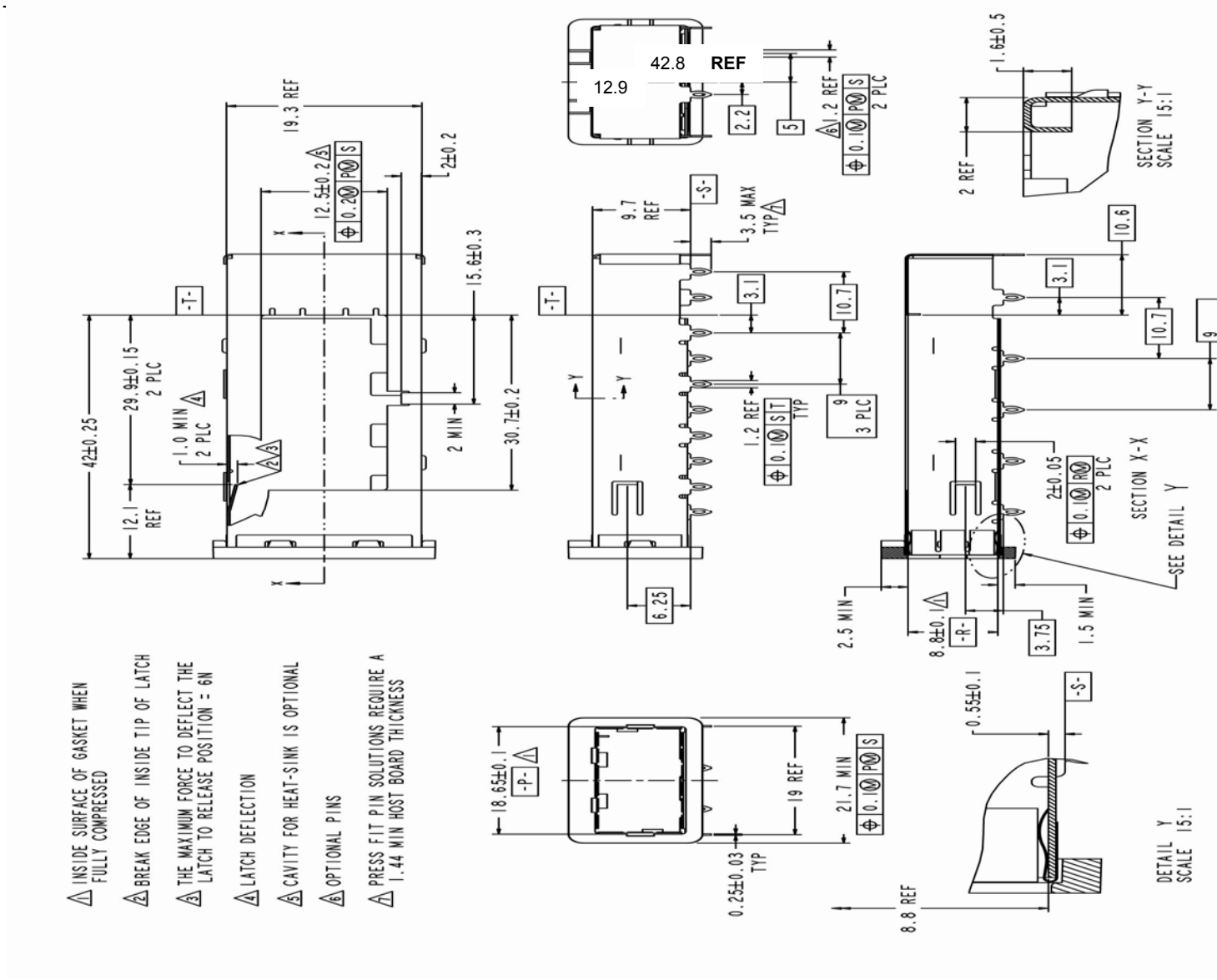



**Figure 16B – 1-by-1 Behind the Bezel Cage Design**

### 5.8.1 QSFP+ Heat Sink Clip Dimensions

The heat sink clip defined in Figure 17 is for reference only. The design of the heat sink clip, heat sink and their attachment features on the cage assembly are vendor specific and not defined in this document. When fastened to the cage, the clip will provide a minimum force of 5 Newtons at the interface of the heat sink and QSFP+ Module. The clip is designed to permit a heat sink to be fastened into the clip then assembled to the cage and to expand slightly during module insertion in order to maintain a contact force between the module and heat sink.

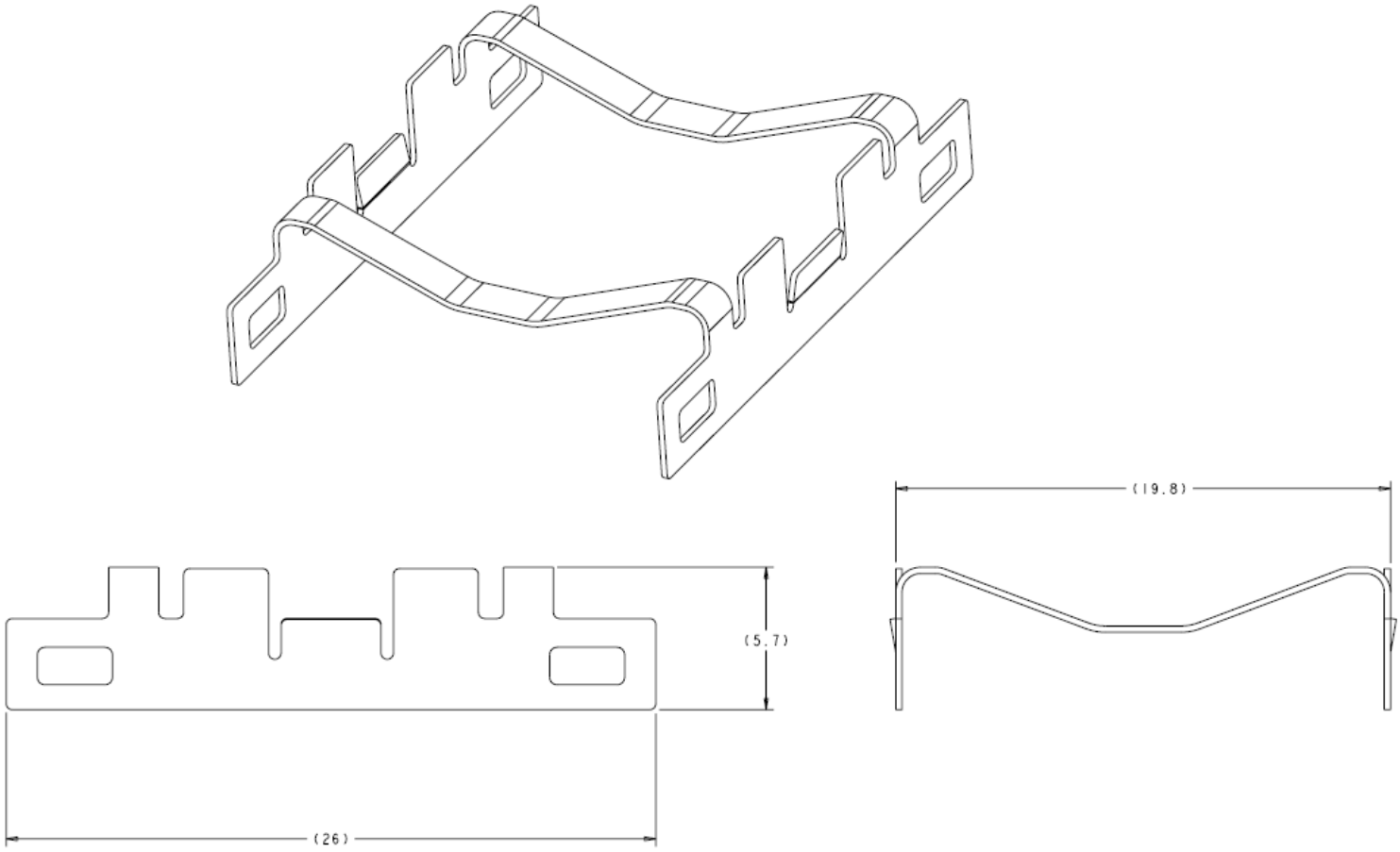



**Figure 17 – QSFP+ Heat Sink Clip**

### 5.8.2 QSFP+ Heat Sink Dimensions

The heat sink illustrated in Figure 18 is for reference only. Critical dimensions to ensure that the heat sink will be compatible with the Heat Sink Clip are defined. The configuration of the fins or posts is application specific along with the outside envelope. The heat sink includes a beveled edge which “rides up” the leading edge of the module as the module is inserted into the cage assembly. The recommended material for the heat sink is aluminum and the surface treatment for the module contacting surface can be anodizing or nickel plating.

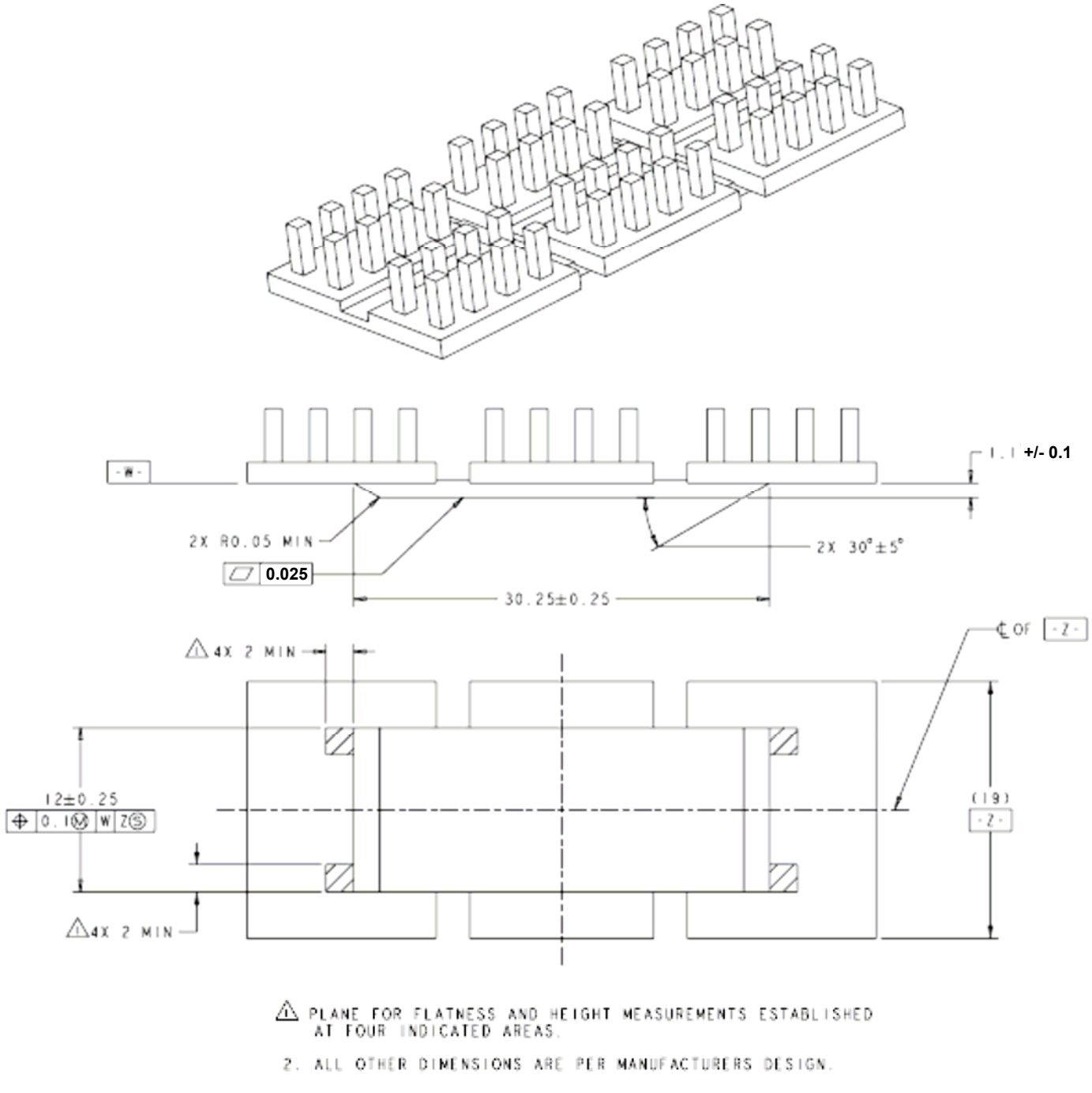



**Figure 18 – QSFP+ Heat Sink**

### 5.8.3 Light Pipes

The use of light pipes to indicate status of the module is application specific.

### 5.9 Dust / EMI Cover

In order to prevent contamination of the internal components and to optimize EMI performance, it is recommended that a Dust/EMI Cover be inserted into the cage assembly when no module is present. See Figure 19 for the recommended design. During installation, the front flange on the cover shall be seated against the front surface of the bezel to prevent dust from entering the equipment. The conductivity of the materials should be chosen for the Dust/EMI Cover to block EMI emissions.

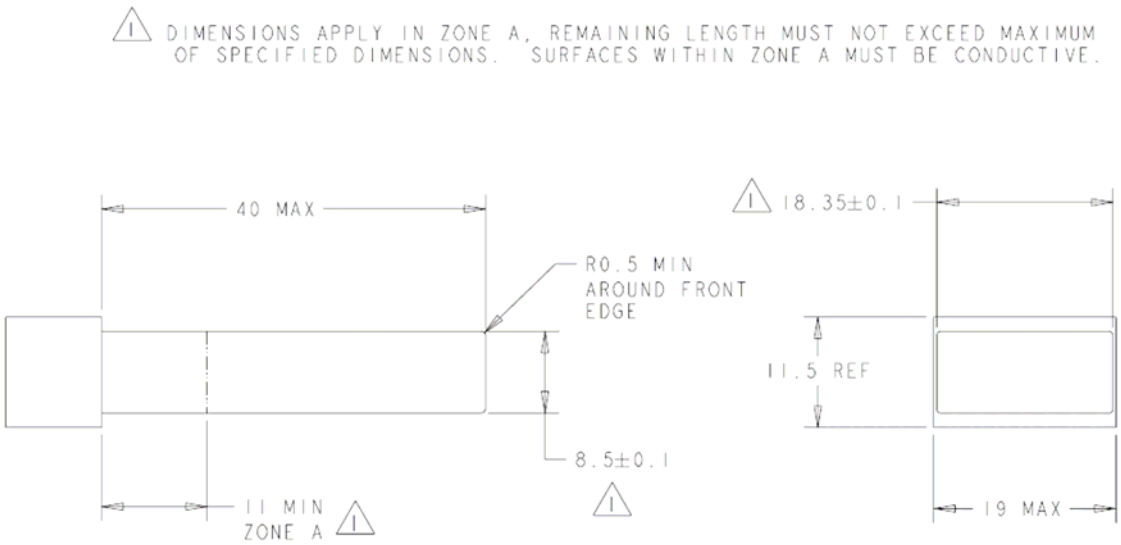



**Figure 19 – Dust / EMI Cover**

**5.10 Optical Interface**

The QSFP+ optical interface port shall be a male MPO connector as specified in IEC 61754-7.

The four fiber positions on the left as shown in Fig. 20a, with the key up, are used for the optical transmit signals (Channel 1 through 4). The fiber positions on the right are used for the optical receive signals (Channel 4 through 1).

The central four fibers may be physically present.
Two alignment pins are present.

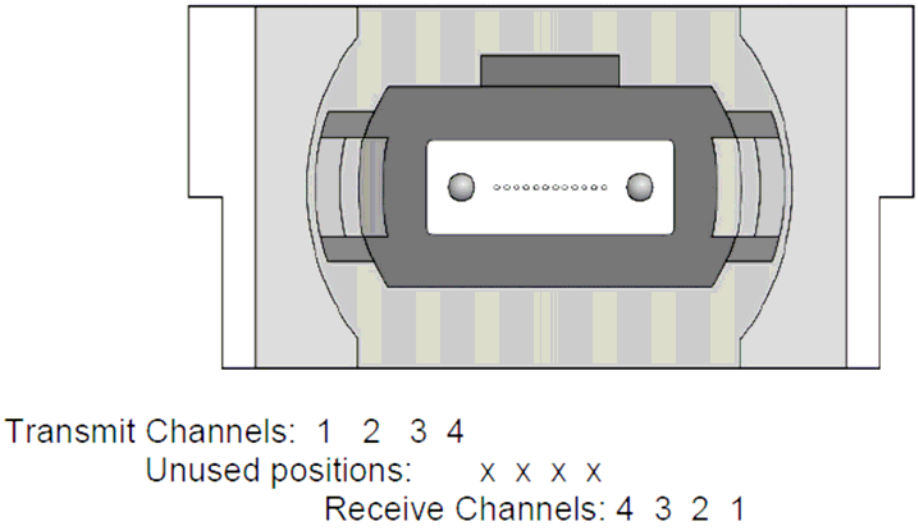



**Figure 20a – QSFP+ Optical Receptacle and Channel Orientation**

Optical Cable connection

Aligned key (Type B) MPO patchcords should be used to ensure alignment of the signals between the modules. The aligned key patchcord is defined in TIA-568 and shown in Figure 20b. The optical connector is orientated such that the keying feature of the MPO receptacle is on the top.

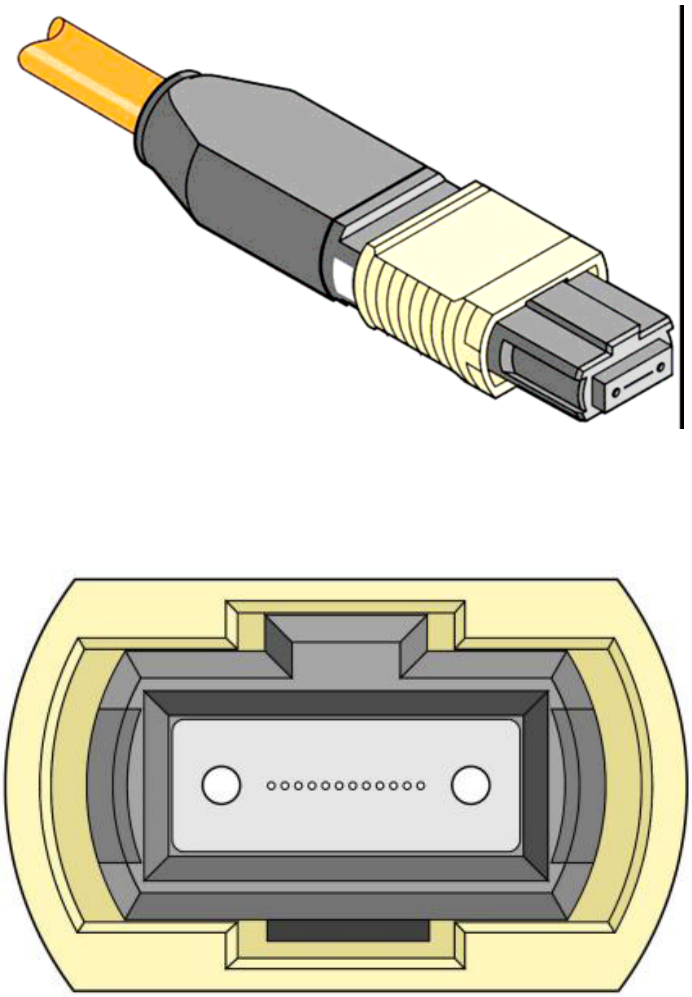


Figure 20b – QSFP+ Optical patchcord

## 6 Environmental and Thermal

### 6.1 Thermal Requirements

The QSFP+ module shall operate within one or more of the case temperatures ranges defined in Table 10. The temperature ranges are applicable between 60m below sea level and 1800m above sea level, (Ref. NEBS GR-63) utilizing the host systems designed airflow.

| Class | Case Temperature Range |
|---|---|
| Standard | 0 through 70C |
| Extended | -5 through 85C |
| Industrial | -40 through 85C |

QSFP+ is designed to allow for up to 16 adjacent modules, ganged and/or belly-to-belly, with the appropriate thermal design for cooling / airflow. (Ref. NEBS GR-63)

## 7 Management Interface

### 7.1 Introduction

A management interface, as already commonly used in other form factors like GBIC, SFP, and XFP, is specified in order to enable flexible use of the module by the user. The specification has been changed in order to adopt the use of a multi-channel module. Some

timing requirements are critical especially for a multi-channel device, so the interface speed has been increased.

## 7.2 Timing Specification

### 7.2.1 Introduction

Low speed signaling is based on Low Voltage CMOS (LVCMOS) operating at Vcc. Hosts shall use a pull-up resistor connected to a Vcc_host on the 2-wire interface SCL (clock) and SDA (Data) signals. Detailed electrical specification is given in Clause 3.1.2. Nomenclature for all registers more than 1 bit long is MSB-LSB.

### 7.2.2 Management Interface Timing Specification

In order to support a multi-channel device a higher clock rate for the serial interface is considered. The timing requirements are shown in Figure 21 and specified in Table 11. QSFP+ is positioned to leverage 2-wire timing (Fast Mode devices) to align the use of related cores on host ASICs. This clause closely follows the XFP MSA specification.

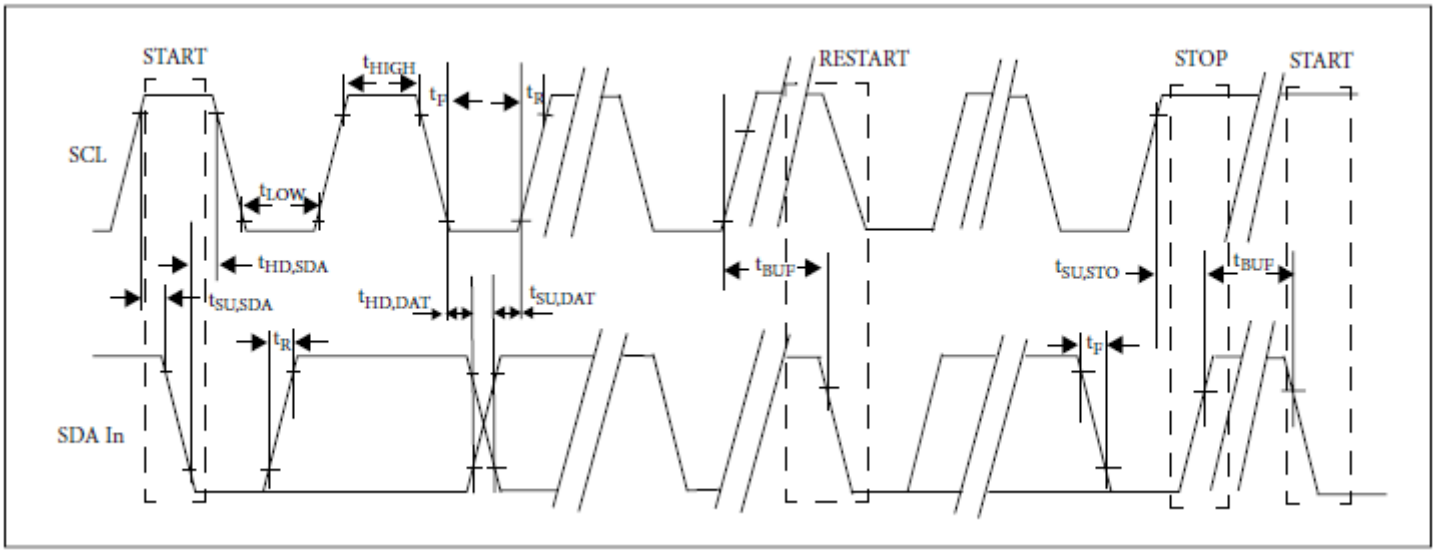



**Figure 21 – QSFP+ Timing Diagram**

Before initiating a 2-wire serial bus communication, the host shall provide setup time (Host_select_setup -Table 11) on the ModSelL line of all modules on the 2-wire bus. The host shall not change the ModSelL line of any module until the 2-wire serial bus communication is complete and the hold time requirement (Host_select_hold - Table 11) is satisfied. The 2-wire serial interface address of the QSFP+ module is 1010000X (A0h). In order to allow access to multiple QSFP+ modules on the same 2-wire serial bus, the QSFP+ pinout includes a ModSelL or module select pin. This pin (which is pulled high or deselected in the module) must be held low by the host to select the module of interest and allow communication over the 2-wire serial interface. The module must not respond to or accept 2-wire serial bus instructions unless it is selected.

### 7.2.3 Serial Interface Protocol

The module asserts LOW for clock stretch on SCL.

#### 7.2.3.1 Management Timing Parameters

The timing parameters for the 2-Wire interface to the QSFP+ module are shown in Table 11.

**Table 11 Management Interface timing parameters**

| Parameter | Symbol | Min | Max | Unit | Conditions |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| Clock Frequency | $f_{SCL}$ | 0 | 400 | kHz | |
| Clock Pulse Width Low | $t_{LOW}$ | 1.3 | | us | |
| Clock Pulse Width High | $t_{HIGH}$ | 0.6 | | us | |
| Time bus free before new transmission can start | $t_{BUF}$ | 20 | | us | Between STOP and START and between ACK and ReStart |
| START Hold Time | $t_{HD.STA}$ | 0.6 | | us | |
| START Set-up Time | $t_{SU.STA}$ | 0.6 | | us | |
| Data In Hold Time | $t_{HD.DAT}$ | 0 | | us | |
| Data in Set-up Time | $t_{SU.DAT}$ | 0.1 | | us | |
| Input Rise Time (400kHz) | $t_{R.400}$ | | 300 | ns | From (VIL,MAX-0.15) to (VIH, MIN +0.15) |
| Input Fall Time (400kHz) | $t_{F,400}$ | | 300 | ns | From (VIH,MIN + 0.15) to (VIL,MAX – 0.15) |
| STOP Set-up Time | $t_{SU,STO}$ | 0.6 | | us | |
| ModSelL Setup Time | Host_select_setup | 2 | | ms | Setup time on the select lines before start of a host initiated serial bus sequence |
| ModSelL Hold Time | Host_select_hold | 10 | | us | Delay from completion of a serial bus sequence to changes of Module select status |
| Aborted sequence – bus release | Deselect _Abort | 2 | | ms | Delay from a host de-asserting ModSelL (at any point in a bus sequence) to the QSFP+ module releasing SCL and SDA |

## 7.3 Memory Interaction Specifications

QSFP+ memory transaction timings are given in Table 12. Single byte writable memory blocks are given in Table 13. Multiple byte writable memory blocks are defined in Table 14.

**Table 12- QSFP+ Memory Specification**

| Parameter | Symbol | Min | Max | Unit | Conditions |
|---|---|---|---|---|---|
| Serial Interface Clock Holdoff “Clock Stretching” | T_clock_hold | | 500 | us | Maximum time the QSFP+ module may hold the SCL line low before continuing with a read or write operation |
| Complete Single or Sequential Write | $t_{WR}$ | | 40 | ms | Complete (up to) 4 Byte Write |
| Endurance (Write Cycles) | | 50K | | cycles | 70 $^{0}$C |

**Table 13- Single Byte Writable Memory Block**

| Page | Address | Volatile or Nonvolatile | Description |
|---|---|---|---|
| A0h | 86 | Volatile | Control register |
| A0h | 87 | Volatile | Rx Rate select register |

| | | | |
|---|---|---|---|
| A0h | 88 | Volatile | Tx Rate select register |
| A0h | 127 | Volatile | Page Select Byte |

**Table 14- Multiple Byte Writable Memory Block**

| Address | # Bytes | Volatile/NonVolatile | Description |
|---|---|---|---|
| 89-92 | 4 | Volatile | Application select per channel |
| 100-106 | 7 | Volatile | Module Mask |
| 119-122 | 4 | Volatile | Password Change Entry Area (Optional) |
| 123-126 | 4 | Volatile | Password Entry Area (Optional) |
| 128-255 | 128 | Non-Volatile | User Writable memory – Page 02h |
| 225-241 | 16 | Volatile | Vendor Specific Channel Controls–Page 03h |
| 242-253 | 12 | Volatile | Channel Monitor Masks – Page 03h |

### 7.3.1 Timing for Soft Control and Status Functions

Timing for QSFP+ soft control and status functions are described in Table 15

**Table 15- Timing for QSFP+ soft control and status functions**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Initialization time | t_init | 2000 | ms | Time from power on[2], hot plug or rising edge of reset until the module is fully functional[3] This time does not apply to non-Power level 0 modules in Low Power State |
| Reset Init Assert Time | t_reset_init | 2 | us | A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin |
| Serial Bus Hardware Ready Time | t_serial | 2000 | ms | Time from power on[2] until module responds to data transmission over the 2-wire serial bus |
| Monitor Data Ready Time | t_data | 2000 | ms | Time from power on[2] to data not ready, bit 0 of Byte 2, deasserted and IntL asserted |
| Reset Assert Time | t_reset | 2000 | ms | Time from rising edge on the ResetL pin until the module is fully functional[3] |
| LPMode Assert Time | ton_LPMode | 100 | us | Time for assertion of LPMode (Vin: LPMode=Vih)until module power consumption reaches Power Level 1. |
| IntL Assert Time | ton_IntL | 200 | ms | Time from occurrence of condition triggering IntL until Vout:IntL=Vol |
| IntL Deassert Time | toff_IntL | 500 | us | Time from clear on read[4] operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits. |
| Rx LOS Assert Time | ton_los | 100 | ms | Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted. |
| Tx Fault Assert Time | ton_Txfault | 200 | ms | Time from Tx Fault state to Tx Fault bit set (value = 1b) and IntL asserted. |
| Flag Assert Time | ton_flag | 200 | ms | Time from occurrence of condition triggering flag to associated flag bit set (value = 1b) and IntL asserted. |
| Mask Assert Time | ton_mask | 100 | ms | Time from mask bit set (value = 1b)[1] until associated IntL assertion is inhibited |
| Mask Deassert Time | toff_mask | 100 | ms | Time from mask bit cleared (value = 0b)[1] until associated IntL operation resumes |

| | | | | |
|---|---|---|---|---|
| Application or Rate Select Change Time | t_ratesel | 100 | ms | Time from change of state of Application or Rate Select bit[1] until transmitter or receiver bandwidth is in conformance with appropriate specification |
| Power_over-ride or Power-set Assert Time | ton_Pdown | 100 | ms | Time from P_Down bit set (value = 1b)[1] until module power consumption reaches Power Level 1 |
| Power_over-ride or Power-set Deassert Time | toff_Pdown | 300 | ms | Time from P_Down bit cleared (value = 0b)[1] until the module is fully functional[3] |
| Note 1. Measured from falling clock edge after stop bit of write transaction | | | | |
| Note 2. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 6 | | | | |
| Note 3. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2, deasserted. The module should also meet optical and electrical specifications. | | | | |
| Note 4. Measured from falling clock edge after stop bit of read transaction | | | | |

Squelch and disable timings are defined in Table 16.

**Table 16 - I/O Timing for Squelch & Disable**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Rx Squelch Assert Time | ton_Rxsq | 80 | us | Time from loss of Rx input signal until the squelched output condition is reached. See Clause 3.1.3.1. |
| Rx Squelch Deassert Time | toff_Rxsq | 80 | us | Time from resumption of Rx input signals until normal Rx output condition is reached. See clause 3.1.3.1. |
| Tx Squelch Assert Time | ton_Txsq | 400 | ms | Time from loss of Tx input signal until the squelched output condition is reached. See clause 3.1.3.2. |
| Tx Squelch Deassert Time | toff_Txsq | 400 | ms | Time from resumption of Tx input signals until normal Tx output condition is reached. See clause 3.1.3.2. |
| Tx Disable Assert Time | ton_txdis | 100 | ms | Time from Tx Disable bit set (value = 1b)[1] until optical output falls below 10% of nominal |
| Tx Disable Deassert Time | toff_txdis | 400 | ms | Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal |
| Rx Output Disable Assert Time | ton_rxdis | 100 | ms | Time from Rx Output Disable bit set (value = 1b)[1] until Rx output falls below 10% of nominal |
| Rx Output Disable Deassert Time | toff_rxdis | 100 | ms | Time from Rx Output Disable bit cleared (value = 0b)[1] until Rx output rises above 90% of nominal |
| Squelch Disable Assert Time | ton_sqdis | 100 | ms | This applies to Rx and Tx Squelch and is the time from bit set (value = 0b)[1] until squelch functionality is disabled. |
| Squelch Disable Deassert Time | toff_sqdis | 100 | ms | This applies to Rx and Tx Squelch and is the time from bit cleared (value = 0b)[1] until squelch functionality is enabled |
| Note 1: Measured from falling clock edge after stop bit of write transaction | | | | |

## 7.4 Device Addressing and Operation

Serial Clock (SCL): The host supplied SCL input to QSFP+ Modules is used to positive-edge clock data into each QSFP+ device and negative-edge clock data out of each device. The SCL line may be pulled low by an QSFP+ module during clock stretching.
Serial Data (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain or open-collector driven and may be wire-ORed with any number of open-drain or open collector devices. Master/Slave: QSFP+ Modules operate only as slave devices. The host must provide a bus master for SCL and initiate all read/write communication.
Device Address: Each QSFP+ is hard wired at the device address A0h. See Clause 6.6 for memory structure within each Module.
Multiple Devices per SCL/SDA: While QSFP+ Modules are compatible with point-to-point SCL/SDA, they can share a single SCL/SDA bus by using the QSFP+ ModSelL line. See Clause 3.1.1.1,Clause 3.1.2 and Table 3 for more information.
Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods indicate a START or STOP condition. All addresses and data words are serially transmitted to and from the QSFP+ in 8-bit words.
Every byte on the SDA line must be 8-bits long. Data is transferred with the most significant bit (MSB) first. START Condition: A high-to-low transition of SDA with SCL high is a START condition, which must precede any other command.
STOP Condition: A low-to-high transition of SDA with SCL high is a STOP condition.
Acknowledge: After sending each 8-bit word, the transmitter releases the SDA line for one bit time, during which the receiver is allowed to pull SDA low (zero) to acknowledge (ACK) that it has received each word.
Device address bytes and write data bytes initiated by the host shall be acknowledged by QSFP+ Modules. Read data bytes transmitted by QSFP+ Modules shall be acknowledged by the host for all but the final byte read, for which the host shall respond with a STOP instead of an ACK.
Memory (Management Interface) Reset: After an interruption in protocol, power loss or system reset the QSFP+ management interface can be reset. Memory reset is intended only to reset the QSFP+ Module management interface (to correct a hung bus). No other Module functionality is implied.
1) Clock up to 9 cycles.
2) Look for SDA high in each cycle while SCL is high.
3) Create a START condition as SDA is high
Device Addressing: QSFP+ devices require an 8-bit device address word following a start condition to enable a read or write operation. The device address word consists of a mandatory sequence for the first seven most significant bits in Figure 22. This is common to all QSFP+ devices.

| 1 | 0 | 1 | 0 | 0 | 0 | 0 | R/W |
|---|---|---|---|---|---|---|---|
| MSB | | | | | | | LSB |

**Figure 22 – QSFP+ Device Address**

The eighth bit of the device address is the read/write operating select bit. A read operation is initiated if this bit is set high and a write operation is initiated if this bit is set low. Upon compare of the device address (with ModSelL in the low state) the QSFP+ Module shall output a zero (ACK) on the SDA line to acknowledge the address.

## 7.5 Read/Write Functionality

### 7.5.1 QSFP+ Memory Address Counter (Read AND Write Operations)

QSFP+ devices maintain an internal data word address counter containing the last address accessed during the latest read or write operation, incremented by one. The address counter is incremented whenever a data word is received or sent by the Module. This address stays valid between operations as long as QSFP+ power is maintained. The address “roll over” during read and writes operations is from the last byte of the 128-byte memory page to the first byte of the same page.

7.5.2 Read Operations (Current Address Read)

A current address read operation requires only the device address read word (10100001) be sent, see Figure 23. Once acknowledged by the QSFP+, the current address data word is serially clocked out. The host does not respond with an acknowledge, but does generate a STOP condition once the data word is read.

| | | ←QSRP ADDR→ | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| HOST | START | MSB | | | | | | LSB | READ | | | | | | | | | NACK | STOP |
| | | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | x | x | x | x | x | x | x | x | 1 | |
| QSFP | | | | | | | | | | ACK | MSB | | | | | | | LSB | | |
| | | | | | | | | | | | ←DATA WORD→ | | | | | | | | | |

**Figure 23 – QSFP+ Current Address Read Operation**

### 7.5.3 Read Operations (Random Read)

A random read operation requires a “dummy” write operation to load in the target byte address as shown in Figure 24. This is accomplished by the following sequence: The target 8-bit data word address is sent following the device address write word (10100000) and acknowledged by the QSFP+. The host then generates another START condition (aborting the dummy write without incrementing the counter) and a current address read by sending a device read address (10100001). The QSFP+ acknowledges the device address and serially clocks out the requested data word. The host does not respond with an acknowledge, but does generate a STOP condition once the data word is read.

| | | <-- QSFP ADDR --> | | | | | | | | | <--MEMORY ADDR-> | | | | | | | | | <QSFP ADDR-> | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| HOST | START | MSB | | | | | | LSB | WRITE | | MSB | | | | | | | LSB | | START | MSB | | | | | | LSB | READ | | | | | | | NACK | STOP |
| | | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | x | x | x | x | x | x | x | x | 0 | | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | x | x | x | x | x | x | x | x | 1 | |
| QSFP | | | | | | | | | | ACK | | | | | | | | | ACK | | | | | | | | | ACK | MSB | | | | | | | LSB | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | <DATA WORD n--> | | | | | | | | | |

**Figure 24 – QSFP+ Random Read**

#### 7.5.3.1 Read Operations (Sequential Read)

Sequential reads are initiated by either a current address read Figure 25 or a random address read Figure 26. To specify a sequential read, the host responds with an acknowledge (instead of a STOP) after each data word. As long as the QSFP+ receives an acknowledge, it shall serially clock out sequential data words. The sequence is terminated when the host responds with a NACK and a STOP instead of an acknowledge.

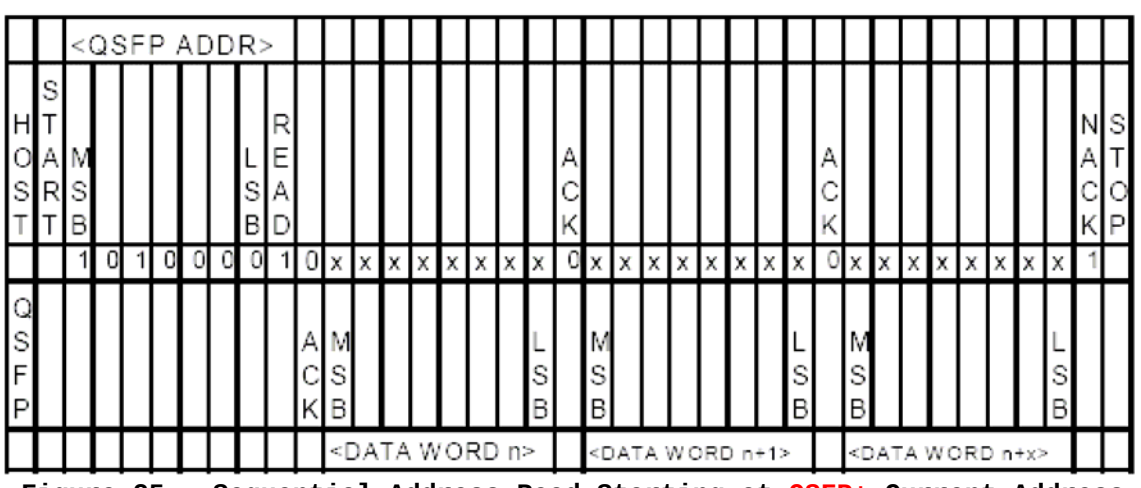



**Figure 25 – Sequential Address Read Starting at QSFP+ Current Address**

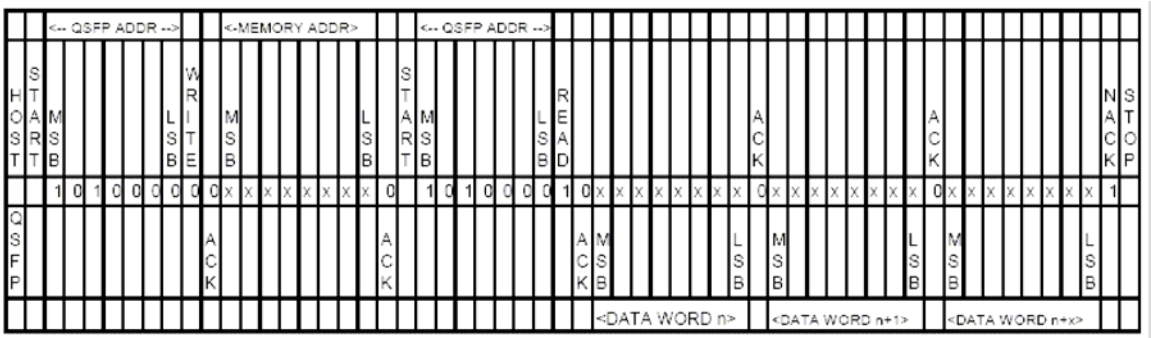



**Figure 26 – Sequential Address Read Starting with Random QSFP+ Read**

### 7.5.4 Write Operations (BYTE Write)

A write operation requires an 8-bit data word address following the device address write word (10100000) and acknowledgement, see Figure 27. Upon receipt of this address, the QSFP+ shall again respond with a zero (ACK) to acknowledge and then clock in the first 8-bit data word. Following the receipt of the 8-bit data word, the QSFP+ shall output a zero (ACK) and the host master must terminate the write sequence with a STOP condition for the write cycle to begin. If a START condition is sent in place of a STOP condition (i.e. a repeated START per the 2-wire interface specification) the write is aborted and the data received during that operation is discarded. Upon receipt of the proper STOP condition, the QSFP+ enters an internally timed write cycle, tWR, to internal memory. The QSFP+ disables it's management interface input during this write cycle and shall not respond or acknowledge subsequent commands until the write is complete. Note that 2-wire interface "Combined Format" using repeated START conditions is not supported on QSFP+ write commands.

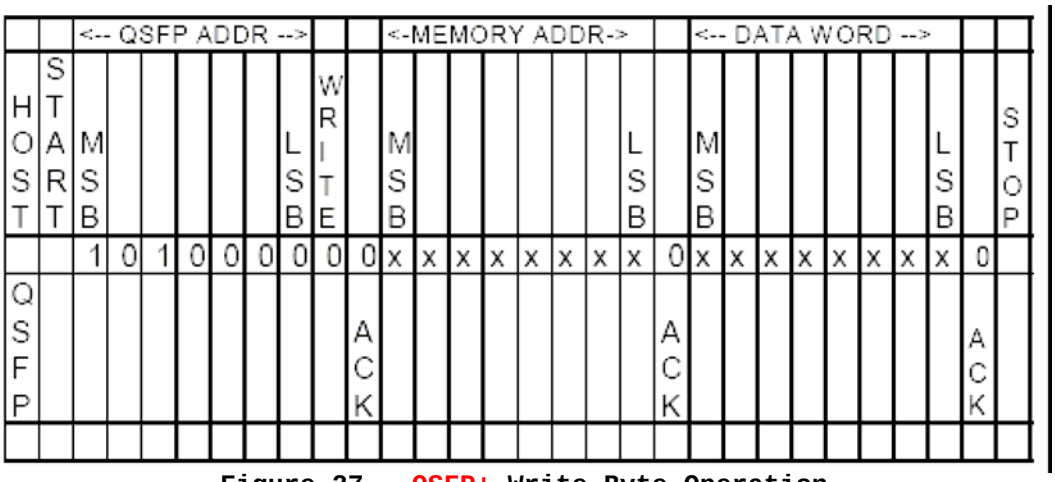



**Figure 27 – QSFP+ Write Byte Operation**

### 7.5.5 Write Operations (Sequential Write)

QSFP+'s shall support up to a 4 sequential byte write without repeatedly sending QSFP+ address and memory address information as shown in Figure 28. A "sequential" write is initiated the same way as a single byte write, but the host master does not send a stop condition after the first word is clocked in. Instead, after the QSFP+ acknowledges receipt of the first data word, the host can transmit up to three more data words. The QSFP+ shall send an acknowledge after each data word received. The host must terminate the sequential write sequence with a STOP condition or the write operation shall be aborted and data discarded. Note that 2-wire interface "combined format" using repeated START conditions is not supported on QSFP+ write commands.

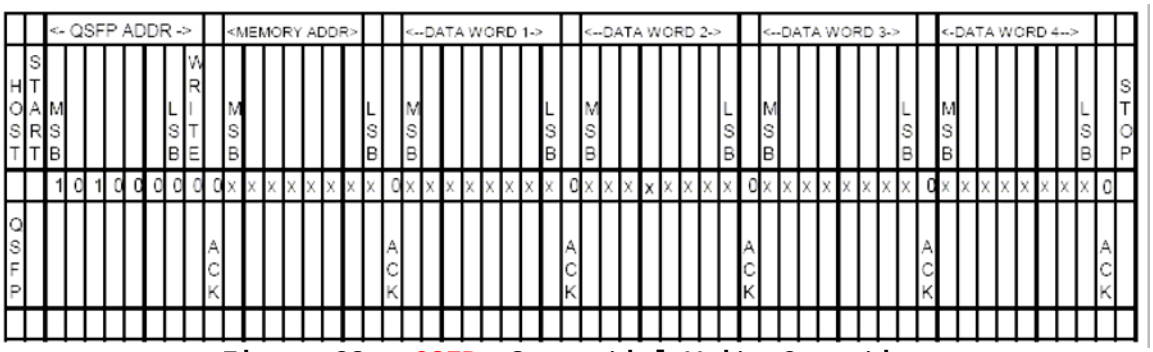



**Figure 28 – QSFP+ Sequential Write Operation**

### 7.5.6 Write Operations (Acknowledge Polling)

Once the QSFP+ internally timed write cycle has begun (and inputs are being ignored on the bus) acknowledge polling can be used to determine when the write operation is complete. This involves sending a START condition followed by the device address word. Only if the internal write cycle is complete shall the QSFP+ respond with an acknowledge to subsequent commands, indicating read or write operations can continue.

## 7.6 QSFP+ Memory Map

This subclause defines the Memory Map for QSFP+ Module used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all QSFP+ devices. The interface has been designed largely after the XFP MSA as defined in INF-8077i Rev.4.0. The memory map has been changed in order to accommodate 4 optical channels and limit the required memory space. The single address approach as used in XFP using paging for provision of more less time critical memory content is used in order to enable time critical interactions between host and Module.

The structure of the memory is shown in Figure 29. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, e.g. Interrupt Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function. The structure also provides address expansion by adding additional upper pages as needed. For example, in Figure 29 upper pages 01 and 02 are optional. Upper page 01 allows implementation of Application Select Table, and upper page 02 provides user read/write space. The lower page and upper page 00 are always implemented. Page 03 is required if byte 2, bit 2 in the lower page is set high. See Table 39 for details regarding declaration of optional upper pages 01 and 02.

The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a "one-time-read" for all data related to an interrupt situation. After an Interrupt, IntL, has been asserted, the host can read out the flag field to determine the effected channel and type of flag.

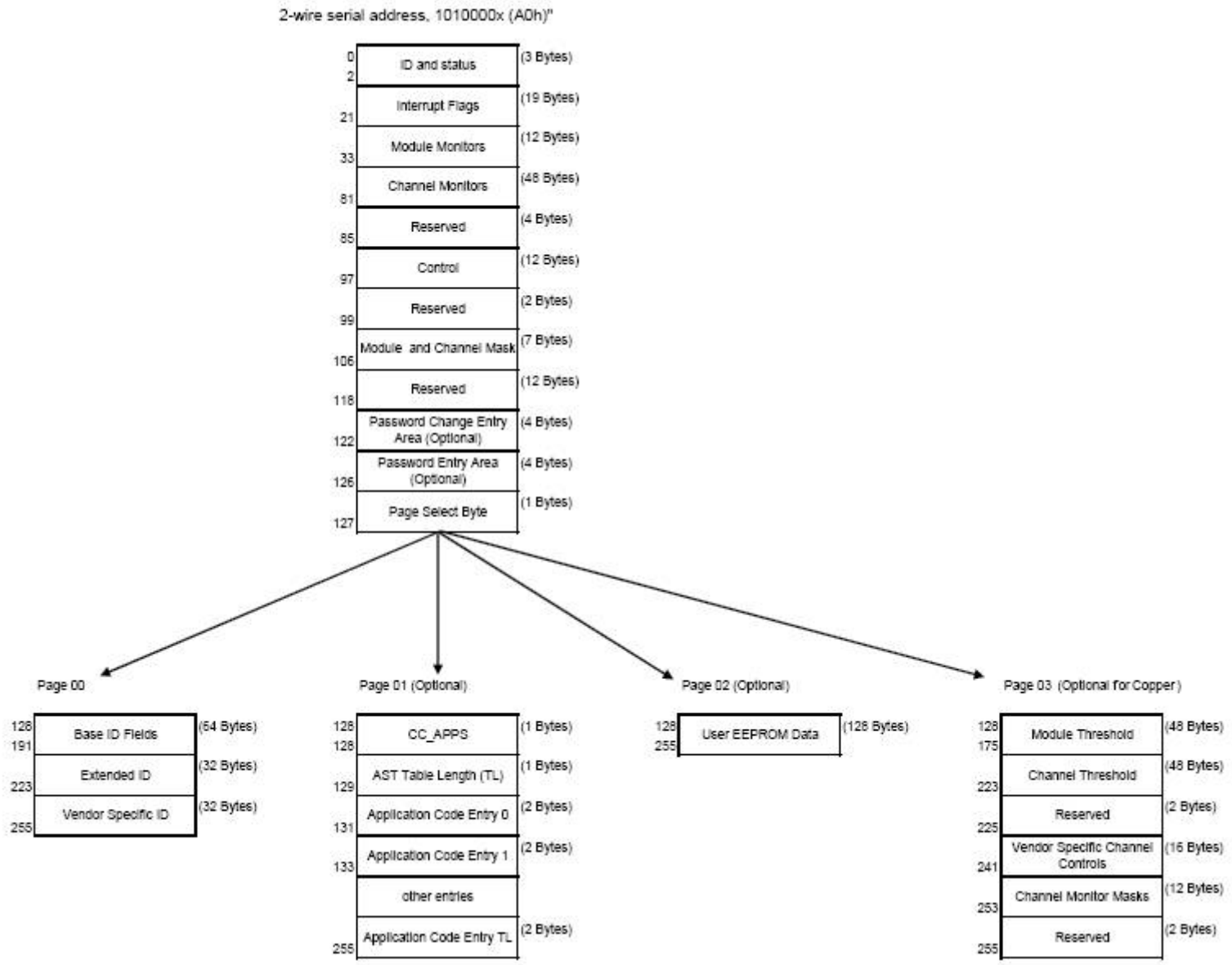



**Figure 29 – QSFP+ Memory Map**

In order to allow access to multiple QSFP+ Modules on the same 2-wire serial interface, the QSFP+ pinout includes a ModSelL pin which allows the host to select the respective Module for interaction. See Clause 3.1.1.1 for details on ModSelL and Clause 3.1.2 for details of the 2-Wire serial interface.
Note: Unless specifically noted, all informative ID fields must be filled out. Using a value of 0 to indicate a field is unspecified (as is common in the SFP definition) is not permitted. Reserved memory locations are to be filled with logic zeros in all bit locations for reserved bytes, and in reserved bit locations for partially specified byte locations as described in this clause.

**APPLICABLE DOCUMENTS**
Digital Diagnostic Monitoring Interface for Optical Modules SFF document number: SFF-8472, rev. 9.5 June 1, 2004.

### 7.6.1 Lower Memory Map

The lower 128 bytes of the 2-wire serial bus address space, see Table 17, is used to access a variety of measurements and diagnostic functions, a set of control functions, and a means to select which of the various upper memory map pages are accessed on subsequent reads. This portion of the address space is always directly addressable and thus is chosen for monitoring and control functions that may need to be repeatedly accessed. The definition of Identifier field is the same as page 00h Byte 128.

**Table 17 – Lower Memory Map**

| Byte Address | Description | Type |
|---|---|---|
| 0 | Identifier (1 Byte) | Read-Only |
| 1-2 | Status (2 Bytes) | Read-Only |
| 3-21 | Interrupt Flags (19 Bytes) | Read-Only |
| 22-33 | Module Monitors (12 Bytes) | Read-Only |
| 34-81 | Channel Monitors (48 Bytes) | Read-Only |
| 82-85 | Reserved (4 Bytes) | Read-Only |
| 86-97 | Control (12 Bytes) | Read/Write |
| 98-99 | Reserved (2 Bytes) | Read/Write |
| 100-106 | Module and Channel Masks (7 Bytes) | Read/Write |
| 107-118 | Reserved (12 Bytes) | Read/Write |
| 119-122 | Password Change Entry Area (optional) (4 Bytes) | Read/Write |
| 123-126 | Password Entry Area (optional) 4 Bytes | Read/Write |
| 127 | Page Select Byte | Read/Write |

#### 7.6.1.1 Status Indicator Bits

The Status Indicators are defined in Table 18.

**Table 18 – Status Indicators**

| Byte | Bit | Name | Description |
|---|---|---|---|
| 1 | All | Reserved | |
| 2 | 7 | Reserved | |
| | 6 | Reserved | |
| | 5 | Reserved | |
| | 4 | Reserved | |
| | 3 | Reserved | |
| | 2 | Flat_mem | Upper memory flat or paged. Flat memory: 0= paging, 1= page 0 only |
| | 1 | IntL | Digital state of the IntL Interrupt output pin |
| | 0 | Data_Not_Ready | Indicates Module has not yet achieved power up and monitor data is not ready. Bit remains high until data is ready to be read at which time the device sets the bit low. |

The Data_Not_Ready bit is high during module power up and prior to a valid suite of monitor readings. Once all monitor readings are valid, the bit is set low until the device is powered down.

#### 7.6.1.2 Interrupt Flags

A portion of the memory map (Bytes 3 through 21), form a flag field. Within this field, the status of LOS and Tx Fault as well as alarms and warnings for the various monitored items is reported. For normal operation and default state, the bits in this field have the value of 0b. For the defined conditions of LOS, Tx Fault, module and channel alarms and warnings, the appropriate bit or bits are set, value = 1b. Once asserted, the bits remained set (latched) until cleared by a read operation that includes the affected bit or reset by the ResetL pin. The Channel Status Interrupt Flags are defined in Table 19.

**Table 19 – Channel Status Interrupt Flags**

| Byte | Bit | Name | Description |
|---|---|---|---|
| 3 | 7 | L-Tx4 LOS | Latched TX LOS indicator, channel 4 (Optional) |
| | 6 | L-Tx3 LOS | Latched TX LOS indicator, channel 3 (Optional) |
| | 5 | L-Tx2 LOS | Latched TX LOS indicator, channel 2 (Optional) |
| | 4 | L-Tx1 LOS | Latched TX LOS indicator, channel 1 (Optional) |
| | 3 | L-Rx4 LOS | Latched RX LOS indicator, channel 4 |
| | 2 | L-Rx3 LOS | Latched RX LOS indicator, channel 3 |
| | 1 | L-Rx2 LOS | Latched RX LOS indicator, channel 2 |
| | 0 | L-Rx1 LOS | Latched RX LOS indicator, channel 1 |
| 4 | 7-4 | Reserved | |
| | 3 | L-Tx4 Fault | Latched TX fault indicator, channel 4 |
| | 2 | L-Tx3 Fault | Latched TX fault indicator, channel 3 |
| | 1 | L-Tx2 Fault | Latched TX fault indicator, channel 2 |
| | 0 | L-Tx1 Fault | Latched TX fault indicator, channel 1 |
| 5 | All | Reserved | |

The Module Monitor Interrupt Flags are defined in Table 20.

**Table 20 – Module Monitor Interrupt Flags**

| Byte | Bit | Name | Description |
|---|---|---|---|
| 6 | 7 | L-Temp High Alarm | Latched high temperature alarm |
| | 6 | L-Temp Low Alarm | Latched low temperature alarm |
| | 5 | L-Temp High Warning | Latched high temperature warning |
| | 4 | L-Temp Low Warning | Latched low temperature warning |
| | 3-0 | Reserved | |
| 7 | 7 | L-Vcc High Alarm | Latched high supply voltage alarm |
| | 6 | L-Vcc Low Alarm | Latched low supply voltage alarm |
| | 5 | L-Vcc High Warning | Latched high supply voltage warning |
| | 4 | L-Vcc Low Warning | Latched low supply voltage warning |
| | 3-0 | Reserved | |
| 8 | All | Rerserved | |

The Channel Monitor Interrupt Flags are defined in Table 21.

**Table 21 – Channel Monitor Interrupt Flags**

| Byte | Bit | Name | Description |
|---|---|---|---|
| 9 | 7 | L-Rx1 Power High Alarm | Latched high RX power alarm, channel 1 |
| | 6 | L-Rx1 Power Low Alarm | Latched low RX power alarm, channel 1 |
| | 5 | L-Rx1 Power High Warning | Latched high RX power warning, channel 1 |
| | 4 | L-Rx1 Power Low Warning | Latched low RX power warning, channel 1 |
| | 3 | L-Rx2 Power High Alarm | Latched high RX power alarm, channel 2 |
| | 2 | L-Rx2 Power Low Alarm | Latched low RX power alarm, channel 2 |
| | 1 | L-Rx2 Power High | Latched high RX power warning, channel |

| | | | |
|---|---|---|---|
| | | Warning | 2 |
| | 0 | L-Rx2 Power Low Warning | Latched low RX power warning, channel 2 |
| 10 | 7 | L-Rx3 Power High Alarm | Latched high RX power alarm, channel 3 |
| | 6 | L-Rx3 Power Low Alarm | Latched low RX power alarm, channel 3 |
| | 5 | L-Rx3 Power High Warning | Latched high RX power warning, channel 3 |
| | 4 | L-Rx3 Power Low Warning | Latched low RX power warning, channel 3 |
| | 3 | L-Rx4 Power High Alarm | Latched high RX power alarm, channel 4 |
| | 2 | L-Rx4 Power low Alarm | Latched low RX power alarm, channel 4 |
| | 1 | L-Rx4 Power high Warning | Latched high RX power warning, channel 4 |
| | 0 | L-Rx4 Power low warning | Latched low RX power warning, channel 4 |
| 11 | 7 | L-Tx1 Bias High Alarm | Latched high TX bias alarm, channel 1 |
| | 6 | L-Tx1 Bias Low Alarm | Latched low TX bias alarm, channel 1 |
| | 5 | L-Tx1 Bias high Warning | Latched high TX bias warning, channel 1 |
| | 4 | L-Tx1 Bias Low Warning | Latched low TX bias warning, channel 1 |
| | 3 | L-Tx2 Bias High Alarm | Latched high TX bias alarm, channel 2 |
| | 2 | L-Tx2 Bias Low Alarm | Latched low TX bias alarm, channel 2 |
| | 1 | L-Tx2 Bias High Warning | Latched High TX bias warning, channel 2 |
| | 0 | L-Tx2 Bias Low Warning | Latched low TX bias warning, channel 2 |
| 12 | 7 | L-Tx3 Bias High Alarm | Latched high TX bias alarm, channel 3 |
| | 6 | L-Tx3 Bias Low Alarm | Latched low TX bias alarm, channel 3 |
| | 5 | L-Tx3 Bias High Warning | Latched high TX bias warning, channel 3 |
| | 4 | L-Tx3 Bias Low Warning | Latched low TX bias warning, channel 3 |
| | 3 | L-Tx4 Bias High Alarm | Latched high TX bias alarm, channel 4 |
| | 2 | L-Tx4 Bias Low Alarm | Latched low TX bias alarm, Channel 4 |
| | 1 | L-Tx4 Bias High Warning | Latched high TX bias warning, channel 4 |
| | 0 | L-Tx4 Bias Low Warning | Latched low TX bias warning, channel 4 |
| 13-14 | All | Reserved | Reserved channel monitor flags, set 3 |
| 15-16 | All | Reserved | Reserved channel monitor flags, set 4 |
| 17-18 | All | Reserved | Reserved channel monitor flags, set 5 |
| 19-20 | All | Reserved | Reserved channel monitor flags, set 6 |
| 21 | All | Reserved | |

**7.6.1.3 Module Monitors**

Real time monitoring for the QSFP+ module include Module temperature, Module supply voltage, and monitoring for each transmit and receive channel. Channel monitoring functions are described in Clause 6.6.1.4.

Measured parameters are reported in 16-bit data fields, i.e., two concatenated bytes. These are shown in Table 22. The 16 bit-data fields allow for wide dynamic range. This is not

intended to imply that a 16-bit A/D system is recommended or required in order to achieve the accuracy goals stated below. The width of the data field should not be taken to imply a given level of precision. It is conceivable that the accuracy goals herein can be achieved by a system having less than 16 bits of resolution. It is recommended that any low-order data bits beyond the system's specified accuracy be fixed at zero. Overall system accuracy and precision will be vendor dependent.

To guarantee coherency of the diagnostic monitoring data, the host is required to retrieve any multi-byte fields from the diagnostic monitoring data structure by the use of a single two-byte read sequence across the 2-wire serial interface. The Module is required to insure that any multi-byte fields that are updated with diagnostic monitoring data must have this update done in a fashion that guarantees coherency and consistency of the data. In other words, the update of a multi-byte field by the Module must not occur such that a partially updated multi-byte field can be transferred to the host. Also, the Module shall not update a multi-byte field within the structure during the transfer of that multi-byte field to the host, such that partially updated data would be transferred to the host.

Accuracy requirements specified below shall apply to the operating signal range specified in the relevant standard. The manufacturer's specification should be consulted for more detail on the conditions under which the accuracy requirements are met.

Measurements are calibrated over vendor specified operating temperature and voltage and should be interpreted as defined below. Alarm and warning threshold values should be interpreted in the same manner as real time 16-bit data.

Internally measured Module temperature are represented as a 16-bit signed twos complement value in increments of 1/256 degrees Celsius, yielding a total range of –128C to +128C that is considered valid between –40 and +125C. Temperature accuracy is vendor specific but must be better than ±3 degrees Celsius over specified operating temperature and voltage. Please see vendor specification for details on location of temperature sensor.

Internally measured Module supply voltage are represented as a 16-bit unsigned integer with the voltage defined as the full 16 bit value (0 – 65535) with LSB equal to 100 uVolt, yielding a total measurement range of 0 to +6.55 Volts. Practical considerations to be defined by Module manufacturer will tend to limit the actual bounds of the supply voltage measurement. Accuracy is vendor specific but must be better than ±3% of the manufacturer's nominal value over specified operating temperature and voltage.

**Table 22 – Module Monitoring Values**

| Byte | Bit | Name | Description |
|---|---|---|---|
| 22 | All | Temperature MSB | Internally measured module temperature |
| 23 | All | Temperature LSB | |
| 24-25 | All | Reserved | |
| 26 | All | Supply Voltage MSB | Internally measured module supply voltage |
| 27 | All | Supply Voltage LSB | |
| 28-33 | All | Reserved | |

### 7.6.1.4 Channel Monitoring

Real time channel monitoring is for each transmit and receive channel and includes optical input power and Tx bias current. Module monitoring functions are described in Clause 6.6.1.3. Measurements are calibrated over vendor specified operating temperature and voltage and should be interpreted as defined below. Alarm and warning threshold values should be interpreted in the same manner as real time 16-bit data. Table 23 defines the Channel Monitoring.

Measured TX bias current is in mA and are represented as a 16-bit unsigned integer with the current defined as the full 16 bit value (0 – 65535) with LSB equal to 2 uA, yielding a total measurement range of 0 to 131 mA. Accuracy is vendor specific but must be better than ±10% of the manufacturer's nominal value over specified operating temperature and voltage.

Measured RX received optical power is in mW and can represent either average received power or OMA depending upon how bit 3 of byte 220 (upper memory page 00h) is set. Represented as a 16 bit unsigned integer with the power defined as the full 16 bit value (0 – 65535) with LSB equal to 0.1 uW, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm). Absolute accuracy is dependent upon the exact optical wavelength. For the vendor specified wavelength, accuracy shall be better than ±3 dB over specified temperature and voltage. This accuracy shall be maintained for input power levels up to the lesser of maximum transmitted or maximum received optical power per the appropriate standard. It shall be maintained down to the minimum transmitted power minus cable plant loss (insertion loss or passive loss) per the appropriate standard. Absolute accuracy beyond this minimum required received input optical power range is vendor specific.

**Table 23 – Channel Monitoring Values**

| Byte | Bit | Name | Description |
|---|---|---|---|
| 34 | All | Rx1 Power MSB | Internally measured RX input power, channel 1 |
| 35 | All | Rx1 Power LSB | |
| 36 | All | Rx2 Power MSB | Internally measured RX input power, channel 2 |
| 37 | All | Rx2 Power LSB | |
| 38 | All | Rx3 Power MSB | Internally measured RX input power, channel 3 |
| 39 | All | Rx3 Power LSB | |
| 40 | All | Rx4 Power MSB | Internally measured RX input power, channel 4 |
| 41 | All | Rx4 Power LSB | |
| 42 | All | Tx1 Bias MSB | Internally measured TX bias, channel 1 |
| 43 | All | Tx1 Bias LSB | |
| 44 | All | Tx2 Bias MSB | Internally measured TX bias, channel 2 |
| 45 | All | Tx2 Bias LSB | |
| 46 | All | Tx3 Bias MSB | Internally measured TX bias, channel 3 |
| 47 | All | Tx3 Bias LSB | |
| 48 | All | Tx4 Bias MSB | Internally measured TX bias, channel 4 |
| 49 | All | Tx4 Bias LSB | |
| 50-57 | | | Reserved channel monitor set 3 |
| 58-65 | | | Reserved channel monitor set 4 |
| 66-73 | | | Reserved channel monitor set 5 |
| 74-81 | | | Reserved channel monitor set 6 |

#### 7.6.1.5 Control Bytes

Control Bytes are defined in Table 24.

**Table 24 – Control Bytes**

| Byte | Bit | Name | Description |
|---|---|---|---|
| 86 | 7-4 | Reserved | |
| | 3 | Tx4 Disable | Read/Write bit that allows software disable of transmitters[1] |
| | 2 | Tx3 Disable | Read/Write bit that allows software disable of transmitters[1] |
| | 1 | Tx2 Disable | Read/Write bit that allows software disable of transmitters[1] |
| | 0 | Tx1 Disable | Read/Write bit that allows software disable of transmitters[1] |
| 87 | 7 | Rx4_Rate_select | Software rate select. Rx Channel 4 MSB (optional) |
| | 6 | Rx4_Rate_select | Software rate select. Rx Channel 4 LSB (optional) |
| | 5 | Rx3_Rate_select | Software rate select. Rx Channel 3 MSB (optional) |
| | 4 | Rx3_Rate_select | Software rate select. Rx Channel 3 LSB (optional) |
| | 3 | Rx2_Rate_select | Software rate select. Rx Channel 2 MSB (optional) |
| | 2 | Rx2_Rate_select | Software rate select. Rx Channel 2 LSB (optional) |
| | 1 | Rx1_Rate_select | Software rate select. Rx Channel 1 MSB (optional) |
| | 0 | Rx1_Rate_select | Software rate select. Rx Channel 1 LSB (optional) |
| 88 | 7 | Tx4_Rate_select | Software rate select. Rx Channel 4 MSB (optional) |
| | 6 | Tx4_Rate_select | Software rate select. Rx Channel 4 LSB (optional) |
| | 5 | Tx3_Rate_select | Software rate select. Rx Channel 3 MSB (optional) |
| | 4 | Tx3_Rate_select | Software rate select. Rx Channel 3 LSB (optional) |
| | 3 | Tx2_Rate_select | Software rate select. Rx Channel 2 MSB (optional) |
| | 2 | Tx2_Rate_select | Software rate select. Rx Channel 2 LSB (optional) |
| | 1 | Tx1_Rate_select | Software rate select. Rx Channel 1 MSB (optional) |
| | 0 | Tx1_Rate_select | Software rate select. Rx Channel 1 LSB (optional) |
| 89 | All | Rx4_Application_Select | Software Application Select per SFF-8078, Rx Channel 4 (optional) |
| 90 | All | Rx3_Application_Select | Software Application Select per SFF-8078, Rx Channel 3 (optional) |
| 91 | All | Rx2_Application_Select | Software Application Select per SFF-8078, Rx Channel 2 (optional) |
| 92 | All | Rx1_Application_Select | Software Application Select per SFF-8078, Rx Channel 1 (optional) |
| 93 | 2-7 | Reserved | |
| 93 | 1 | Power set | Power set to Low Power Mode Default 0 |
| 93 | 0 | Power override | Override of LP mode signal setting the power mode with software |
| 94 | All | Tx4_Application_Select | Software application per SFF-8079, Tx Channel 4 (optional) |
| 95 | All | Tx3_Application_Select | Software application per SFF-8079, Tx Channel 3 (optional) |
| 96 | All | Tx2_Application_Select | Software application per SFF-8079, Tx Channel 2 (optional) |
| 97 | All | Tx1_Application_Select | Software application per SFF-8079, Tx Channel 1 (optional) |
| 98-99 | All | Reserved | |

1 Writing "1" disables the laser of the channel

If software Rate Select is not implemented, the Module ignores the value of Rate Select bits. The registers read all “0”s upon power-up.

#### 7.6.1.6 Module and Channel Masks

The host system may control which flags result in an interrupt (IntL) by setting high individual bits from a set of masking bits in bytes 100-104 for module flags, and bytes 242-253 of page 03h for channel flags. These are described in Table 25 and Table 48. A 1 value in a masking bit prevents the assertion of the hardware IntL pin by the corresponding latched flag bit. Masking bits are volatile and startup with all unmasked (masking bits 0). The mask bits may be used to prevent continued interruption from on-going conditions, which would otherwise continually reassert the hardware IntL pin.

**Table 25 – IntL Masking Bits for Module and Channel Status Interrupts**

| Byte | Bit | Name | Description |
|---|---|---|---|
| 100 | 7 | M-Tx4 LOS | Masking bit for TX LOS indicator, channel 4 (optional) |
| | 6 | M-Tx3 LOS | Masking bit for TX LOS indicator, channel 3 (optional) |
| | 5 | M-Tx2 LOS | Masking bit for TX LOS indicator, channel 2 (optional) |
| | 4 | M-Tx1 LOS | Masking bit for TX LOS indicator, channel 1 (optional) |
| | 3 | M-Rx4 LOS | Masking bit for RX LOS indicator, channel 4 |
| | 2 | M-Rx3 LOS | Masking bit for RX LOS indicator, channel 3 |
| | 1 | M-Rx2 LOS | Masking bit for RX LOS indicator, channel 2 |
| | 0 | M-Rx1 LOS | Masking bit for RX LOS indicator, channel 1 |
| 101 | 7-4 | Reserved | |
| | 3 | M-Tx4 Fault | Masking bit for TX fault indicator, channel 4 |
| | 2 | M-Tx3 Fault | Masking bit for TX fault indicator, channel 3 |
| | 1 | M-Tx2 Fault | Masking bit for TX fault indicator, channel 2 |
| | 0 | M-Tx1 Fault | Masking bit for TX fault indicator, channel 1 |
| 102 | All | Reserved | |
| 103 | 7 | M-Temp High Alarm | Masking bit for high Temperature alarm |
| | 6 | M-Temp Low Alarm | Masking bit for low Temperature alarm |
| | 5 | M- Temp High Warning | Masking bit for high Temperature warning |
| | 4 | M-Temp Low Warning | Masking bit for low Temperature warning |
| | 3-0 | Reserved | |
| 104 | 7 | M-Vcc High alarm | Masking bit for high Vcc alarm |
| | 6 | M-Vcc Low alarm | Masking bit for low Vcc alarm |
| | 5 | M-Vcc High Warning | Masking bit for high Vcc warning |
| | 4 | M-Vcc Low Warning | Masking bit for low Vcc warning |
| | 3-0 | Reserved | |
| 105-106 | All | Reserved | |

#### 7.6.1.7 Rate Select

Rate Select is an optional control used to limit the receiver bandwidth for compatibility with multiple data rates (most likely Fibre Channel). In addition, rate selection allows the transmitter to be fine tuned for specific data rate transmissions.
The Module may:

a) Provide no support for rate selection
b) Rate selection using extended rate select
c) Rate selection with application select tables

**7.6.1.7.1 No Rate Selection Support**

When no rate selection is supported, (page 00h, byte 221, bits 2 and 3) have a value of 0 and Options (page 00h, byte 195, bit 5) have a value of 0. Lack of implementation does not indicate lack of simultaneous compliance with multiple standard rates. Compliance with particular standards should be determined from Module Values (See Table 33).

**7.6.1.7.2 Extended Rate Selection**

When (page 00h, byte 221, bits 2 and 3) have the values of 0 and 1 respectively and at least one of the bits in the Extended Rate Compliance byte (page 00h, byte 141) have a value of one, the module supports extended rate select. Extended rate selection has reserved two bits per channel in the Rxn_Rate_Select and two bits per channel in the Txn_Rate_Select to denote up to four rates. Table 26 defines the functionality when bit 0 of byte 141 is 1. All other values of Extended Rate Compliance byte are reserved.

**Table 26 – Functionality of xN_Rate_Select with Extended Rate selection**

| xN_Rate_Select msb Value | xN-Rate_Select Isb Value | Description |
|---|---|---|
| 0 | 0 | Optimized for data rates less than 2.2Gb/s |
| 0 | 1 | Optimized for data rates from 2.2 up to 6.6 Gb/s |
| 1 | 0 | Optimized for 6.6 Gb/s data rates and above |
| 1 | 1 | Reserved |

**7.6.1.7.3 Rate Selection Using Application Select Tables**

Application Select maximizes compatibility with SFF-8079 Part 2 for Modules that are SFF-8472 compliant.
When the Rate Select declaration bits (page 00h, byte 221, bits 2 and 3) have the values of 1 and 0 respectively, the Application Select method defined in Page 01h is used (see Clause 6.6.3).
The host reads the entire application select table on page 01h to determine the capabilities of the Module. The host controls each channel separately by writing a Control Mode and Table Select (TS) byte to bytes 89-92 and bytes 94-97. The bits of the Rx_Application Select and the Tx_Application Select registers are defined in Table 27.

**Table 27--Definition of Application Select (Bytes 89 to 92 and Bytes 94 to 97))**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Control Mode | | Table Select TS | | | | | |

Control Mode defines the application control mode. Table Select selects module behavior from the AST among 63 possibilities (000000 to 111110). Note that (111111) is invalid.

**Table 28 – Detailed Description of Control Mode**

| Bit 7 | Bit 6 | Function | Address 87, 88 Control | Table Select Control |
|---|---|---|---|---|
| 0 | 0 | Extended rate selection | LSB and MSB are used according to declaration bits. | Ignored |
| 1 | Don't care | Application select | Ignored | field points to application |

Note: Default values for control mode is 0,0 and is volatile memory.

**7.6.1.8 Password Entry and change**

Bytes 119-126 are reserved for an optional password entry function. The Password entry bytes are write only and will be retained until power down, reset, or rewritten by host. This function may be used to control read/write access to vendor specific page 02h. Additionally, module vendors may use this function to implement write protection of Serial ID and other QSFP+ read only information. Passwords may be supplied to and used by Host manufacturers to limit write access in the User EEPROM Page 02h.

Password access shall not be required to access QSFP+ defined data in the lower memory page 00h or in upper pages 00h, 02h and 03h. Note that multiple module manufacturer passwords may be defined to allow selective access to read or write to various sections of memory as allowed above.

Host manufacturer and module manufacturer passwords shall be distinguished by the high order bit (bit 7, byte 123). All host manufacturer passwords shall fall in the range of 00000000h to 7FFFFFFFh, and all module manufacturer passwords in the range of 80000000h to FFFFFFFFh.

Host manufacturer passwords shall be initially set to 00001011h in new modules.

Host manufacturer passwords may be changed by writing a new password in bytes 119-122 when the correct current Host manufacture password has been entered in 123-126, with the high order bit being ignored and forced to a value of 0 in the new password.

The password entry field shall be set to 00000000h on power up and reset.

### 7.6.2 Upper Memory Map Page 00h

Page 00h consists of the Serial ID and is used for read only identification information. The Serial ID is divided into the Base_ID Fields, Extended ID Fields and Vendor Specific ID Fields. The format of the Serial ID Memory Map is shown in Table 29.

**Table 29 – Serial ID: Data Fields**

| Address | Size (Bytes) | Name | Description of Base ID Field |
|---|---|---|---|
| Base ID fields | | | |
| 128 | 1 | Identifier | Identifier Type of serial Module |
| 129 | 1 | Ext. Identifier | Extended Identifier of Serial Module |
| 130 | 1 | Connector | Code for connector type |
| 131-138 | 8 | Module | Code for electronic compatibility or optical compatibility |
| 139 | 1 | Encoding | Code for serial encoding algorithm |
| 140 | 1 | BR, nominal | Nominal bit rate, units of 100 MBits/s |
| 141 | 1 | Extended rateselect Compliance | Tags for extended rate select compliance |
| 142 | 1 | Length(SMF) | Link length supported for SMF fiber in km (note 1) |
| 143 | 1 | Length(OM3 50 um) | Link length supported for EBW 50/125 um fiber (OM3), units of 2m (note 1) |
| 144 | 1 | Length(OM2 50 um) | Link length supported for 50/125 um fiber (OM2), units of 1m (note 1) |
| 145 | 1 | Length(OM1 62.5 um) | Link length supported for 62.5/125 um fiber (OM1), units of 1m (note 1) |
| 146 | 1 | Length(Copper) | Link length supported for copper or active cable, units of 1 m (note 1) |
| 147 | 1 | Device tech | Device technology |
| 148-163 | 16 | Vendor name | QSFP+ vendor name(ASCII) |
| 164 | 1 | Extended Module | Extended Module codes for |

| | | | |
|---|---|---|---|
| | | | InfiniBand |
| 165-167 | 3 | Vendor OUI | QSFP+ vendor IEEE company ID |
| 168-183 | 16 | Vendor PN | Part number provided by QSFP+ vendor(ASCII) |
| 184-185 | 2 | Vendor rev | Revision level for part number provided by vendor(ASCII) |
| 186-187 | 2 | Wave length or Copper cable Attenuation | Nominal laser wavelength (wavelength=value/20 in nm) or copper cable attenuation in dB at 2.5GHz (Adrs 186) and 5.0GHz (Adrs 187) |
| 188-189 | 2 | Wavelength tolerance | Guaranteed range of laser wavelength(+/- value) from nominal wavelength.(wavelength Tol.=value/200 in nm) |
| 190 | 1 | Max case temp. | Maximum case temperature in degrees C |
| 191 | 1 | CC_BASE | Check code for base ID fields (addresses 128-190) |
| Extended ID fields | | | |
| 192-195 | 4 | Options | Rate Select, TX Disable, TX Fault, LOS, Warning indicators for: Temperature, VCC, RX power, TX Bias |
| 196-211 | 16 | Vendor SN | Serial number provided by vendor (ASCII) |
| 212-219 | 8 | Date Code | Vendor's manufacturing date code |
| 220 | 1 | Diagnostic Monitoring Type | Indicates which type of diagnostic monitoring is implemented (if any) in the Module. Bit 1,0 Reserved |
| 221 | 1 | Enhanced Options | Indicates which optional enhanced features are implemented in the Module. |
| 222 | 1 | Reserved | Reserved |
| 223 | 1 | CC_EXT | Check code for the Extended ID Fields (addresses 192-222) |
| Vendor Specific ID Fields | | | |
| 224-255 | 32 | Vendor Specific | Vendor Specific EEPROM |

Note 1: A value of zero means that the Module does not support the specified technology or that the length information must be determined from the Module technology

**7.6.2.1 Identifier (Address 128)**

The identifier value specifies the physical device described by the serial information. This value shall be included in the serial data. The defined identifier values are shown in Table 30. The QSFP+ Module shall use the identifier 0Ch.

**Table 30 – Identifier Values (Address 128)**

| Value | Description of Physical device |
|---|---|
| 00h | Unknown or unspecified |
| 01h | GBIC |
| 02h | Module/connector soldered to motherboard |
| 03h | SFP |
| 04h | 300 pin XBI |
| 05h | XENPAK |
| 06h | XFP |
| 07h | XFF |
| 08h | XFP-E |
| 09h | XPAK |
| 0Ah | X2 |

| | |
|---|---|
| 0Bh | DWDM-SFP |
| 0Ch | QSFP |
| 0Dh | QSFP+ |
| 0Eh-7Fh | Reserved |
| 80-FFh | Vendor Specific |

#### 7.6.2.2 Extended Identifier (Address 129)

The extended identifier provides additional information about the basic Module types such as whether the Module contains a CDR function and identifies the power consumption class it belongs to.

**Table 31 – Extended Identifier Values (Address 129)**

| Bit | Description of Device Type |
|---|---|
| 7-6 | 00: Power Class 1 Module (1.5W max. Power consumption) |
| | 01: Power Class 2 Module (2.0W max. Power consumption) |
| | 10: Power Class 3 Module (2.5W max. Power consumption) |
| | 11: Power Class 4 Module (3.5W max. Power consumption) |
| 5 | Reserved |
| 4 | 0: No CLEI code present in Page 02h |
| | 1: CLEI code present in Page 02h |
| 3 | 0: No CDR in TX , 1: CDR present in TX |
| 2 | 0: No CDR in RX , 1: CDR present in RX |
| 1-0 | Reserved |

#### 7.6.2.3 Connector (Address 130)

The Connector value indicates the external connector provided on the interface. This value shall be included in the serial data. The defined connector values are shown in Table 32. Note that 01h – 0Bh are not QSFP+ compatible, and are included for compatibility with other standards.

**Table 32 – Connector Values (Address 130)**

| Value | Description of Connector |
|---|---|
| 00h | Unknown or unspecified |
| 01h | SC |
| 02h | FC Style 1 copper connector |
| 03h | FC Style 2 copper connector |
| 04h | BNC/TNC |
| 05h | FC coax headers |
| 06h | Fiberjack |
| 07h | LC |
| 08h | MT-RJ |
| 09h | MU |
| 0Ah | SG |
| 0Bh | Optical Pigtail |
| 0Ch | MPO |
| 0D-1Fh | Reserved |
| 20h | HSSDC II |
| 21h | Copper pigtail |
| 22h | RJ45 |
| 23h | No separable connector |
| | |
| 24h-7Fh | Reserved |
| | |
| 80-FFh | Vendor specific |

#### 7.6.2.4 Module (Address 131-138)

The following bit significant indicators define the electronic or optical interfaces that are supported by the QSFP+ Module. At least one bit shall be set in this field. For Fibre Channel

QSFP+s, the Fibre Channel speed, transmission media, transmitter technology, and distance capability shall all be indicated.

**Table 33 – Module Values (Address 131-138)**

| Address | Bit | Description of Module data |
|---|---|---|
| 10/40G Ethernet Compliance Code | | |
| 131 | 7 | Reserved |
| 131 | 6 | 10GBase-LRM |
| 131 | 5 | 10GBase-LR |
| 131 | 4 | 10GBase-SR |
| 131 | 3 | 40G-Active Cable |
| 131 | 2 | 40GBase-CR4 |
| 131 | 1 | 40GBase-SR4 |
| 131 | 0 | Reserved |
| SONET Compliance codes | | |
| 132 | 7-4 | Reserved |
| 132 | 3 | Reserved |
| 132 | 2 | OC 48, long reach |
| 132 | 1 | OC 48, intermediate reach |
| 132 | 0 | OC 48 short reach |
| SAS/SATA compliance codes | | |
| 133 | 7- | Reserved |
| 133 | 6 | SAS/SATA 6.0G |
| 133 | 5 | SAS/SATA 3.0G |
| 133 | 4 | SATA 1.5G |
| Gigabit Ethernet Compliant codes | | |
| 134 | 3 | 1000Base-T |
| 134 | 2 | 1000Base-CX |
| 134 | 1 | 1000Base-LX |
| 134 | 0 | 1000Base-SX |
| Fibre Channel link length | | |
| 135 | 7 | Very long distance (V) |
| 135 | 6 | Short distance (S) |
| 135 | 5 | Intermediate distance (I) |
| 135 | 4 | Long distance (L) |
| 135 | 3 | Medium (M) |
| Fibre Channel Transmitter Technology | | |
| 135 | 2 | Reserved |
| 135 | 1 | Longwave laser (LC) |
| 135 | 0 | Electrical inter-enclosure (EL) |
| 136 | 7 | Electrical intra-enclosure |
| 136 | 6 | Shortwave laser w/o OFC (SN) |
| 136 | 5 | Shortwave laser w OFC (SL) |
| 136 | 4 | Longwave Laser (LL) |
| 136 | 0-3 | Reserved |
| Fibre Channel transmission media | | |
| 137 | 7 | Twin Axial Pair (TW) |
| 137 | 6 | Shielded Twisted Pair (TP) |
| 137 | 5 | Miniature Coax (MI) |
| 137 | 4 | Video Coax (TV) |
| 137 | 3 | Multi-mode 62.5m (M6) |
| 137 | 2 | Multi-mode 50m (M5) |
| 137 | 1 | Multi-mode 50um (OM3) |
| 137 | 0 | Single Mode (SM) |
| Fibre Channel Speed | | |
| 138 | 7 | 1200 Mbytes/Sec |
| 138 | 6 | 800 Mbytes/Sec |
| 138 | 5 | 1600 Mbytes/Sec |
| 138 | 4 | 400 Mbytes/Sec |
| 138 | 3 | |
| 138 | 2 | 200 Mbytes/Sec |
| 138 | 1 | Reserved |

| | | |
|---|---|---|
| 138 | 0 | 100 Mbytes/Sec |

**7.6.2.5 Encoding (Address 139)**

The encoding value indicates the serial encoding mechanism that is the nominal design target of the particular QSFP+ Module. The value shall be contained in the serial data. The defined encoding values are shown in Table 34.

**Table 34 – Encoding Values (Address 139)**

| Code | Description of encoding mechanism |
|---|---|
| 00h | Unspecified |
| 01h | 8B10B |
| 02h | 4B5B |
| 03h | NRZ |
| 04h | SONET Scrambled |
| 05h | 64B66B |
| 06h | Manchester |
| 07h-FFh | Reserved |

**6.6.2.6 BR, nominal (Address 140)**

The nominal bit rate (BR, nominal) is specified in units of 100 Megabits per second, rounded off to the nearest 100 Megabits per second. The bit rate includes those bits necessary to encode and delimit the signal as well as those bits carrying data information. A value of 0 indicates that the bit rate is not specified and must be determined from the Module technology. The actual information transfer rate will depend on the encoding of the data, as defined by the encoding value.

**7.6.2.7 Extended RateSelect Compliance (Address 141)**

The Extended RateSelect Compliance field is used to allow a single QSFP+ Module the flexibility to comply with single or multiple Extended RateSelect definitions. A definition is indicated by presence of a "1" in the specified bit tag position. If exclusive, non-overlapping bit tag definitions are used, Page 00h, byte 141 will allow compliance to 8 (1-8) distinct multi-rate definitions.

**Table 35 – Extended RateSelect Compliance Tag Assignment (Address 141)**

| Address | Bits | Description |
|---|---|---|
| 141 | 7-1 | Reserved |
| 141 | 0 | QSFP+ Rate Select Version 1. This functionality is different from SFF-8472 and SFF-8431. |

Note: Further details of the use of this field can be found in Clause 7.6.1.7.

**7.6.2.8 Length (Standard SM Fiber)-km (Address 142)**

Addition to EEPROM data from original GBIC definition. This value specifies the link length that is supported by the QSFP+ Module while operating in compliance with the applicable standards using single mode fiber. Supported link length is as specified in the SFF 8074i standard. The value is in units of kilometers. A value of zero means that the Module does not support single mode fiber or that the length information must be determined from the Module technology.

**7.6.2.9 Length (OM3) (Address 143)**

This value specifies the link length that is supported by the QSFP+ Module while operating in compliance with the applicable standards using 2000 MHZ*km (850 nm) extended bandwidth 50 micron core multimode fiber. The value is in units of 2 meters. A value of zero means that the Module does not support OM3 fiber or that the length information must be determined from the Module technology.

**7.6.2.10 Length (OM2) (Address 144)**

This value specifies the link length that is supported by the QSFP+ Module while operating in compliance with the applicable standards using 500 MHz*Km (850 nm and 1310 nm) 50 micron multi-mode fiber. The value is in units of 1 meter. A value of zero means that the Module does not support OM2 fiber or that the length information must be determined from the Module technology.

**7.6.2.11 Length (OM1) (Address 145)**
This value specifies the link length that is supported by the QSFP+ Module while operating in compliance with the applicable standards using 200 MHz*Km (850 nm) and 500 MHz*Km (1310 nm) 62.5 micron multi-mode fiber. The value is in units of 1 meter. A value of zero means that the Module does not support OM1 fiber or that the length information must be determined from the Module technology.

**7.6.2.12 Length (Copper) (Address 146)**
This value specifies the minimum link length that is supported by the QSFP+ Module while operating in compliance with the applicable standards using copper cable. The value is in units of 1 meter. Supported link length is as specified in the SFF 8074i standard. A value of zero means that the Module does not support Copper or that the length information must be determined from the Module technology. Further information about the cable design, equalization, and connectors is usually required to guarantee meeting a particular length requirement.

**7.6.2.13 Device Tech (Address 147)**
The technology used in the device is described in Table 36 and Table 37. The top 4 bits of the Device Tech byte describe the device technology used. The lower four bits (bits 7-4) of the Device Tech byte are used to describe the transmitter technology.

**Table 36 – Description of Device Technology (Address 147)**

| Bits | Description of Physical device |
|---|---|
| 7-4 | Transmitter technology |
| 3 | 0: No wavelength control<br>1: Active wavelength control |
| 2 | 0: Uncooled transmitter device<br>1: Cooled transmitter |
| 1 | 0: Pin detector<br>1: APD detector |
| 0 | 0: Transmitter not tuneable<br>1: Transmitter tuneable |

**Table 37 – Transmitter Technology (Address 147 bits 7-4)**

| Value | Description of physical device |
|---|---|
| 0000b | 850 nmVCSEL |
| 0001b | 1310 nmVCSEL |
| 0010b | 1550 nm VCSEL |
| 0011b | 1310 nm FP |
| 0100b | 1310 nm DFB |
| 0101b | 1550 nm DFB |
| 0110b | 1310 nm EML |
| 0111b | 1550 nm EML |
| 1000b | Copper or others |
| 1001b | 1490 nm DFB |
| 1010b | Copper cable unequalized |
| 1011b | Copper cable passive equalized |
| 1100b | Copper cable, near and far end equalizers |
| 1101b | Copper cable, far end equalizers |
| 1110b | Copper cables, near end equalizer |
| 1111b | Reserved |

**7.6.2.14 Vendor Name (Address 148-163)**
The vendor name is a 16 character field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h). The vendor name shall be the full name of the corporation, a commonly accepted abbreviation of the name of the corporation, the SCSI company code for the corporation, or the stock exchange code for the corporation. At least one of the vendor name or the vendor OUI fields shall contain valid serial data.

**7.6.2.15 Extended Module Codes (Address 164)**
The Extended Module Codes define the electronic or optical interfaces for InfiniBand that are supported by the QSFP+ Module as shown in Table 38.

**Table 38 – Extended Module Code Values (Address 164)**

| Address | Bit | Description of Module Data |
|---|---|---|
| Infiniband Compliance codes | | |
| 164 | 7-4 | Reserved |
| 164 | 3 | EDR Speed (20 Gb/s) |
| 164 | 2 | QDR Speed (10 Gb/s) |
| 164 | 1 | DDR Speed (5.0 Gb/s) |
| 164 | 0 | SDR Speed (2.5 Gbps) |

**7.6.2.16 Vendor OUI (Address 165-167)**

The vendor organizationally unique identifier field (vendor OUI) is a 3-byte field that contains the IEEE Company Identifier for the vendor. A value of all zero in the 3-byte field indicates that the Vendor OUI is unspecified.

**7.6.2.17 Vendor PN (Address 168-183)**

The vendor part number (vendor PN) is a 16-byte field that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor part number or product name. A value of all zero in the 16-byte field indicates that the vendor PN is unspecified.

**7.6.2.18 Vendor Rev (Address 184-185)**

The vendor revision number (vendor rev) is a 2-byte field that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor's product revision number. A value of all zero in the field indicates that the vendor Rev is unspecified.

**7.6.2.19 Wavelength (Address 186-187)**

Nominal transmitter output wavelength at room temperature. 16 bit hex value with byte 186 as high order byte and byte 187 as low order byte. The laser wavelength is equal to the 16 bit integer value divided by 20 in nm (units of 0.05nm). This resolution should be adequate to cover all relevant wavelengths yet provide enough resolution for all expected DWDM applications. For accurate representation of controlled wavelength applications, this value should represent the center of the guaranteed wavelength range.

If the cable is identified as copper these registers will be used to define the cable attenuation. An indication of 0 dB attenuation refers to the case where the attenuation is not known or is unavailable.

Address 186 (00-FFh) is the copper cable attenuation at 2.5GHz in units of 1 dB

Address 187 (00-FFh) is an 8 bit hex value indicating the copper cable attenuation at 5.0GHz in units of 1 dB.

**7.6.2.20 Wavelength Tolerance (Address 188-189)**

The guaranteed +/- range of transmitter output wavelength under all normal operating conditions. 16 bit value with byte 188 as high order byte and byte 189 as low order byte. The laser wavelength is equal to the 16 bit integer value divided by 200 in nm (units of 0.005nm). Thus, the following two examples:

Example 1:

10GBASE-LR Wavelength Range = 1260 to 1355 nm

Nominal Wavelength in bytes 186 - 187 = 1307.5 nm.

Represented as INT(1307.5 nm * 20) = 26150 = 6626h

Wavelength Tolerance in bytes 188 - 189 = 47.5nm.

Represented as INT(47.5 nm * 200) = 9500 = 251Ch

Example 2:

ITU-T Grid Wavelength = 1534.25 nm (195.4 THz) with 0.236 nm ( 30 GHz) Tolerance

Nominal Wavelength in bytes 186 - 187 = 1534.25 nm.

Represented as INT(1534.25nm * 20) = 30685 = 77DDh

Wavelength Tolerance in bytes 188 - 189 = 0.236 nm.

Represented as INT(0.236 nm * 200) = 47 = 002Fh

**7.6.2.21 Max Case Temp (Address 190)**

Allows specification of a maximum case temperature other than the QSFP+ standard of 70C. Maximum case temperature is an 8-bit value in Degrees C.

**7.6.2.22 CC_BASE (Address 191)**

The check code is a one byte code that can be used to verify that the first 63 bytes of serial information in the QSFP+ Module is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 128 to byte 190, inclusive.

**7.6.2.23 Options (Address 192-195)**

The bits in the option field shall specify the options implemented in the QSFP+ Module as described in Table 39.

**Table 39 – Option Values (Address 192-195)**

| Address | Bit | Description of option |
|---|---|---|
| 192 | 7-0 | Reserved |
| 193 | 7-1 | Reserved |
| 193 | 0 | RX output amplitude programming, coded 1 if implemented, else 0. |
| 194 | 7-4 | Reserved |
| 194 | 3 | Rx Squelch Disable implemented, coded 1 if implemented, else 0. |
| 194 | 2 | Rx Output Disable capable: coded 1 if implemented, else 0. |
| 194 | 1 | Tx Squelch Disable implemented: coded 1 if implemented, else 0. |
| 194 | 0 | Tx Squelch implemented: coded 1 if implemented, else 0. |
| 195 | 7 | Memory page 02 provided: coded 1 if implemented, else 0. |
| 195 | 6 | Memory page 01 provided: coded 1 if implemented, else 0. |
| 195 | 5 | RATE_SELECT is implemented. If the bit is set to 1 then active control of the select bits in the upper memory table is required to change rates. If the bit is set to 0, no control of the rate select bits in the upper memory table is required. In all cases, compliance with multiple rate standards should be determined by Module Codes in Bytes 132, 133, 134 and 135 of Page 00h. |
| 195 | 4 | Tx_DISABLE is implemented and disables the serial output. |
| 195 | 3 | Tx_FAULT signal implemented, coded 1 if implemented, else 0 |
| 195 | 2 | Tx Squelch implemented to reduce OMA coded 0, implemented to reduce Pave coded 1. |
| 195 | 1 | Loss of Signal implemented, coded 1 if implemented, else 0 |
| 195 | 0 | Reserved |

**7.6.2.24 Vendor SN (Address 196-211)**

The vendor serial number (vendor SN) is a 16-character field that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor's serial number for the QSFP+ Module. A value of all zero in the 16-byte field indicates that the vendor SN is unspecified.

**7.6.2.25 Date Code (Address 212-219)**

The date code is an 8-byte field that contains the vendor's date code in ASCII characters. The date code is mandatory. The date code shall be in the format specified by Table 40.

**Table 40 – Date Codes (Address 212-219)**

| Address | Description of field |
|---|---|
| 212-213 | ASCII code, two low order digits of year. (00=2000) |
| 214-215 | ASCII code digits of month(01=Jan through 12=Dec |
| 216-217 | ASCII code day of month (01-31) |

| | |
|---|---|
| 218-219 | ASCII code, vendor specific lot code, may be blank |

**7.6.2.26 Diagnostic Monitoring Type (Address 220)**

"Diagnostic Monitoring Type" is a 1-byte field with 8 single bit indicators describing how diagnostic monitoring is implemented in the particular QSFP+ Module. Bit indicators are shown in Table 41.

Digital Diagnostic Monitors monitor received power, bias current, supply voltage and temperature. Additionally, alarm and warning thresholds must be written as specified in this document. Auxiliary monitoring fields are optional extensions to Digital Diagnostics. All digital monitoring values must be internally calibrated and reported in the units defined in this document.

Bit 3 indicates whether the received power measurement represents average input optical power or OMA. If the bit is set, average power is monitored. If not, OMA is monitored.

**Table 41 – Diagnostic Monitoring Type (Address 220)**

| Address | Bits | Description |
|---|---|---|
| 220 | 7-5 | Reserved |
| 220 | 4 | Module Respond to FEC BER. 0=no BER Support. 1=BER Support |
| 220 | 3 | Received power measurements type. 0=OMA 1=Average Power |
| 220 | 2 | Reserved |
| 220 | 1-0 | Reserved |

**7.6.2.27 Enhanced Options (Address 221)**

The format of the Enhanced Options byte are shown in Table 42. The use of the Enhanced Options field is defined in Clause 6.6.1.7. The state where the Rate Select declaration bits both have a value of 1 is reserved and should not be used.

**Table 42 – Enhanced Options (byte 221))**

| Address | Bit | Description |
|---|---|---|
| 221 | 7-4 | Reserved |
| 221 | 3 | Rate Selection Declaration: When this Declaration bit is 0 the module does not support rate selection. When this Declaration bit is 1, rate selection is implemented using extended rate selection. See 6.6.1.7.2 |
| 221 | 2 | Application select table declaration. When this declaration bit is 1, the module supports rate selection using application select table mechanism. When this declaration bit is 0, the module does not support application select and page 01 does not exist |
| 221 | 1-0 | Reserved |

**7.6.2.28 CC_EXT (Address 223)**

The check code is a one-byte code that can be used to verify that the first 32 bytes of extended serial information in the QSFP+ Module is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 192 to byte 222, inclusive.

**7.6.2.29 Vendor Specific (Address 224-255)**

This area may contain vendor specific information, which can be read from the QSFP+ Module. The data is read only. Bytes 224-255 of Page 00h may be used for Vendor Specific ID functions.

**7.6.3 Upper Memory Map Page 01h**

The format of Page 01h is defined in Table 43.

**Table 43 – Application Select Table (Page 01)**

| Byte | Bit Range | Name of Field | Description |
|---|---|---|---|
| 128 | 7-0 | CC_APPS | Check code for the AST: the check code shall be the low order bits |

| | | | |
|---|---|---|---|
| | | | of the sum of the contents of all the bytes from byte 129 to byte 255, inclusive. |
| 129 | 7-6 | Reserved | |
| 129 | 5-0 | AST Table Length, TL | A 6 bit binary number. TL, specifies how many application table entries are defined in bytes 130-255 addresses. TL is valid between 0 (1 entry) and 62 (for a total of 63 entries) |
| 130,131 | 7-0,7-0 | Application Code 0 | Definition of first application supported |
| … | | Other Table Entries | |
| 130+2*TL<br>131+2*TL | 7-0, 7-0 | Application code TL | Definition of last application supported |

**Table 44 – Application Code Structure**

| Low Order Byte | | | | | | | | High order Byte | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | Category | | | | | | Variant | | | | | | | |

### 7.6.4 User Writable and Vendor Specific Memory

Page 02 is optionally provided as user writable EEPROM. The host system may read or write this memory for any purpose. If bit 4 of Page 00 byte 129 is set, however, the first 10 bytes of Table 02h, bytes128-137 will be used to store the CLEI code for the module.

### 7.6.5 Upper Memory Page 03h

The upper memory map page 03h contains module thresholds, channel thresholds and masks, and optional channel controls. These are shown in Table 45 and described in detail in Clause 6.6.1, Clause 6.6.1.6 and Clause 6.6.1.4.

**Table 45 – Upper Memory Map Page 03h**

| Byte Address | Description | Type |
|---|---|---|
| 128-175 | Module Thresholds (48 Bytes) | Read-Only |
| 176-223 | Channel Thresholds (48 Bytes) | Read-Only |
| 224-225 | Reserved (2 Bytes) | Read-Only |
| 226-239 | Vendor Specific Channel Controls (2 Bytes) | Read/Write |
| 240-241 | Optional Channel Controls (2 bytes) | Read/Write |
| 242-253 | Channel Monitor Masks (12 Bytes) | Read/Write |
| 254-255 | Reserved (2 bytes) | Read/Write |

#### 7.6.5.1 Module and Channel Thresholds

Each monitor value has a corresponding high alarm, low alarm, high warning and low warning threshold. These factory-preset values allow the user to determine when a particular value is outside of “normal” limits as determined by the Module manufacturer. It is assumed that these values will vary with different technologies and different implementations. These values are stored in read-only memory in bytes 128-223 of the upper memory page 03h as shown in Table 46.

The values reported in the Alarm and Warning Thresholds area may be typical values at some chosen nominal operating conditions and may be temperature compensated or otherwise adjusted when setting warning and/or alarm flags. Any threshold compensation or adjustment is vendor specific and optional. Refer to the vendor’s data sheet for use of alarm and warning thresholds.

**Table 46 – Module and Channel Thresholds**

| Address | # Bytes | Name | Description |
|---|---|---|---|

| | | | |
|---|---|---|---|
| 128-129 | 2 | Temp High Alarm | MSB at low address |
| 130=131 | 2 | Temp Low Alarm | MSB at low address |
| 132-133 | 2 | Temp High Warning | MSB at low address |
| 134-135 | 2 | Temp Low Warning | MSB at low address |
| 136-143 | 8 | Reserved | |
| 144-145 | 2 | Vcc High Alarm | MSB at low address |
| 146-147 | 2 | Vcc Low Alarm | MSB at low address |
| 148-149 | 2 | Vcc High Warning | MSB at low address |
| 150-151 | 2 | Vcc Low Warning | MSB at low address |
| 152-175 | 24 | Reserved | |
| 176-177 | 2 | RX Power High Alarm | MSB at low address |
| 178-179 | 2 | RX Power Low Alarm | MSB at low address |
| 180-181 | 2 | RX Power High Warning | MSB at low address |
| 182-183 | 2 | RX Power Low Warning | MSB at low address |
| 184-185 | 2 | Tx Bias High Alarm | MSB at low address |
| 186-187 | 2 | Tx Bias Low Alarm | MSB at low address |
| 188-189 | 2 | Tx Bias High Warning | MSB at low address |
| 190-191 | 2 | Tx Bias Low Warning | MSB at low address |
| 192-199 | 8 | Reserved | Reserved thresholds for channel parameter set 3 |
| 200-207 | 8 | Reserved | Reserved thresholds for channel parameter set 4 |
| 208-215 | 8 | Reserved | Reserved thresholds for channel parameter set 5 |
| 216-223 | 8 | Reserved | Reserved thresholds for channel parameter set 6 |

#### 7.6.5.2 Optional Channel Controls

Upper Memory Page Control Bits are defined in Table 47.

**Table 47 – Optional Channel Controls**

| Byte | Bit | Name | Description |
|---|---|---|---|
| 238 | 7-4 | RX1 output amplitude | Output amplitude levels with no equalization enabled |
| | 3-0 | RX2 output amplitude | Output amplitude levels with no equalization enabled |
| 239 | 7-4 | RX3 output amplitude | Output amplitude levels with no equalization enabled |
| | 3-0 | RX4 output amplitude | Output amplitude levels with no equalization enabled |
| 240 | 7 | Rx4 SQ Disable | Rx Squelch Disable Channel 4 (optional) |
| | 6 | Rx3 SQ Disable | Rx Squelch Disable Channel 3 (optional) |
| | 5 | Rx2 SQ Disable | Rx Squelch Disable Channel 2 (optional) |
| | 4 | Rx1 SQ Disable | Rx Squelch Disable Channel 1 (optional) |
| | 3 | Tx4 SQ Disable | Tx Squelch Disable Channel 4 (optional) |
| | 2 | Tx3 SQ Disable | Tx Squelch Disable Channel 3 (optional) |
| | 1 | Tx2 SQ Disable | Tx Squelch Disable Channel 2 (optional) |
| | 0 | Tx1 SQ Disable | Tx Squelch Disable Channel 1 (optional) |
| 241 | 7 | Rx4 Output Disable | Rx Output Disable channel 4 (optional) |
| | 6 | Rx3 Output Disable | Rx Output Disable channel 3 (optional) |
| | 5 | Rx2 Output Disable | Rx Output Disable channel 2 (optional) |
| | 4 | Rx1 Output Disable | Rx Output Disable channel 1 (optional) |
| | 3 | Reserved | |
| | 2 | Reserved | |
| | 1 | Reserved | |
| | 0 | Reserved | |

**Table 48 --- Output amplitude control (address 238-239)**

| Code | Receiver Output Amplitude No Output Equalization | |
|---|---|---|
| | Nominal | Units |
| 1xxx | Reserved | |
| 0111 | Reserved | mV(pk-pk) |
| 0110 | Reserved | mV(pk-pk) |
| 0101 | Reserved | mV(pk-pk) |
| 0100 | Reserved | mV(pk-pk) |
| 0011 | 600-1200 | mV(pk-pk) |
| 0010 | 400-800 | mV(pk-pk) |
| 0001 | 300-600 | mV(pk-pk) |
| 0000 | 200-400 | mV(pk-pk) |

Squelch and output control functionality is optional; if implemented, squelch and output disable is controlled for each channel using bytes 240 and 241 of page 03h. Squelch is normally operational as described in Clause 3.1.3, High Speed Electrical Specification. Writing a “1” in the Squelch Disable register (byte 240, page 03h) disables the squelch for the associated channel. Writing a “1” in the Output Disable register (byte 241, page 03h) squelches the output of the associated channel. When a “1” is written in both registers for a channel, the associated output is disabled. The registers read all “0”s upon power-up.

### 7.6.5.3 Channel Monitor Masks

The Masking Bits for the Channel Monitor Functions are defined in Table 48.

**Table 49 – Channel Monitor Masks**

| Byte | Bit | Name | Descriptioin |
|---|---|---|---|
| 242 | 7 | M-Rx1 Power High Alarm | Masking Bit for high RX Power alarm channel 1 |
| | 6 | M-Rx1 Power Low Alarm | Masking Bit for low RX Power alarm channel 1 |
| | 5 | M-Rx1 Power High Warning | Masking Bit for high RX Power warning channel 1 |
| | 4 | M-Rx1 Power Low Warning | Masking Bit for low RX Power warning channel 1 |
| | 3 | M-Rx2 Power High Alarm | Masking Bit for high RX Power alarm channel 2 |
| | 2 | M-Rx2 Power Low Alarm | Masking Bit for low RX Power alarm channel 2 |
| | 1 | M-Rx2 Power High Warning | Masking Bit for high RX Power warning channel 2 |
| | 0 | M-Rx2 Power Low Warning | Masking Bit for low RX Power warning channel 2 |
| 243 | 7 | M-Rx3 Power High Alarm | Masking Bit for high RX Power alarm channel 3 |
| | 6 | M-Rx3 Power Low Alarm | Masking Bit for low RX Power alarm channel 3 |
| | 5 | M-Rx3 Power High Warning | Masking Bit for high RX Power warning channel 3 |
| | 4 | M-Rx3 Power Low Warning | Masking Bit for low RX Power warning channel 3 |
| | 3 | M-Rx4 Power High Alarm | Masking Bit for high RX Power alarm channel 4 |
| | 2 | M-Rx4 Power Low Alarm | Masking Bit for low RX Power alarm channel 4 |
| | 1 | M-Rx4 Power High Warning | Masking Bit for high RX Power warning channel 4 |
| | 0 | M-Rx4 Power Low Warning | Masking Bit for low RX Power warning channel 4 |
| 244 | 7 | M-Tx1 Bias High Alarm | Masking Bit for high TX Bias alarm channel 1 |
| | 6 | M-Tx1 Bias Low Alarm | Masking Bit for low TX Bias alarm channel 1 |
| | 5 | M-Tx1 Bias High Warning | Masking Bit for high TX Bias warning channel 1 |
| | 4 | M-Tx1 Bias Low Warning | Masking Bit for low TX Bias warning channel 1 |
| | 3 | M-Tx2 Bias High Alarm | Masking Bit for high TX Bias alarm channel 2 |
| | 2 | M-Tx2 Bias Low Alarm | Masking Bit for low TX Bias alarm channel 2 |
| | 1 | M-Tx2 Bias High Warning | Masking Bit for high TX Bias warning channel |

| | | | |
|---|---|---|---|
| | | | 2 |
| | 0 | M-Tx2 Bias Low Warning | Masking Bit for low TX Bias warning channel 2 |
| 245 | 7 | M-Tx3 Bias High Alarm | Masking Bit for high TX Bias alarm channel 3 |
| | 6 | M-Tx3 Bias Low Alarm | Masking Bit for low TX Bias alarm channel 3 |
| | 5 | M-Tx3 Bias High Warning | Masking Bit for high TX Bias warning channel 3 |
| | 4 | M-Tx3 Bias Low Warning | Masking Bit for low TX Bias warning channel 3 |
| | 3 | M-Tx4 Bias High Alarm | Masking Bit for high TX Bias alarm channel 4 |
| | 2 | M-Tx4 Bias Low Alarm | Masking Bit for low TX Bias alarm channel 4 |
| | 1 | M-Tx4 Bias High Warning | Masking Bit for high TX Bias warning channel 4 |
| | 0 | M-Tx4 Bias Low Warning | Masking Bit for low TX Bias warning channel 4 |
| 246-247 | All | Reserved | Reserved channel monitor masks set 3 |
| 248-249 | All | Reserved | Reserved channel monitor masks set 4 |
| 250-251 | All | Reserved | Reserved channel monitor masks set 5 |
| 252-253 | All | Reserved | Reserved channel monitor masks set 6 |