SFF Committee

SFF-8431 Rev 2
Stabilization Ballot

SFF-8431 Abstract
SFF-8431 Chapter 1
SFF-8431 Chapter 2
SFF-8431 Chapter 4

- -

One of the difficulties with a project such as SFF-8431 is the degree of effort needed for new work while lingering issues with 'complete' sections diffuse the focus.

The following note from Tom Lindsay explains his reasons for closing activity on some sections in order to focus on others:

Dal Allan, Ali and I have had several conversations regarding balloting plans for SFF-8431. The topic was discussed during the 8431 SSWG at Broadcom and again in the general XCVR SSWG April 3 in San Diego. We plan to structure the specification for a stabilization ballot on the next revision (2.0).

A) The Abstract and Chapters 1, 2, and 4 are ready for ballot.

a. These sections are reasonably mature, and feedback from the membership is desired sooner rather than later.
b. Fibre Channel is depending on Chapters 2 and 4 of SFF-8431, and so these chapters should proceed independently of the high-speed sections of SFF-8431.
c. Provide membership a view of the status of the project.

B) Chapter 3 is not ready for ballot, nor are the annexes. However, comments on the non-balloted sections are still encouraged.

- -

Stabilization ballots are a way to bring closure to those parts of a specification which are stable, and will no longer consume SSWG attention after comments to this ballot have been addressed.

Members are encouraged to make their comments on the named sections now.

Comments which are received on these sections will be addressed in the next revision.

I Dal Allan
Chairman

SFF Committee

SFF-8431 Specifications for

Enhanced 8.5 and 10 Gigabit Small Form Factor Pluggable Module "SFP+"

Revision 2.0

26 April 2007

Secretariat: SFF Committee

Abstract: This document defines the electrical interface specifications for 8.5 and 10 Gigabit/s Small Form Factor Pluggable (SFP+) modules and hosts. The module is a hot pluggable small footprint serial-to-serial data-agnostic optical transceiver, intended to support datacom applications (8.5 GBd Fibre Channel, 10 Gigabit Ethernet or 10.51 GBd Fibre Channel). The modules may optionally support lower signaling rates as well. The modules may be used to implement single mode or multi-mode serial optical interfaces at 850 nm, 1310 nm, or 1550 nm. The SFP+ module design may use one of several different optical connectors.

This specification provides a common reference for system manufacturers, system integrators, and suppliers. This is an internal working specification of the SFF Committee, an industry ad hoc group.

This specification is made available for public review, and written comments are solicited from readers. Comments received by the members will be considered for inclusion in future revisions of this specification.

Support: This specification is supported by the identified member companies of the SFF Committee.

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EXPRESSION OF SUPPORT BY MANUFACTURERS

The following member companies of the SFF Committee voted in favor of this industry specification:

tbd

The following member companies of the SFF Committee voted against this industry specification:

tbd

The following member companies of the SFF Committee voted to abstain on this industry specification:

tbd

The user's attention is called to the possibility that implementation to this Specification may require use of an invention covered by patent rights. By distribution of this specification, no position is taken with respect to the validity of a claim or claims of any patent rights in connection therewith. Members of the SFF Committee which advise that a patent exists are required to provide a statement of willingness to grant a license under these rights on reasonable and non-discriminatory terms and conditions to applicants desiring to obtain such a license.

Foreword

The development work on this specification was done by the SFF Committee, an industry group. The membership of the committee since its formation in August 1990 has included a mix of companies which are leaders across the industry.

When 2 1/2” diameter disk drives were introduced, there was no commonality on external dimensions e.g. physical size, mounting locations, connector type, connector location, between vendors.

The first use of these disk drives was in specific applications such as laptop portable computers and system integrators worked individually with vendors to develop the packaging. The result was wide diversity, and incompatibility.

The problems faced by integrators, device suppliers, and component suppliers led to the formation of the SFF Committee as an industry ad hoc group to address the marketing and engineering considerations of the emerging new technology.

During the development of the form factor definitions, other activities were suggested because participants in the SFF Committee faced more problems than the physical form factors of disk drives. In November 1992, the charter was expanded to address any issues of general interest and concern to the storage industry. The SFF Committee became a forum for resolving industry issues that are either not addressed by the standards process or need an immediate solution.

Those companies which have agreed to support a specification are identified in the first pages of each SFF Specification. Industry consensus is not an essential requirement to publish an SFF Specification because it is recognized that in an emerging product area, there is room for more than one approach. By making the documentation on competing proposals available, an integrator can examine the alternatives available and select the product that is felt to be most suitable.

SFF Committee meetings are held during T10 weeks (see www.t10.org), and Specific Subject Working Groups are held at the convenience of the participants. Material presented at SFF Committee meetings becomes public domain, and there are no restrictions on the open mailing of material presented at committee meetings.

Most of the specifications developed by the SFF Committee have either been incorporated into standards or adopted as standards by EIA (Electronic Industries Association), ANSI (American National Standards Institute) and IEC (International Electrotechnical Commission).

If you are interested in participating or wish to follow the activities of the SFF Committee, the signup for membership and/or documentation can be found at:

www.sffcommittee.com/ie/join.html

The complete list of SFF Specifications which have been completed or are currently being worked on by the SFF Committee can be found at:

ftp://ftp.seagate.com/sff/SFF-8000.TXT

If you wish to know more about the SFF Committee, the principles which guide the activities can be found at:

ftp://ftp.seagate.com/sff/SFF-8032.TXT

Suggestions for improvement of this specification will be welcome. They should be sent to the SFF Committee, 14426 Black Walnut Ct, Saratoga, CA 95070.

References

The SFF Committee activities support the requirements of the storage industry, and it is involved with several standards.

Industry Documents

The following interface standards are relevant to SFP+ Specifications.
SFF-8432 - Improved Pluggable Formfactor
SFF-8083 - 0.8 mm SFP+ Card Edge Connector
SFF-8089 - SFP Rate and Application codes
SFF-8079 - SFP Rate and Application Selection
SFF-8472 - Diagnostic Monitoring Interface for Optical Transceivers
INF-8074i - SFP (Small Form Factor) Transceiver
INF-8077i - 10 Gigabit Small Form Factor Pluggable Module (XFP MSA)
FC-PI-4 - High speed signaling for 8.5 GBd Fibre Channel is defined in INCITS FC-PI-4.
10GFC - 10.51875 GBd FC INCITS Project 1413-D
FC-MJSQ - Methodologies for Jitter and Signal Quality Specifications FC INCITS Project 1316-DT Rev 14.1, June 5, 2005
IEEE802.3 CL 49 - IEEE 802.3 Standard (commonly known as 802.3ae 10Gigabit Ethernet 10GBASE-R LAN PHY)
IEEE802.3 CL 50 - IEEE 802.3 Standard (commonly known as 802.3ae 10Gigabit Ethernet 10GBASE-W WAN PHY)
IEEE802.3 CL 52 - IEEE 802.3 Standard (commonly known as 802.3ae 10Gigabit Ethernet Serial PMD)
IEEE802.3 CL 68 - IEEE 802.3 Standard (commonly known as 802.3aq 10Gigabit Ethernet LRM)
IEEE802.3ap-2007 Ethernet Operation Over Electrical Backplanes
OIF CEI - Optical Internetworking Forum -IA # OIF-CEI-02.0 Common Electrical I/O (CEI) - Electrical and Jitter Interoperability agreements for 6G+ bps and 11G+ bps I/O, February 28th, 2005

Acronyms and other abbreviations

BER	bit error ratio
CDR	clock data recovery
CRU	clock recovery unit
dBe	decibel electrical
DCD	Duty cycle distortion
DJ	deterministic jitter
dBm	decibel (relative to 1 mW)
dBo	decibel optical
DDJ	data Dependent Jitter
dRN	Difference of Relative noise see Appendix D
DUT	device under test
dWDP	Difference Waveform Distortion Penalty
EMC	electromagnetic compatibility
EMI	electromagnetic Interference
FC	Fibre Channel
h	hexadecimal notation
IEEE	Institute of Electrical and Electronics Engineers
ITU-T	ITU Telecommunication Standardization Sector
Gbit	gigabit = 10^9 bits
GBd	Gigabaud
OMA	optical modulation amplitude
PCB	printed circuit board
RJ	random jitter

RMS	root mean square
RN	relative noise
Rx	receiver
RX_LOS	Loss of signal same as defined in FC PI-4 and the inverse of signal detect (SD) in 802.3
SD	Signal Detect
SerDes	Serializer/Deserializer
SFI	SFP+ high speed serial electrical interface
SNR	signal-to-noise ratio
SRS	stress receiver sensitivity tester as defined by IEEE 802.3 CL 52
TDR	time domain reflectometry
VMA	voltage modulation amplitude
Tx	transmitter
TxRx	a combination of transmitter and receiver
UI	unit interval = 1 symbol period
WDP	waveform distortion penalty

SFF Specifications

There are several projects active within the SFF Committee. The complete list of specifications which have been completed or are still being worked on are listed in the specification at ftp://ftp.seagate.com/sff/SFF-8000.TXT

Document Sources

Those who join the SFF Committee as an Observer or Member receive electronic copies of the minutes and SFF specifications (http://www.sffcommittee.com/ie/join.html).

Copies of ANSI standards may be purchased from the InterNational Committee for Information Technology Standards (http://tinyurl.com/c4psg).

Copies of SFF, T10 (SCSI), T11 (Fibre Channel) and T13 (ATA) standards and standards still in development are available on the HPE version of CD_Access (http://tinyurl.com/85fts).

Conventions

The American convention of numbering is used i.e., the thousands and higher multiples are separated by a comma and a period is used as the decimal point. This is equivalent to the ISO/IEC convention of a space and comma.

American:	ISO:
0.6	0,6
1,000	1 000
1,323,462.9	1 323 462,

SFP+ Publication History

Revision Number	Description	Date
0.1	Initial Publication of Document, Preliminary	May 9, 2006
0.5	Initial Public Review Draft	June 29, 2006,
1.0	2nd Public Draft	August 28, 2006
1.1	3rd Public Draft	October 10, 2006
1.2	4rd Public Draft	December 21, 2006
1.3	5rd Public Draft	February 16, 2007
2.0	6th Public Draft and the 1st SFF ballot	April 26, 2007

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CHAPTER 1: SCOPE OF SFP+ SPECIFICATION

1.1 INTRODUCTION

This specification defines the electrical interfaces between the SFP+ module and host board for operation up to 11.1 GBd. The high speed electrical interface between the host and SFP+ module is called "SFI". SFI simplifies the module and leverages host based transmit pre-emphasis and host based receive equalization to overcome PCB and external media impairments.

SFI typically operates over 200mm of improved FR4 material or up to about 150 mm of standard FR4 with one connector, see 1.3. The electrical interface is based on high speed, low voltage AC coupled logic with a nominal differential impedance of 100 Ω.

The SFP+ specification includes management, connector[1], mechanical[2], low speed signaling, high speed signaling, and appendices providing implementation and measurement suggestions.

The SFP+ module could be an Electrical-to-Optical or an Electrical-to-Electrical device intended to support one or more of the applications listed in Table 1.

This specification support all data encodings for the above standards. SFP+ modules common implementation are single mode fiber, multi-mode fiber, or transmission on copper media.

SFP+ compliant hosts are permitted to support just linear modules, just limiting modules, or both linear and limiting modules.

1.2 THE SFP+ SUPPORTED STANDARDS

An SFP+ module may comply with any combination of the standards shown in Table 1, and may be suitable for other or future standards. This specification does not preclude operation at other lower signaling rates not listed in this table, such as 1.25 GBd for IEEE Gigabit Ethernet, 2.125 GBd for 2X FC, or 4.25 GBd for 4X FC.

1. Defined in SFF-8083
2. Defined in SFF-8432

Table 1 SFP+ Standard Compliance

Standard	*Signaling Rate (GBd)*	*High Speed Serial Interface*	*High Speed Serial Test Method*	*Low Speed Electrical Definitions*	*Low Speed Test Methods*	*Management*	*Mechanical / Connector*
8 GFC	8.5	FC-PI-4	FC-PI-4	Chapter 2:	Appendix D:	SFF-8472, SFF-8079, SFF-8089	SFF-8432 SFF-8083
IEEE 802.3 CL 52 (10 Gb/s Ethernet LAN PHY)	10.3125	Chapter 3:	Appendix D:				
IEEE 802.3 CL 52 (10 Gb/s Ethernet WAN PHY)	9.95328						
IEEE 802.3 CL 68 (LRM)	10.3125						
10 GFC	10.51875						
10GBase-R (IEEE 802.3 CL 49) Encapsulated in G.709 ODU-2 Frame (FEC)	11.10						

1.3 SFI TYPICAL PCB REACH (INFORMATIVE)

The SFI channel may be implemented with either Microstrip or Stripline structures. A list of common host board designs with typical PCB trace reaches are listed in Table 2, detailed channel properties and requirements are documented in A.1.

Table 2 Host Board Achievable Trace Length

Type	*Material*	*Trace Width (mm)*	*Loss Tangent*	*Copper Thickness (oz)*[1]	*Copper Thickness (µm)*	*Trace Length (mm)*
Microstrip	FR4-6/8	0.3	0.022	1	35	200
	Nelco 4000-13	0.3	0.016	1	17.5	300
Stripline	FR4-6/8	0.125	0.022	0.5	17.5	150
	Nelco 4000-13	0.125	0.016	0.5	35	200

1. Copper (oz) is defined as an ounce of copper rolled over one square foot of laminate.

CHAPTER 2: LOW SPEED ELECTRICAL AND POWER SPECIFICATIONS

2.1 INTRODUCTION

The SFP+ module low speed electrical interface has several enhancements over the Classic SFP module (INF-8074i), but an SFP+ host can be designed to also support most legacy SFP modules.

2.2 GENERAL REQUIREMENTS

The SFP+ modules are hot-pluggable. Hot pluggable refers to plugging in or unplugging a module while the host board is powered. The module signal ground pins VeeR and VeeT shall be isolated from module case.

All SFP+ module compliance points are defined and measured through the mated reference test card as defined by C.3. All SFP+ host compliance points are defined and measured through the mated reference test card as defined by C.2. All electrical specifications shall be met over the entire specified range of power supplies given in section 2.8.

2.3 SFP+ HOST CONNECTOR DEFINITION

The SFP+ host connector is a 0.8 mm pitch 20 position right angle improved connector specified by SFF-8083, or equivalent stacked connector. Host PCB pin assignment is shown in Figure 1 and pin definitions are given in Table 3. SFP+ module pins make contact to the host in the order of ground, power, followed by signal as illustrated by Figure 2 and the pin sequence order listed in Table 2.

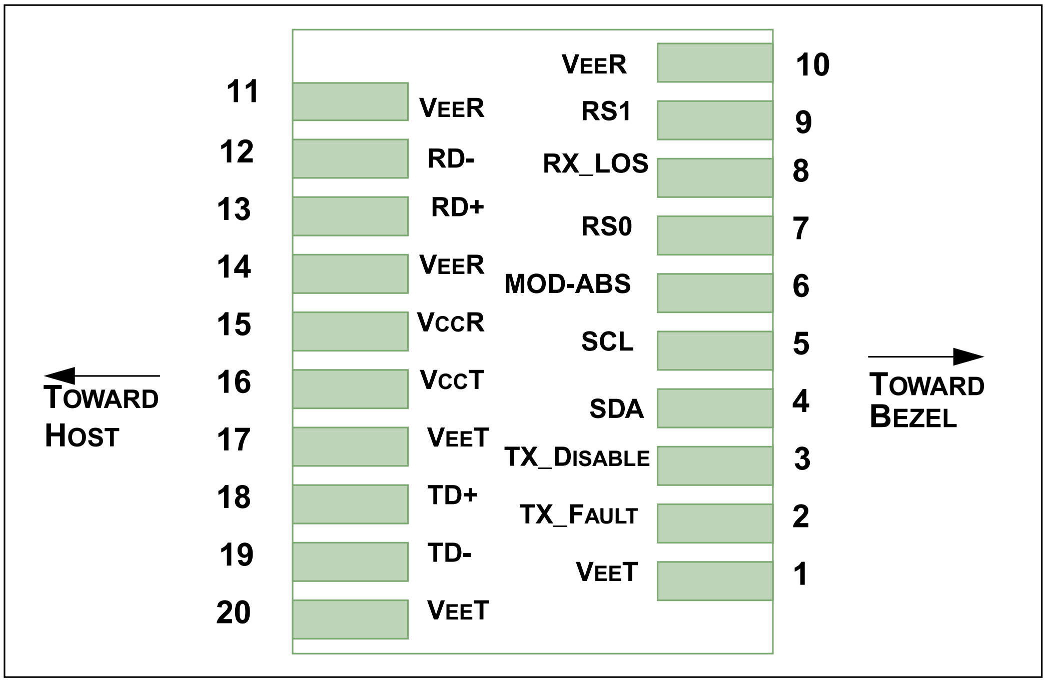

Figure 1 Host PCB SFP+ Pad Pinout Top View

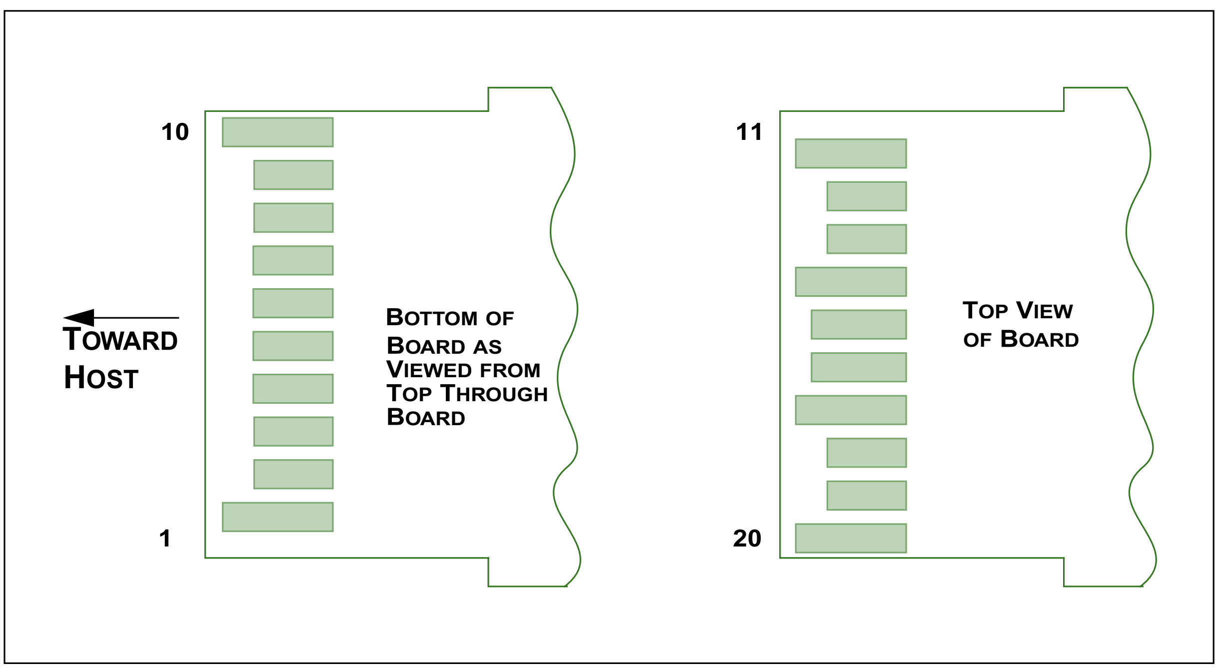

Figure 2 SFP+ Module PCB Pinout

Table 3 Module Electrical Pin Definition

Pin	Logic	Symbol	Power Sequence Order	Name/Description	Note
1		VeeT	1st	Module Transmitter Ground	1
2	LVTTL-O	TX_Fault	3rd	Module Transmitter Fault	2
3	LVTTL-I	TX_Disable	3rd	Transmitter Disable; Turns off transmitter laser output	3
4	LVTTL-I/O	SDA	3rd	2-wire Serial Interface Data Line (Same as MOD-DEF2 as defined in the INF-8074i)	4
5	LVTTL-I/O	SCL	3rd	2-wire Serial Interface Clock (Same as MOD-DEF1 as defined in the INF-8074i)	4
6		MOD_ABS	3rd	Module Absent, connected to VeeT or VeeR in the module	5
7	LVTTL-I	RS0	3rd	Rate Select 0, optionally controls SFP+ module receiver. When high input signaling rate> 4.25 GBd and when low input signaling rate ≤ 4.25 GBd.	6
8	LVTTL-O	RX_LOS	3rd	Receiver Loss of Signal Indication (In FC designated as Rx_LOS and in Ethernet designated as Signal Detect)	2
9	LVTTL-I	RS1	3rd	Rate Select 1, optionally controls SFP+ transmitter. When high input signaling rate> 4.25 GBd and when low input signaling rate ≤ 4.25 GBd.	6
10		VeeR	1st	Module Receiver Ground	1
11		VeeR	1st	Module Receiver Ground	1
12	CML-O	RD-	3rd	Receiver Inverted Data Output	
13	CML-O	RD+	3rd	Receiver Non-Inverted Data Output	
14		VeeR	1st	Module Receiver Ground	1
15		VccR	2nd	Module Receiver 3.3 V Supply	
16		VccT	2nd	Module Transmitter 3.3 V Supply	
17		VeeT	1st	Module Transmitter Ground	1
18	CML-I	TD+	3rd	Transmitter Non-Inverted Data Input	
19	CML-I	TD-	3rd	Transmitter Inverted Data Input	
20		VeeT	1st	Module Transmitter Ground	1

1. The module signal ground pins, VeeR and VeeT, shall be isolated from the module case.
2. This pin is an open collector/drain output pin and shall be pulled up with 4.7-10 kΩ to Vcc_Host Table 5 on the host board. Pull ups can be connected to multiple power supplies, however the host board design shall ensure that no module pin has voltage exceeding module VccT/R + 0.5 V.
3. This pin is an open collector/drain input pin and shall be pulled up with 4.7-10 kΩ to VccT in the module.
4. See 4.2 2-wire Electrical Specifications .
5. This pin shall be pulled up with 4.7-10 kΩ to Vcc_Host on the host board.
6. If implementing SFF-8079 pin 7 and 9 are used for AS0 and AS1 respectively.

2.4 LOW SPEED ELECTRICAL CONTROL PINS AND 2-WIRE INTERFACE

In addition to the 2-wire serial interface, the SFP+ module has the following low speed pins for control and status:

- TX_Fault
- TX_Disable
- RS0/RS1
- MOD_ABS
- RX_LOS

2.4.1 TX_FAULT

TX_Fault is a module output pin that when high, indicates that the module transmitter has detected a fault condition related to laser operation or safety.

The TX_Fault output pin is an open drain/collector and must be pulled up to the Vcc_Host in the host with a resistor in the range 4.7-10 kΩ, or with an active termination according to Table 6.

2.4.2 TX_DISABLE

TX_Disable is a module input pin. When TX_Disable is asserted high or left open, the SFP+ module transmitter output must be turned off. The TX_Disable pin must be pulled up to VccT in the SFP+ module.

When TX_Disable is asserted low or grounded the module transmitter is operating normally.

2.4.3 RS0/RS1

RS0 and RS1 are module input rate select pins and are pulled low to VeeT with a > 30 kΩ resistor in the module. RS0 is an input hardware pin which optionally selects the optical receive data path rate coverage for an SFP+ module. RS1 is an input hardware pin which optionally selects the optical transmit path data rate coverage for an SFP+ module. For logical definitions of RS0/RS1 see 2.5.

RS1 is commonly connected to VeeT or VeeR in the classic SFP modules. The host needs to ensure that it will not be damaged if this pin is connected to VeeT or VeeR in the module.

2.4.4 MOD_ABS

Mod_ABS is connected to VeeT or VeeR in the SFP+ module. The host may pull this pin up to Vcc_Host with a resistor in the range 4.7-10 kΩ. MOD_ABS is asserted “High” when the SFP+ module is physically absent from a host slot. In the SFP MSA (INF-8074i) this pin had the same function but is called MOD_DEF0.

2.4.5 SCL/SDA

SCL is the 2-wire interface clock and SDA is the 2-wire interface data line. SCL and SDA are pulled up to a voltage in the range of 3.14 V to 3.46 V on the host. For full specifications see Chapter 4: SFP+ 2-wire Interface .

2.4.6 RX_LOS

RX_LOS when high indicates an optical signal level below that specified in the relevant standard. The RX_LOS pin is an open drain/collector output and must be pulled up to Vcc_Host in the host with a resistor in the range 4.7-10 kΩ, or with an active termination according to Table 6.

RX_LOS assert min and de-assert max are defined in the relevant standard. To avoid spurious transition of RX_LOS a minimum hysteresis of 0.5 dBo is recommended.

2.5 Rate Select Hardware Control

The SFP+ module provides two inputs RS0 and RS1 that can optionally be used for rate selection. RS0 controls the receive path signaling rate capability, and RS1 controls the transmit path signaling rate capability, as defined in Table 4. The host and module may choose to use either, both, or none of these functions. A host utilizing RS1 must provide short circuit protection in case a Classic SFP [1] module is inserted.

This rate select functionality can also be controlled by software as defined by SFF-8472.

Optionally the rate select methods of Part 2 of SFF-8079 can be used instead of the method described here by setting the management declaration bit (A0h byte 93 bit 2) to 1, see SFF-8472.

Table 4 Rate Select Hardware Control Pins

Parameter	*State*	*Conditions*
RS0	Low	RX signaling rate less than or equal to 4.25 GBd
	High	RX signaling rate greater than 4.25 GBd
RS1	Low	TX signaling rate less than or equal to 4.25 GBd
	High	TX signaling rate greater than 4.25 GBd

2.6 Low Speed Electrical Specifications

SFP+ Low speed signaling is based on Low Voltage TTL (LVTTL) operating with a supply of 3.3 V ± 5%.

The 2-wire interface protocol and electrical specifications are defined in Chapter 4:.

1. RS1 pin is grounded in the Classic SFP.

2.6.1 THE SFP+ MODULE LOW SPEED ELECTRICAL SPECIFICATIONS

The SFP+ module low speed electrical specifications are given in Table 5. All I/O powered by VccT is referenced to VeeT and similarly VccR is referenced to VeeR.

Table 5 Low Speed Module Electrical Specifications

Parameter	*Symbol*	*Min.*	*Max.*	*Unit*	*Conditions*
Module Vcc Range	VccT, VccR	3.14	3.46	V	
TX_Fault, RX_LOS	V_{OL}	0.0	0.40	V	
	V_{OH}	Vcc_Host - 0.5	Vcc_Host + 0.3	V	
TX_Disable	V_{IL}	-0.3	0.8	V	Shall be pulled up with 4.7k-10k Ω to VccT in the module.
	V_{IH}	2.0	VccT + 0.3	V	Shall be pulled up with 4.7k-10k Ω to VccT in the module.
RS0, RS1	V_{IL}	-0.3	0.8	V	Shall be pulled low to VeeT with a >30 k Ω resistor in the module
	V_{IH}	2.0	VccT + 0.3	V	Shall be pulled low to VeeT with a >30 k Ω resistor in the module

2.6.2 THE SFP+ HOST LOW SPEED ELECTRICAL SPECIFICATIONS

The SFP+ Host low speed electrical specifications are given in Table 6. All I/O powered by VccT is referenced to VeeT and similarly VccR is referenced to VeeR.

Table 6 Low Speed Host Electrical Specifications

Parameter	*Symbol*	*Min.*	*Max.*	*Unit*	*Conditions*
Host Vcc Pullup	Vcc_Host	2.0	3.46	V	
TX_Fault, RX_LOS	V_{IL}	-0.3	0.8	V	Rp[1] pulled to Vcc_Host, measured at host side of connector. I_{OL}(max) = 1 mA
	V_{IH}	2.0	VccT + 0.3	V	Rpp[1] pulled to Vcc_Host, measured at host side of connector.
TX_Disable	V_{OL}	0	0.4	V	
	V_{OH}	VccT-0.5	VccT + 0.3	V	
RS0, RS1	V_{OL}	-0.3	0.4	V	
	V_{OH}	2.0	VccT + 0.3	V	

1. Rp is the pull up resistor. Active bus termination may be used by the host in place of a pullup resistor. Pull ups can be connected to multiple power supplies, however the host board design shall ensure that no module pin has voltage exceeding module VccT/R + 0.5 V.

2.7 TIMING REQUIREMENT OF CONTROL AND STATUS I/O

The timing requirements of control and status I/O are defined in Table 7.

Table 7 Timing Parameters for SFP+ Management

Parameter	Symbol	Min.	Max.	Unit	Conditions
TX_Disable assert time	t_off		10	µs	rising edge of TX_Disable to fall of output signal below 10% of nominal
TX_Disable negate time	t_on		2	ms	Falling edge of Tx_disable to rise of output signal above 90% of nominal. This only applies in normal operation, not during start up or fault recovery.
Time to initialize 2-wire interface	t_2w_start_up		300	ms	From power on or hot plug after the supply meeting Table 8.
Time to initialize	t_start_up		300	ms	From power supplies meeting Table 8 or hot plug or Tx disable negated during power up, or Tx_fault recovery, until non-cooled power level I part (or non-cooled power level II part already enabled at power level II for Tx_fault recovery) is fully operational.
Time to initialize cooled module	t_start_up_cooled		90	s	From power supplies meeting Table 8 or hot plug, or Tx disable negated during power up or Tx_fault recovery, until cooled power level I part (or cooled power level II part during fault recovery) is fully operational.
Time to Power Up to Level II	t_power_level2		300	ms	From falling edge of stop bit enabling power level II until non-cooled module is fully operational
Time to Power Down from Level II	t_power_down		300	ms	From falling edge of stop bit disabling power level II until module is within power level I requirements
TX_Fault assert	TX_Fault_on		1	ms	From occurrence of fault to assertion of TX_Fault
TX_Fault assert for cooled module	TX_Fault_on		50	ms	From occurrence of fault to assertion of TX_Fault
TX_Fault Reset	t_reset	10		µs	Time TX_Disable must be held high to reset TX_Fault
RS0, RS1 rate select timing for FC	t_RS0_FC, RS1_FC		500	µs	From assertion till stable output
RS0, RS1 rate select timing non FC	t_RS0, t_RS1		10	ms	From assertion till stable output
RX_LOS assert delay	t_los_on		100	µs	From occurrence of loss of signal to assertion of RX_LOS
RX_LOS negate delay	t_los_off		100	µs	From occurrence of presence of signal to negation of RX_LOS

2.7.1 SFP+ POWER ON INITIALIZATION PROCEDURE, TX_DISABLE NEGATED

During power on of the SFP+, TX_FAULT, if implemented, may be asserted (High) as soon as power supply voltages are within specification. For SFP+ initialization with TX_DISABLE negated, TX_FAULT shall be negated when the transmitter safety circuitry, if implemented, has detected that the transmitter is operating in its normal state. If a transmitter fault has not occurred, TX_FAULT shall be negated within a period t_start_up from the time that $V_{CC}T$ exceeds the specified minimum operating voltage (see Table 8). If the TX_FAULT remains asserted after t_start_up, the host shall determine whether the module is cooled by reading the status bit over I2C. If the module is not cooled, the host may assume that a transmission fault has occurred. If the module is cooled, the host may assume that a transmission fault has occurred if TX_FAULT remains asserted beyond t_start_up_cooled

If no transmitter safety fault reporting circuitry is implemented, the TX_FAULT signal may be tied to its negated state.

The power on initialization timing for a SFP+ with TX_DISABLE negated is shown in Figure 3.

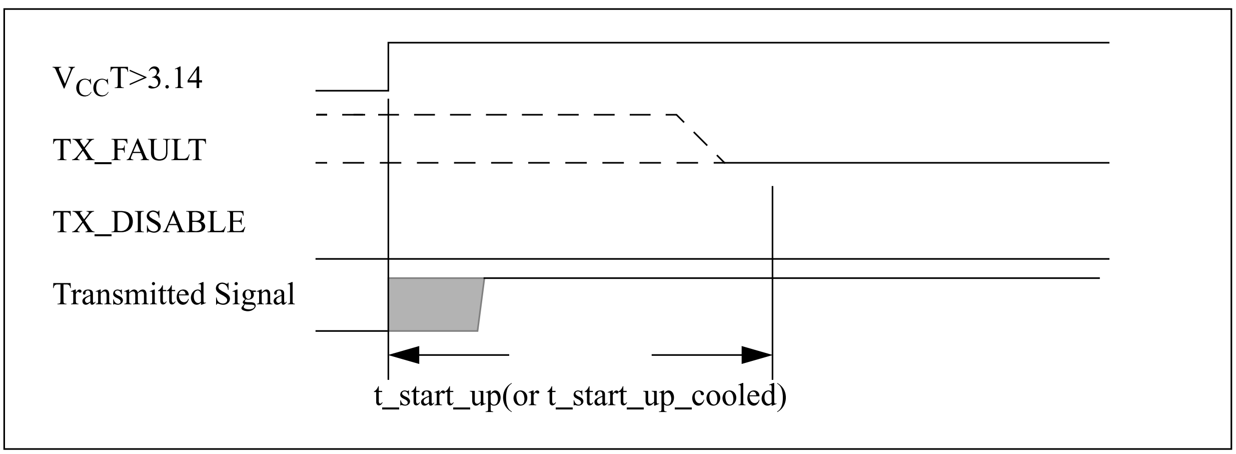

Figure 3 Power on initialization of SFP+, TX_DISABLE negated

2.7.2 SFP+ POWER ON INITIALIZATION PROCEDURE, TX_DISABLE ASSERTED.

For SFP+ power on initialization with TX_DISABLE asserted, the state of TX_FAULT is not defined while TX_DISABLE is asserted. After TX_DISABLE is negated, TX_FAULT may be asserted while safety circuit initialization is performed. TX_FAULT shall be negated when the transmitter safety circuitry, if implemented, has detected that the transmitter is operating in its normal state. If a transmitter fault has not occurred, TX_FAULT shall be negated within a period t_start_up from the time that TX_DISABLE is negated. If TX_FAULT remains asserted beyond the period t_start_up, the host may assume that a transmission fault has been detected by the SFP+.

If no transmitter safety circuitry is implemented, the TX_FAULT signal may be tied to its negated state.

The power on initialization timing for a SFP+ with TX_DISABLE asserted is shown in Figure 4.

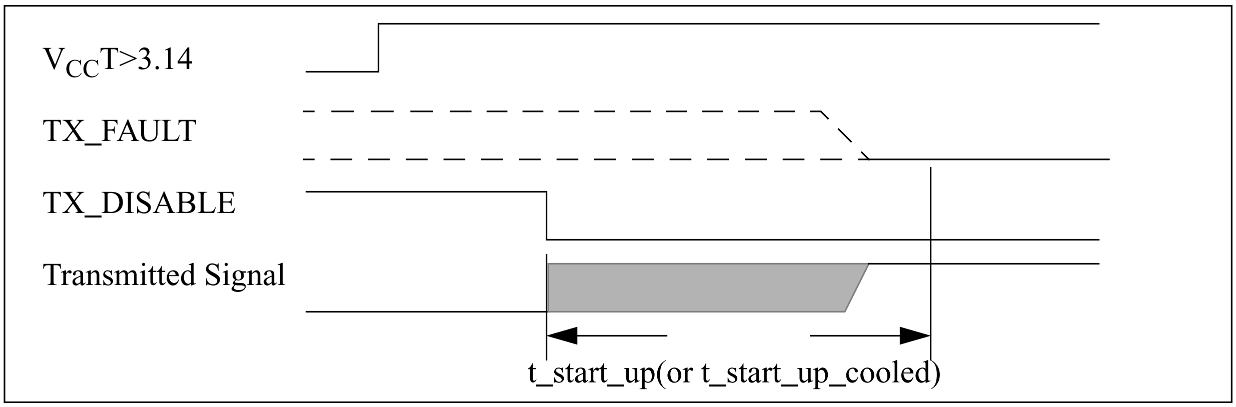

Figure 4 Power on initialization of SFP+, TX_DISABLE asserted Initialization during hot plugging of SFP+

2.7.3 Initialization During Hot Plugging

When a SFP+ is not installed, TX_FAULT is held to the asserted state by the pull up circuits on the host. As the SFP+ is installed, contact is made with the ground, voltage, and signal contacts in the specified order. After the SFP+ has determined that V_{cc}T has reached the specified value, the power on initialization takes place as described in the previous section. An example of initialization during hot plugging is provided in Figure 5.

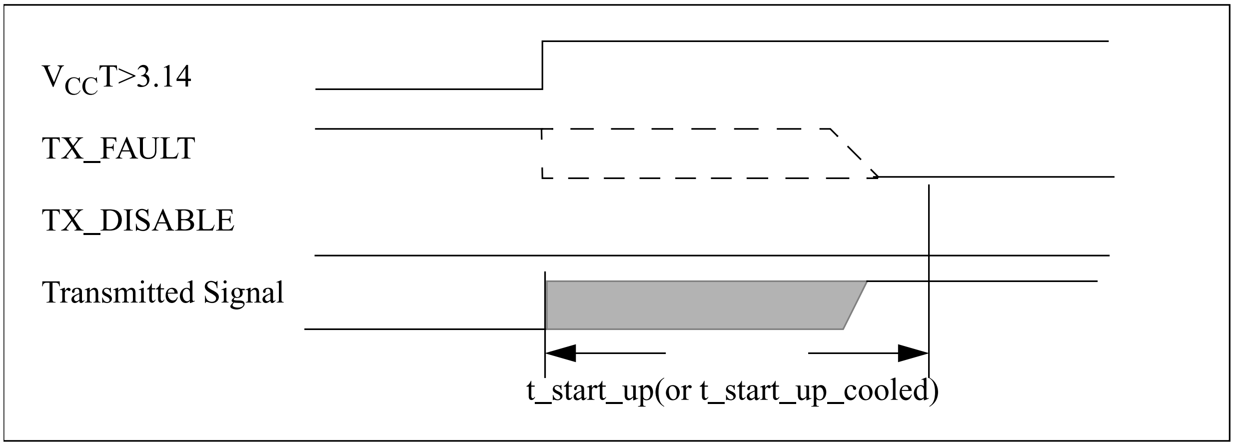

Figure 5 Example of initialization during hot plugging, TX_DISABLE negated.

2.7.4 SFP+ TRANSMITTER MANAGEMENT

The timing requirements for the management of optical outputs from the SFP+ using the TX_DISABLE signal are shown in Figure 6. Note that t_on time refers to the maximum delay until the modulated optical signal reaches 90% of the final value, not just the average optical power.

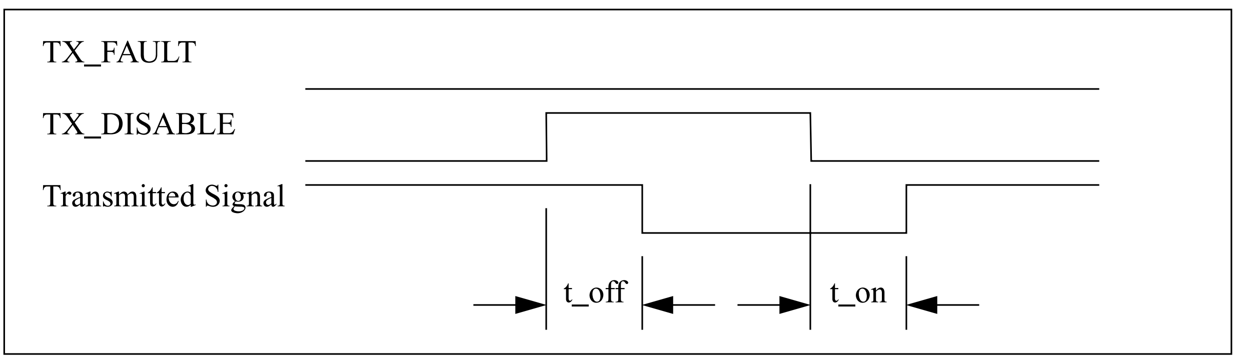

Figure 6 Management of SFP+ during normal operation, TX_DISABLE implemented

2.7.5 SFP+ FAULT DETECTION AND PRESENTATION

If TX_FAULT is implemented it shall meet the timing requirements of Figure 7. If TX_FAULT is not implemented, the signal shall be held to the low state by the SFP+.

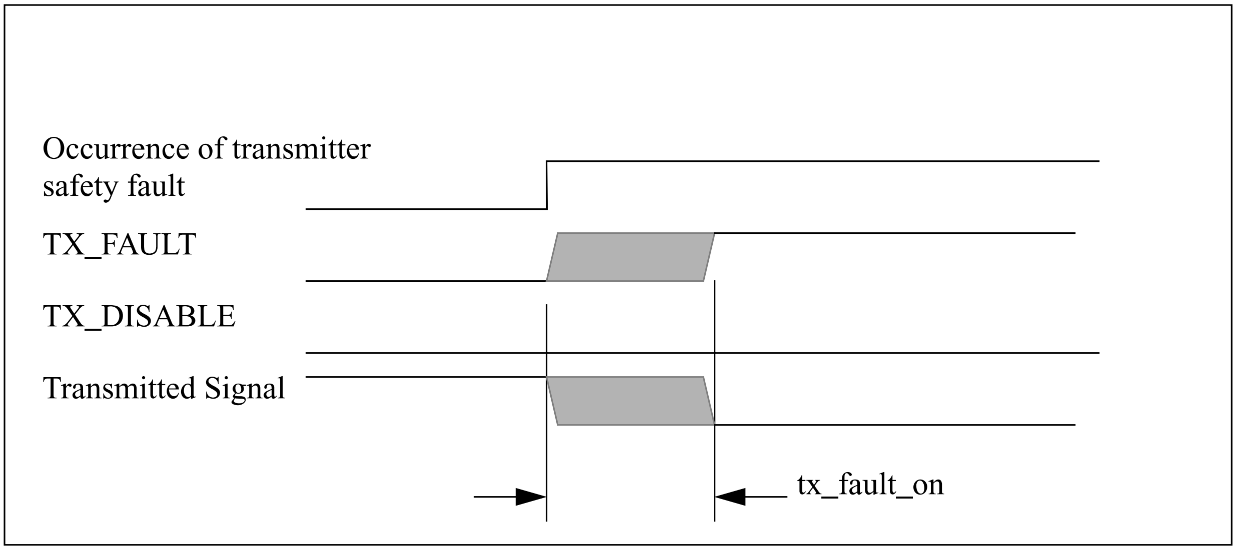

Figure 7 Detection of transmitter safety fault condition

2.7.6 SFP+ FAULT RECOVERY

The detection of a safety-related transmitter fault condition presented by TX_FAULT shall be latched. The following protocol may be used to reset the latch in case the transmitter fault condition is transient.

To reset the fault condition and associated detection circuitry, TX_DISABLE shall be asserted for a minimum of t_reset. TX_Disable shall then be negated. Alternatively the Software Tx disable is asserted and negated. In less than the maximum value of t_start_up the optical transmitter will correctly reinitialize the laser circuits, negate TX_FAULT, and begin normal operation if the fault condition is no longer present. If a fault condition is detected during the reinitialization, TX_FAULT shall again be asserted, the fault condition again latched, and the optical transmitter circuitry will again be disabled until the next time a reset protocol is attempted. The manufacturer of the SFP+ shall ensure that the optical power emitted from an open connector or fiber is compliant with applicable eye safety requirements during all reset attempts, during normal operation or upon the occurrence of reasonable single fault conditions. The SFP+ may require internal protective circuitry to prevent the frequent assertion of the TX_Disable signal from generating frequent pulses of energy that violate the safety requirements. The timing for successful recovery from a transient safety fault condition is shown in Figure 8.

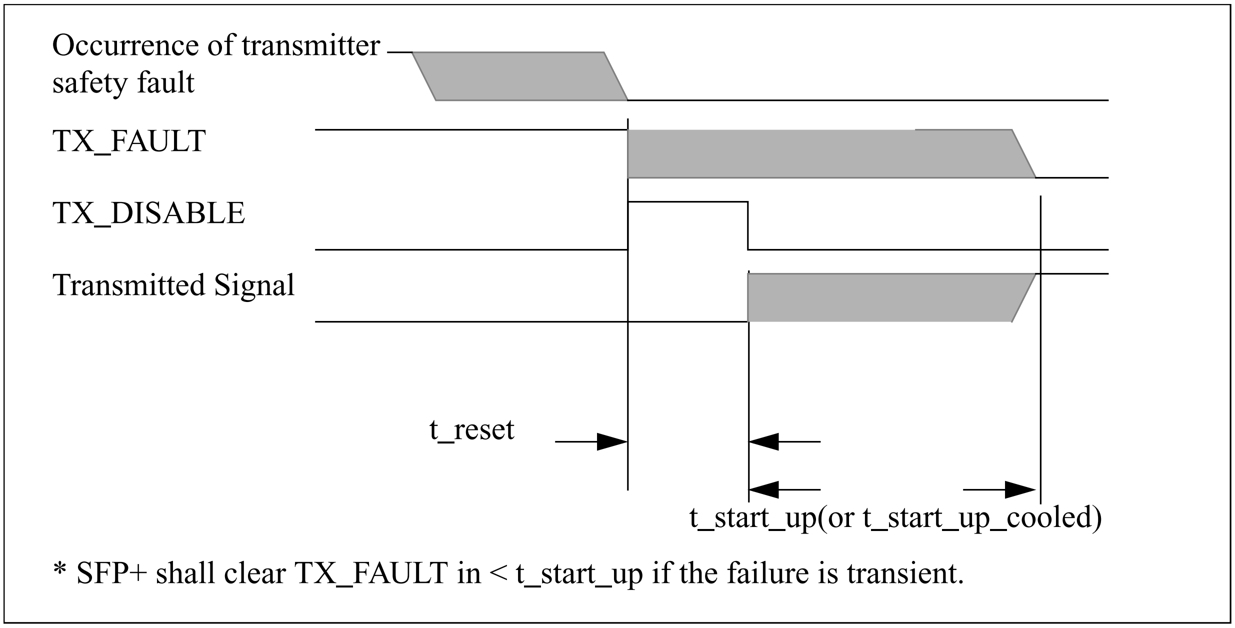

Figure 8 Successful recovery from transient safety fault condition

An example of an unsuccessful recovery, where the fault condition was not transient, is shown in figure 9.

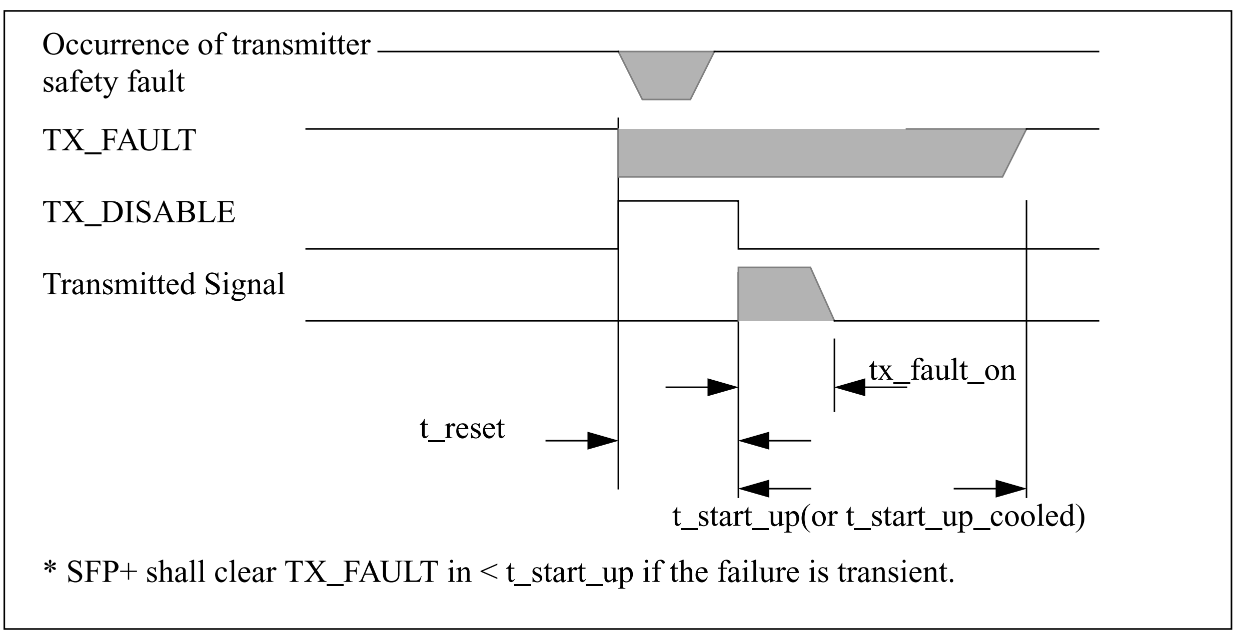

Figure 9 Unsuccessful recovery from safety fault condition

2.7.7 SFP+ LOSS OF SIGNAL INDICATION

The RX_LOS signal is intended as a preliminary indication to the system in which the SFP+ is installed that the link signals are likely to be outside the required values for proper operation. Such indications typically point to non-installed cables, broken cables, or a disabled, failing or a powered off transmitter at the far end of the cable. Additional indications are provided by the system in which the SFP+ is installed to verify that the information being transmitted is valid, correctly encoded, and in the correct format. Such additional indications are outside the scope of the SFP+ specification.

If RX_LOS is not implemented on a SFP+, it shall be held to the low state by the SFP+. If the module definition of the SFP+ is specified as implementing RX_LOS, the timing is specified in Figure 10.

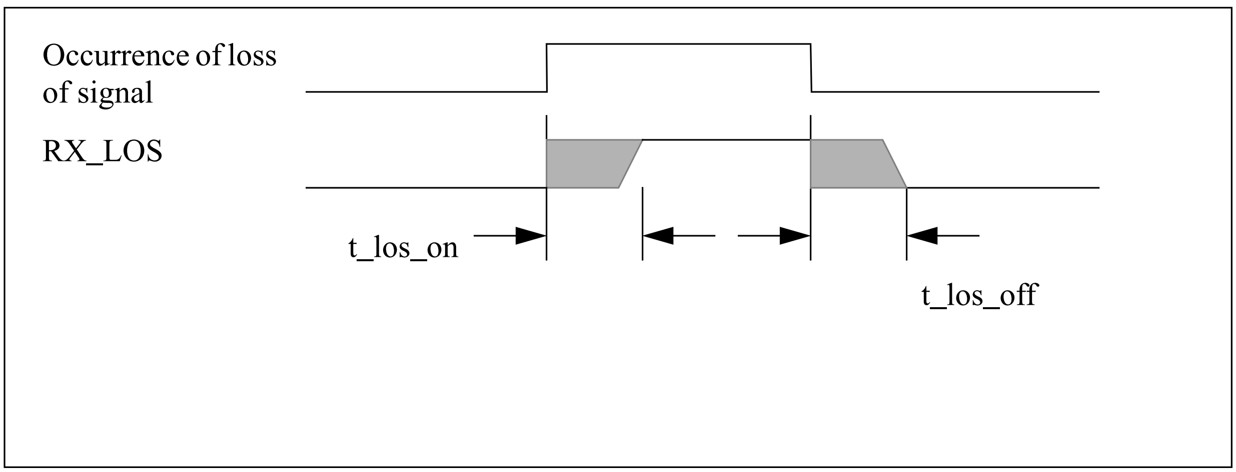

Figure 10 Timing of RX_RX_LOS detection

2.8 SFP+ POWER REQUIREMENT

The SFP+ host has two 3.3 V power pins one supplying the module transmitter voltage (VccT) and the other supplying the module receiver voltage (VccR). The maximum current capacity, both continuous and peak, for each connector pin is 500 mA.

SFP+ module maximum power dissipation must meet one of the following power classes:

- Power Level I modules – Up to 1.0 W
- Power Level II modules – Up to 1.5 W

To avoid exceeding system power supply limits and cooling capacity, all modules at power up by default must operate with ≤ 1.0W. Hosts supporting Level II operation may enable a Level II module through the 2-wire interface.

Maximum power level is allowed to exceed the classified power level for 500 ms following hot insertion or power up, or power level II authorization, however the current is limited to values given by Table 8. At host power up the host shall supply VccT and VccR to the module within 100 ms of each other.

2.8.1 MODULE POWER SUPPLY REQUIREMENTS

SFP+ module operates from the host supplied VccT and VccR. To protect the host and system operation, each SFP+ module during hot plug and normal operation shall follow the requirements listed in Table 8.

Table 8 SFP+ Module Power Supply Requirements

Parameters	*Symbol*	*Conditions*	*Min*	*Max*	*Units*
Power Level I Operation					
Power supply noise tolerance including ripple [peak-to-peak]		see		see Figure 11	mV
Power supply voltages including ripple, droop and noise below 10 Hz	VccT, VccR	Note 1	3.14	3.46	V
Module maximum peak current at hot plug		Note 2, 4		330	mA
Maximum average current for VccT or VccR		Note 5		200	mA
Module maximum current ramp		Note 2		50	mA/µs
Maximum power				1.0	W
Power Level II Operation					
Power supply noise tolerance including Ripple [peak-to-peak]		see		see Figure 11	mV
Power supply voltages including ripple, droop and noise below 10 Hz	VccT, VccR	Note 1	3.14	3.46	V
Module maximum peak current at hot plug		Note 2, 4		330	mA
Module peak current on enabling power level II		Note 2, 4		500	mA
Maximum average current for VccT or VccR		Note 5		320	mA
Module maximum current ramp		Note 2		50	mA/µs
Maximum power				1.5	W
Maximum power for the +3.3V rail at power up		Note 3		1	W

1.Set point is measured at the input to the connector on the host board. Droop is any temporary drop in voltage of the power supply such as that caused by plugging in another module or when enabling another module to power level II.
2. Current ramp is measured at the connector pin with low impedance probe.
3. Maximum module power dissipation shall not exceed 1.0 W at power up until host enables level II operation.
4. Maximum peak current duration is 500 ms
5. The maximum power dissipation is specified so a module can not use the maximum allowed current on both supplies.

2.8.2 Power Supply Noise Output

To limit wide band noise power, the host system and module shall each generate a maximum of 66 mV peak-peak noise when measured with a 1 MHz low pass filter. In addition, the host system and the module shall generate a maximum of 99 mV peak-peak noise when measured with a band-pass filter from 1 MHz-10 MHz, Table 9. For measurement methods see D.16.1.

Table 9 Maximum Noise Amplitude for SFP+ power supplies

Power Supply	*10 Hz-1 MHz (2% p-p)*	*1-10 MHz (3% p-p)*
3.3 V	66 mV	99 mV

2.8.3 POWER SUPPLY NOISE TOLERANCE

SFP+ modules shall meet all electrical requirements and remain fully operational in the presence of noise on both power input pins. The recommended tolerance test is to sweep a sinusoidal waveform on each voltage input. Power supply noise tolerance is defined by the following procedure. A sinusoidal waveform is swept in frequency at each input pin with level given by Figure 11. This test is performed with the D.16.3 Module Power Supply Tolerance Testing .

This test applies at minimum and maximum DC setpoint levels. It is also desirable for a module and host to each tolerate a degree of random or semi-random noise on all voltage pins simultaneously, but the characteristics of this noise are beyond the scope of this document.

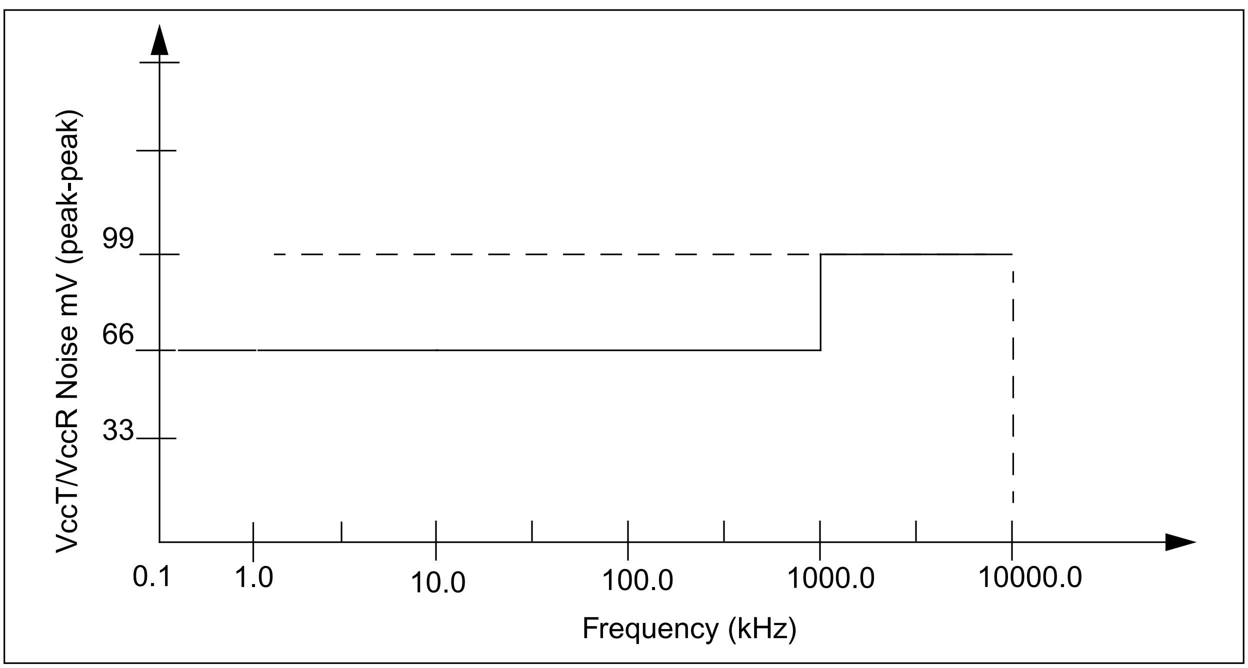

Figure 11 Power Supply Noise Tolerance

For power supply noise tolerance testing and methodology see D.16.

2.8.4 ESD

The SFP+ module and host SFI pins (High Speed Pins) shall withstand 1000 V electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B.

The SFP+ module and all host pins with exception of the SFI pins (High Speed Pins) shall withstand 2 kV electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B.

The SFP+ module shall meet ESD requirements given in EN61000-4-2, criterion B test specification such that units are subjected to 15 kV air discharges during operation and 8 kV direct contact discharges to the case.

CHAPTER 3: HIGH SPEED ELECTRICAL SPECIFICATION SFI

3.1 INTRODUCTION

SFI signaling is based on differential high speed low voltage logic with AC-coupling in the module. SFI was developed with the primary goal of low power and low electromagnetic interference (EMI). To satisfy this requirement the nominal differential signal levels are ~500 mV p-p with edge speed control to reduce EMI.

Editor Notes

This chapter has sections for which agreed values are still being determined. In some cases, the parameter definitions themselves may change. These areas are specifically marked with editor's notes. Participation to help complete these areas is encouraged.

3.2 SFI APPLICATIONS DEFINITION

The application reference model for SFI connects a high speed ASIC/SERDES to the SFP+ module as shown in Figure 12. The SFI interface is designed to support IEEE 802.3 10Gig standards Clauses 49, 50, and 51, and 10GFC. For all other FC signaling rates see FC-PI-4. SFI supported signaling rates are listed in Table 10. SFP+ compliant modules and hosts may support one or more of the signaling rates listed in Table 10.

Table 10 SFI Supported Signaling Rates

Standard	*Description*	*Signaling Rate*	*Units*
IEEE std-802.3 CL 50	10GBASE-W WAN PHY	9.95328	GBd
IEEE std-802.3 CL 49	10GBASE-R LAN PHY	10.3125	GBd
INCITS/T11 Project 1413-D	10GFC	10.51875	GBd
10Gig Ethernet with FEC	10GBASE-R over G.709	11.10	GBd

The SFI interface operates from 9.95 to 11.1 GBd.

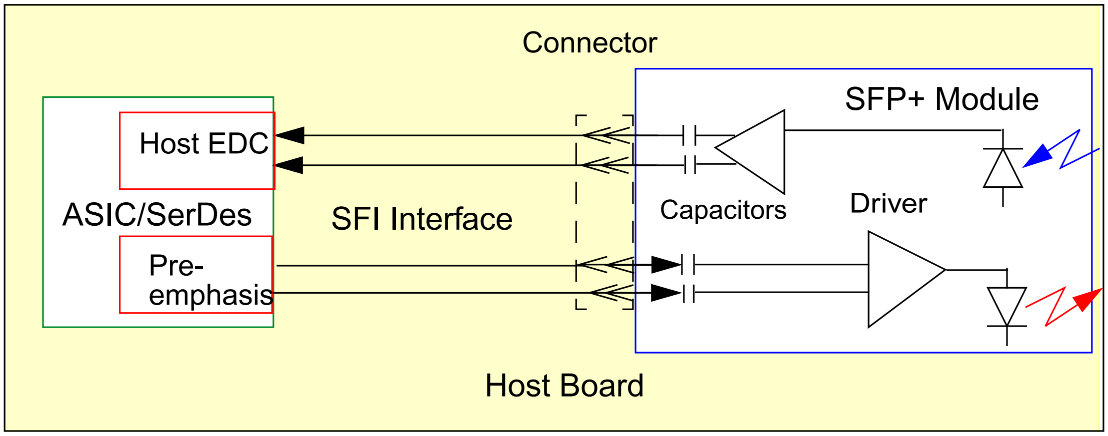

Figure 12 SFI Application Reference Model

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> **Editor Notes**
>
> Informative annex will be added for comparison between of FC-PI-4 and SFI.

3.3 SFI Test Points Definition and Measurements

SFI reference compliance test points are defined with a set of defined test boards for measurement consistency. The reference test boards provide a set of overlapping measurements for ASIC/SerDes, Module, and Host validation to ensure system interoperablity.

3.3.1 ASIC/SerDes Test Points (Informative)

ASIC/SerDes transmitter and receiver are tested on a test board as shown in Figure 13 with nominal trace loss as specified by C.1.3 to avoid degradation due to excessive trace loss and to ensure consistent measurements. The ASIC/SerDes test points are A and D.

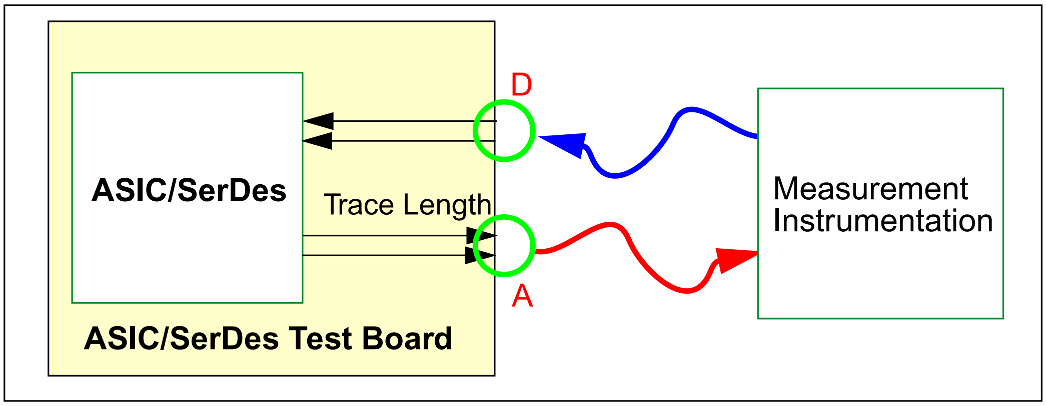

Figure 13 ASIC/SerDes Test Board

SFI ASIC/SerDes Test points are defined as the following:

- A: SerDes transmitter output at the output of the ASIC/SerDes Test Board. Specifications for A are given in B.2
- D: ASIC/SerDes input receiver at the input of the ASIC/SerDes Test Board. Specifications for D are given in B.3.

3.3.2 SFP+ Host Compliance Point

Host system transmitter and receiver compliance are defined by tests in which a Host Compliance Test Board is inserted as shown in Figure 14 in place of the SFP+ module. Test card construction should be such that it meets the requirements specified by C.1.1. The compliance points are B and C.

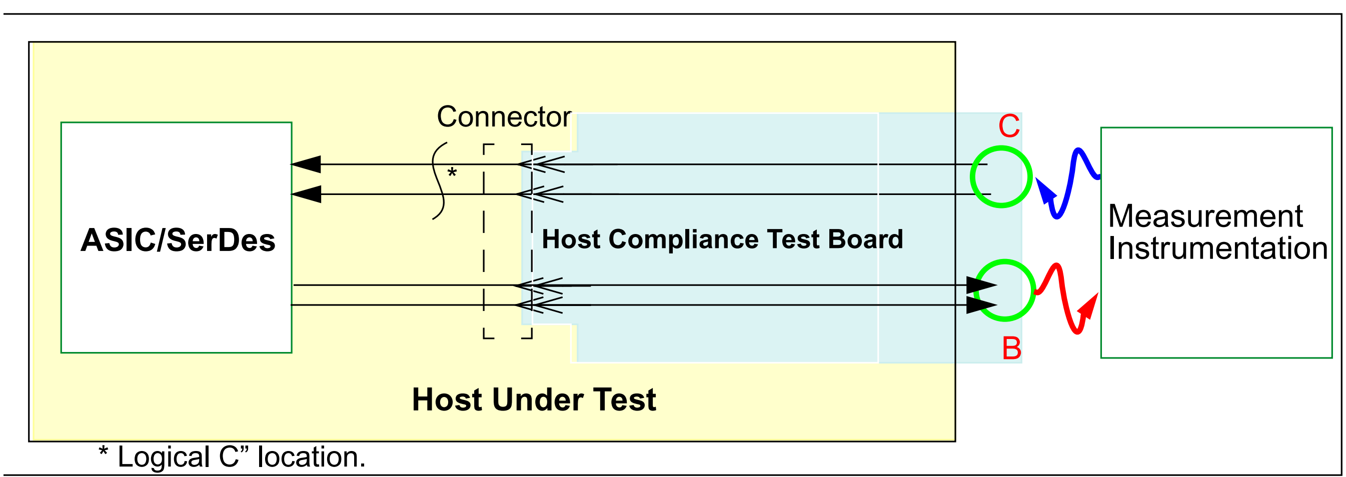

Figure 14 Host Compliance Test Board

SFP+ Host compliance points are defined as the following:

- B: Host output at the output of the Host Compliance Test Board. Specifications for B are given in 3.5.1.
- C: Host input at the input of the Host Compliance Test Board. Specifications for C are given in 3.5.2.

3.3.3 SFP+ MODULE COMPLIANCE TEST POINT

Module transmitter and receiver compliance are defined by tests in which the module is inserted into the Module Compliance Test Board as shown in Figure 15. Test card construction should be such that it meets the requirements specified by C.1.2. For improved measurement accuracy, the deviation from nominal insertion loss given in C.1.2 may be calibrated out. The compliance measurements for the module are B' and C'.

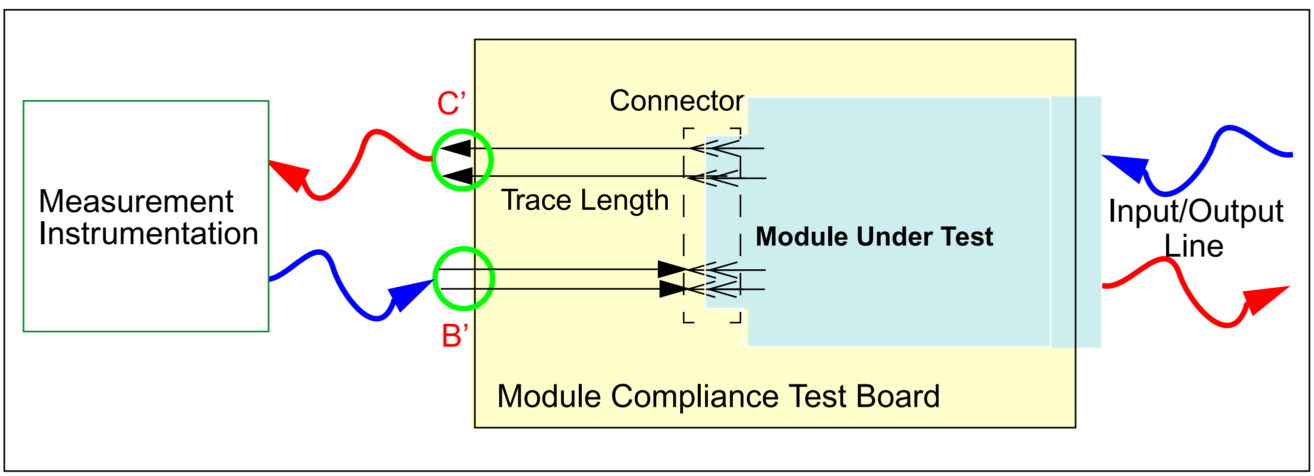

Figure 15 Module Compliance Test Board

SFP+ module compliance points are defined as the following:

- B': SFP+ module transmitter input at the input of the Module Compliance Test Board. Specifications for B' are given in 3.6.1.
- C': SFP+ module receiver output at the output of the Module Compliance Test Board. Specifications for C' are given in 3.6.2.

3.3.4 Module Input Calibration Points

Module transmitter input tolerance signal is calibrated through the Module Compliance Test Board at the output of the Host Compliance Test Board as shown in Figure 16. The opposite data path is excited with asynchronous test source with PRBS31 or a valid 64B/66B signal. The module input calibration point is at B” with specifications for B” given in 3.6.1. Compliance point B” has additional trace loss beyond the module pins given by C.1.1.

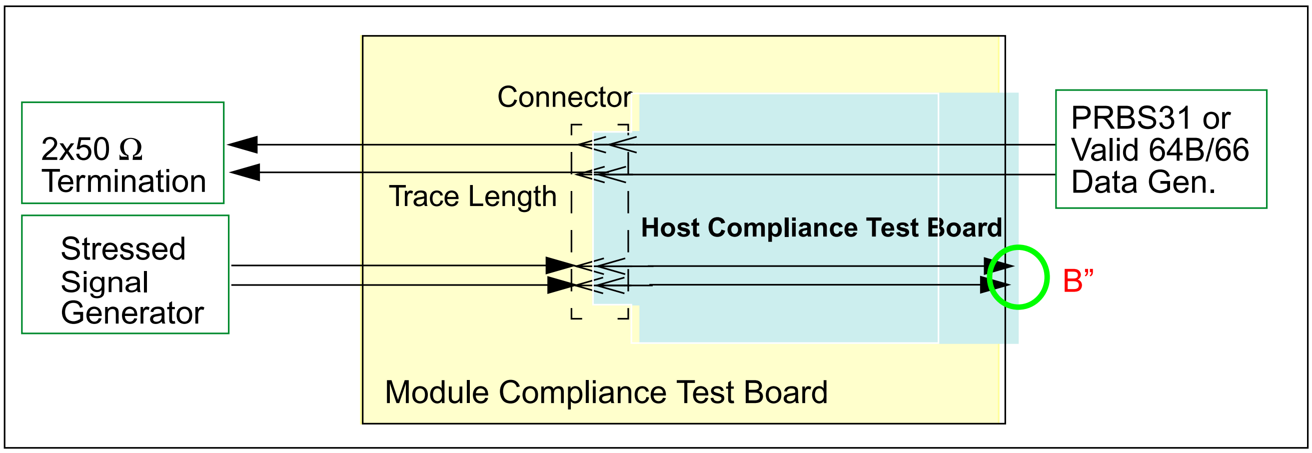

Figure 16 Module input calibration point B”

3.3.5 Host Input Calibration Point

Host receiver input tolerance signal is calibrated through Host Compliance Test Board at the output of the Module Compliance Test Board as shown in Figure 16. The host input calibration point is at C” with specifications for C” given in 3.5.2. The compliance point C” has additional trace loss beyond the SFF-8083 connector pin pins given by C.1.2.

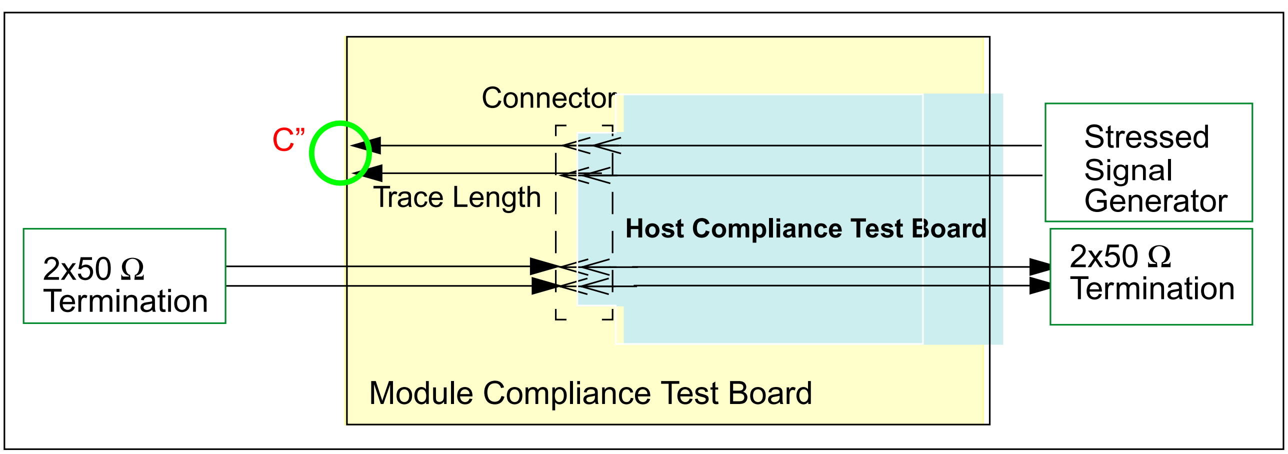

Figure 17 Host input calibration point C”

3.4 SFI TERMINATION AND DC BLOCKING

The SFI link uses nominal 100 Ω differential source and load terminations on both the host board and the module. The SFI driver terminations provide both differential and common mode termination. The SFI driver and receiver termination specifications for each of the compliance points are given by:

- Host – 3.5 SFP+ Host System Specifications
- Module – 3.6 SFP+ Module Specifications .

Host SerDes termination recommendations are given by:

- ASIC/SerDes – Appendix B:

SFP+ modules shall incorporate blocking capacitors on all SFI input and outputs as shown in Figure 18. The SFI driver is represented by terminations Z_p and Z_n which form a 100 Ω differential source. Each termination has a nominal value of 50 Ω, and therefore the common mode impedance is 25 Ω. The SFI receiver is represented with termination Z_{diff} with nominal 100 Ω value. This representation is not intended to preclude the use of other implementations which may provide common mode termination, however the SFI specification does not require any common mode termination at the receiver.

Warning: The host expects DC blocking in the module, but for improved performance the Host Compliance Test Board does not incorporate DC blocking. DC blocks within the test equipment or external are necessary.

It is recommended that both the module and the host use transmission lines targeted to have 100 W differential impedance with about 7% coupling. Differential traces with nominal 7% coupling offer a good compromise and delivers reasonable common mode match while maintaining practical transmission lines geometry. These are the targets for the module and host compliance test boards described in Appendix C:.

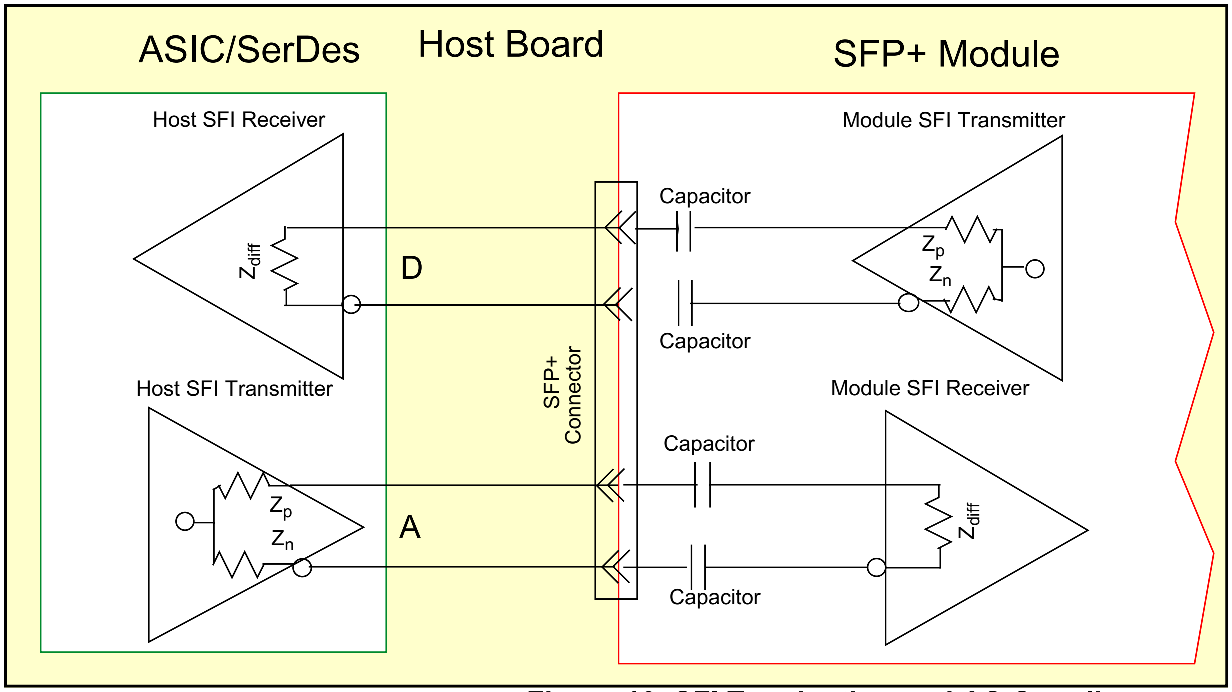

Figure 18 SFI Termination and AC Coupling

3.5 SFP+ HOST SYSTEM SPECIFICATIONS

SFP+ Host system transmitter specifications at compliance point B are given in 3.5.1. SFP+ Host system receiver specifications at compliance point C are given in 3.5.2.

All specifications are to be met using the Host Compliance Test Board as defined in 3.3.2.

Editor Notes

Rise and fall times are measured with Module or Host compliance test boards. The rise and fall time values are estimated. With further investigation, these number may change.

3.5.1 SFP+ HOST TRANSMITTER OUTPUT SPECIFICATIONS AT B

SFP+ Host transmitter electrical specifications defined at compliance point B are given in Table 11. These specifications are defined at the output of the Host Compliance Test Board specified in C.2..

Editor Notes

Table 12, jitter specifications are still under development. Differential return losses are specified to help control data-dependent jitter due to multiple-path reflections when a module is plugged into a host. Although tighter differential return loss specifications can reduce jitter, the trade off with other options and cost must be considered.

Editor Notes

Differential return losses are specified to help control data-dependent jitter due to multiple-path reflections when a module is plugged into a host. Although tighter differential return loss specifications can reduce jitter, the trade off with other options and cost must be considered.

D?.?/AT108 asks: Having redefined all the S-parameters as seen through a channel with ~0.7 dB one-way loss at 5.5 GHz, do we need to revise all the spec limits?

D1.0/AT52 asks to tighten the -10 dB low frequency SDD22, to reduce jitter-induced reflections.

Editor Notes

Limits on crosstalk and return loss are required for the electrical connector and/or the combined compliance test boards. The forum for this work is TBD, as are the exact parameters and values of the specs. D1.1/AT183 proposes a frequency-integrated crosstalk spec or smoothed crosstalk mask as well as an unsmoothed mask. D1.3/AT102 proposes a frequency-integrated SDD22 spec or smoothed SDD22 mask as well as an unsmoothed mask, in each case where an SDD11 or SDD22 spec is used.

Table 11 SFP+ Host Transmitter Output Electrical Specifications at B

Parameter - B	*Symbol*	*Conditions*	*Min*	*Target*	*Max*	*Units*
Termination Mismatch at 1 MHz	ΔZ_M	See D.15, Figure 46			5	%
Single Ended Output Voltage Range			-0.3		4.0	V
Output AC Common Mode Voltage		See D.13			12.5	mV (RMS)
Differential Output S-parameter [1]	SDD22	0.01-2.8 GHz			-10	dB
		2.8-11.1 GHz			see 2	dB
Common Mode Output S-parameter [3,4]	SCC22	0.01-2.5 GHz			-6	dB
		2.5-11.1 GHz			-3	dB

1. Reference differential impedance is 100 Ω.
2. Reflection coefficient given by equation $SDD22(dB) = -6.15 + 13.33 \, Log_{10}(f/5.5)$, with f in GHz.
3. Common mode reference impedance is 25 Ω.
4. The specification of common mode input return loss reduces EMI and noise by absorbing common mode reflections and noise.

Editor Notes

D1.1/AT57 says eye mask X1 should keep in step with TJ_max/2 but at a realistic threshold of statistical significance >10^-12. Referred to ad hoc. Change could lead to changes in methodology in D.2.

Editor Notes

D0.5/AT27 says review if UJ limit is appropriate for SR and LR.

Editor Notes

D1.1/AT51says TJ of 0.28 UI is referred to ad hoc to further study.

Editor Notes

Deterministic pulse shrinkage has been shown to be the most harmful form of DDJ for affecting TDP and TWDP, and it must be separately controlled. See 'Relationship of TX DDJ and PWS to TWDP and TDP' and 'Jitter specs at B' and B derived from necessity: Effect of high probability jitter into Tx on TWDP' from March meeting. See also D1.1/AT53 (beware factors of 2 in definition), D1.1/AT54, D1.2/AT31, and D1.3/AT57.

Editor Notes

DDJ limit is controversial. D0.5/G3 and D0.5/B1ask for an increase because 0.1UI DDJ might be challenging for the host taking into account SERDES jitter and channel jitter, temperature and process. D0.5/AT24, D1.0/AT53 and D1.1/AT52 point out that non-test-equipment reflections force a relative tightening of jitter generation vs. jitter tolerance, suggests tightening the transmit jitter specs. D0.5/AT26 says these jitter numbers degrade TWDP too much. D0.5/P24 proposes DDJ max 0.08 to achieve TDP. See also D1.0/G4, and D1.3/AT55.

The SFI jitter specifications at reference point B are listed in Table 12 and the compliance mask is shown in Figure 19.

Table 12 SFP+ Host Transmitter Output Jitter and Eye Mask Specifications at B

Parameters- B	*Symbol*	*Conditions*	*Min*	*Target*	*Max*	*Units*
Total Jitter	TJ	See 1, D.5			0.28	UI(p-p)
Data Dependent Jitter	DDJ	See D.3			0.1	UI(p-p)
Pulse Width Shrinkage Jitter	PWS				TBD	UI (p-p)
Uncorrelated Jitter	UJ	See D.4			0.023	UI (RMS)
Eye Mask	X1	See D.2			0.14	UI
Eye Mask	X2				0.35	UI
Eye Mask	Y1		90			mV
Eye Mask	Y2				350	mV

1. The data pattern for the Total Jitter Measurement is one of IEEE 802.3 CL52.9 Pattern 1, Pattern 3, or valid 64/66B data traffic.

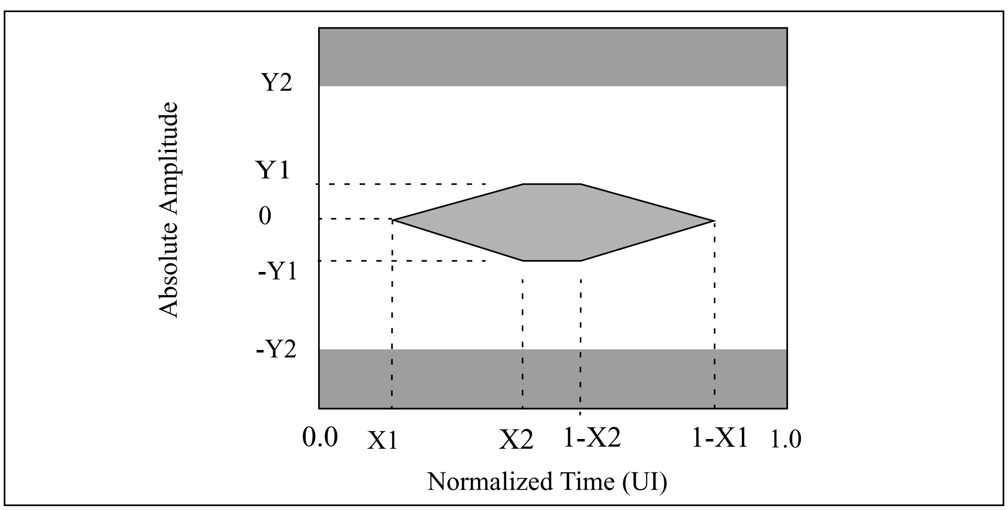

Figure 19 SFP+ Host Transmitter Differential Output Compliance Mask at B

3.5.2 SFP+ HOST RECEIVER INPUT SPECIFICATIONS AT C AND C”

The SFP+ Host receiver electrical specifications at compliance point C are given in Table 13. The host shall provide differential termination and must constrain differential to common mode conversion for quality signal termination and low EMI, as given in Table 13. Common mode termination on the receiver is not required.

Signals used as input tolerance test conditions are calibrated at C” with the Host Compliance Test Board connected through a Module Compliance Test Board to measurement instrumentation. Specifications at C” supporting limiting module are given in Table 14. Specifications at C” supporting linear module are given in Table 15.

SFP+ compliant hosts are allowed to support just linear modules, just limiting modules, or both linear and limiting modules.

Table 13 SFP+ Host Receiver Input Electrical Specifications at C

Parameter - C	*Symbol*	*Conditions*	*Min*	*Target*	*Max*	*Units*
Single Ended Output Voltage Range	Vcm		-0.3		4.0	V
Differential Input S-parameter [1]	SDD11	0.01-2.8 GHz			-10	dB
		2.8-11.1 GHz			see 2	dB
Differential to Common Mode Conversion	SCD11	0.1-11.1 GHz			-10	dB

1. Reference differential impedance is 100 Ω.
2.Reflection Coefficient given by equation SDD11(dB)= -6.15 + 13.33 Log_{10}(f/5.5), with f in GHz .

Jitter specifications to support the limiting module are listed in Table 14. Figure 20 gives the host compliance eye mask requirements for the limiting module. Host shall operate at and between the sensitivity and overload limits. SFP+ limiting host shall operate with sinusoidal jitter tolerance given by Figure 21. Test procedures for the host for limiting module are given in D.7.

Editor Notes

D1.1/AT61 says EDC receiver can do better than G.Ethernet host (0.462 UI of DJ), proposes DJ max 0.5. Response compares 4GFC (0.4 UI?).

Editor Notes

D1.1/AT62 says EDC receiver can do better than G.Ethernet host (0.749 UI of TJ), proposes TJ max 0.75. Response compares 4GFC (0.65 UI?). D1.2/CO1 compares XFP, proposes at least 0.65 or explicitly specify the portion of the TJ that is expected to be equalizable. D1.3/G1 says Random Jitter may be greater than 0.28UI at BER 1E-12 with an SRS input, Increase TJ to 0.76UIpp.

Editor Notes

D1.1/AT57 says eye mask X1 should keep in step with TJ_max/2 but at a realistic threshold of statistical significance $>10^{-12}$. Referred to ad hoc. Change could lead to changes in methodology in D.2.

Table 14 SFP+ Host Receiver Input Specifications at C" Supporting Limiting Module

Parameters - C	*Symbol*	*Conditions*	*Min*	*Target*	*Max*	*Units*
Input AC Common Mode Voltage Tolerance		See D.14			7.5	mV (RMS)
Input Rise and Fall time (20% to 80%)	Tr,Tf	See 1		34		ps
Deterministic Jitter	DJ	See 2, D.5, D.7			0.42	UI (p-p)
Pulse Width Shrinkage Jitter	PWS	See D.3			TBD	UI (p-p)
Total Jitter	TJ	BER 1E-12 see 3, D.5, D.7			0.70	UI (p-p)
Eye Mask	X1	See D.2, D.7			0.35	UI
Eye Mask Amplitude Sensitivity	Y1		150			mV
	Y2				TBD	mV
Eye Mask Amplitude Overload	Y1		TBD			mV
	Y2				425	mV

1. Measured with Host Compliance Test Board
2. Includes sinusoidal jitter when measured with the reference PLL specified by the given standard.
3. The data pattern for the Total Jitter Measurement is one of IEEE 802.3 CL52.9 Pattern 1, Pattern 3, or valid 64B/66B data traffic.

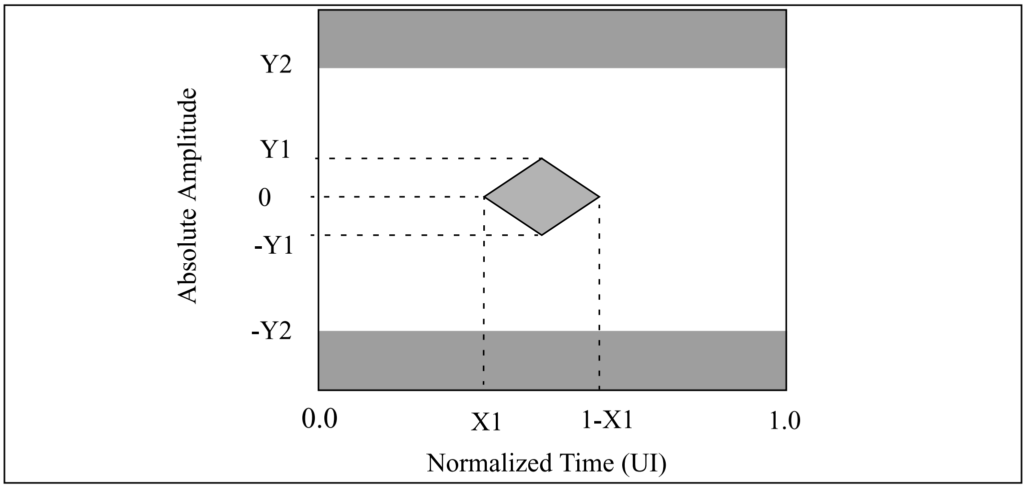

Figure 20 SFP+ Host Receiver Differential Input Compliance Mask at C" Supporting Limiting Module

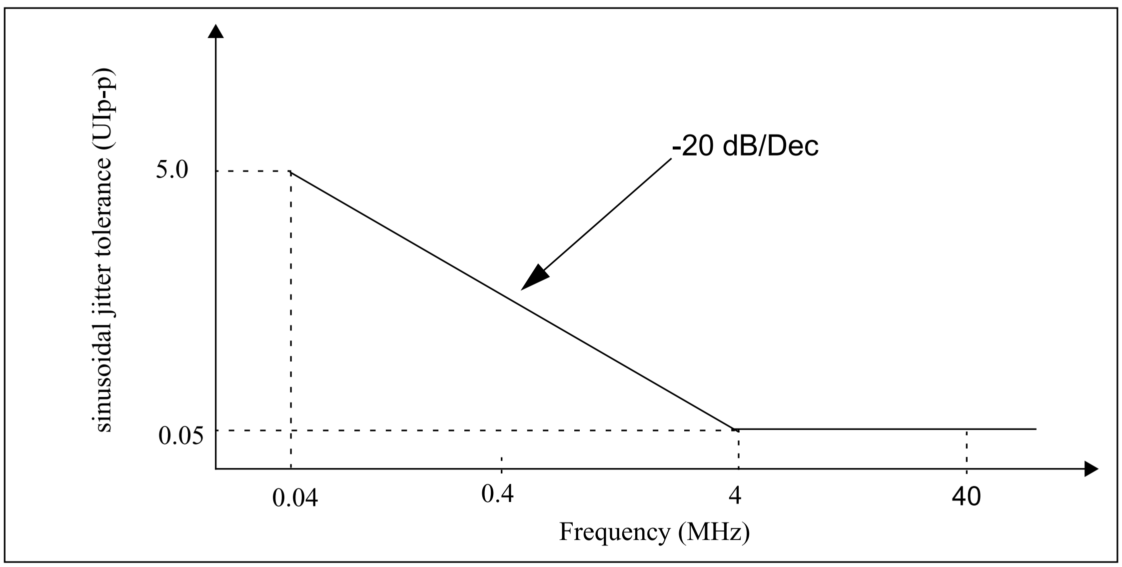

Figure 21 SFP+ Limiting Host Sinusoidal Jitter Tolerance Mask

The parameters in the Table 15 include the effects of a worst case module that operates in conjunction with optical TP3 tester(s) defined for the LRM and LR standards. Test procedures for the linear host are given in D.11.

Editor Notes

Host compliance test conditions for LR, including RN, are under development. The RN values for LRM links should include the contribution from the TP3 test conditions; the LRM RN values are currently based on the trade off equation for dRN (module noise only) in Table 20.

Table 15 SFP+ Host receiver supporting linear module input compliance test signal calibrated at C"

Parameters - C	*Symbol*	*Conditions*	*Min*	*Target*	*Max*	*Units*
Input AC Common Mode Voltage Tolerance		See D.14		7.5		mV (RMS)
Input Rise and Fall time (20% to 80%)	Tr, Tf			34		ps
Waveform Distortion Penalty for host supporting a linear LR module[1]	WDP	See 2 and D.11 with RN=0.084 RMS		TBD		dB
Waveform Distortion Penalty for host supporting an LRM module	WDP	See 2 and D.11 for Pre-Cursor with RN=0.030 RMS		4.6		dB
	WDP	See 2 and D.11 for Symmetric Stressor with RN=0.0135 RMS		5.2		dB
	WDP	See 2 and D.11 for Post-Cursor with RN=0.030 RMS		4.7		dB
Differential Voltage Modulation Amplitude	VMA	See 3	180		600	mV

1. SR specifications are covered by the fact that LR links have high noise, and on the other extreme, LRM links have high distortion.
2. Compliance stress test conditions. WDP is calibrated with reference receiver with FFE/DFE (14,5).
3.Peak levels may exceed VMA due to overshoot of the far end transmitter.

3.6 SFP+ MODULE SPECIFICATIONS

SFP+ module transmitter specifications at compliance point B’ are given in 3.6.1. SFP+ module receiver specifications at compliance point C’ are given in 3.6.2.

Editor Notes

Rise and fall times are measured with Module or Host compliance test boards. The rise and fall time values are estimated. With further investigation, these number may change.

3.6.1 SFP+ MODULE TRANSMITTER INPUT SPECIFICATIONS AT B’ AND B”

The SFP+ module transmitter electrical specifications are given in Table 16, at compliance point B’ are measured with the Module Compliance Test Board as shown in 3.3.3. The transmitter input impedance is 100 Ω differential. The module must provide differential termination and reduce differential to common mode conversion for quality signal termination and low EMI, as given in Table 16.

The specifications used for this calibration are listed in Table 17 and the compliance mask is shown in Figure 22. Signals used as input conditions for testing the transmitter input tolerance are calibrated at B” with the module compliance test board connected through a host compliance test board to appropriate instrumentation.

Editor Notes

Differential return losses are specified to help control data-dependent jitter due to multiple-path reflections when a module is plugged into a host. Although tighter differential return loss specifications can reduce jitter, the trade off with other options and cost must be considered.

Table 16 SFP+ Module Transmitter Input Electrical Specifications at B'

Parameter - B'	*Symbol*	*Conditions*	*Min*	*Target*	*Max*	*Units*
Single Ended Output Voltage Tolerance	Vcm		-0.3		4.0	V
Differential Input S-parameter [1]	SDD11	0.01-3.9 GHz			-10	dB
		3.9-11.1 GHz			see 2	dB
Differential to Common Mode Conversion [3,4]	SCD11	0.01-11.1 GHz			-10	dB

1. Reference differential impedance is 100 Ω.
2. Reflection Coefficient given by equation SDD11(dB)= -8 + 13.33 Log_{10}(f/5.5), with f in GHz.
3. Common mode reference impedance is 25 Ω.
4. Differential to common mode conversion relates to generation of EMI.

Editor Notes

Table 17, jitter specifications are still under development. Differential return losses are specified to help control data-dependent jitter due to multiple-path reflections when a module is plugged into a host. Although tighter differential return loss specifications can reduce jitter, the trade off with other options and cost must be considered.

Editor Notes

See editor's notes for DDJ and PWS for Table 12. See also D0.5/AT29, D1.0/AT66, D0.5/P31, D1.1/AT76, D1.3/BR14, and D1.3/AT72.

Editor Notes

See editor's notes for TJ for Table 12. See also D1.1/AT74.

Editor Notes

See editor's notes for UJ for Table 12. Also, D1.2/AMCC27 says: Spec allows 0.18 UIpp for all non-DDJ jitter. If Gaussian, around 0.0013 UIrms. Part must be allocated to other jitter sources such as crosstalk and systematic jitter in the SERDES. If 2/3 allocated to SERDES random noise and 1/3 to other sources, then the remainder for SERDES random jitter is 0.00086 UIrms, approaching the jitter contributed by reasonably priced crystal oscillators.

Editor Notes

Response to D1.3/AT125 suggests using the stressed eye generator of D.6 with different parameters to validate the jitter limits of 3.6.1. What parameters should define this SEG? Referred to ad hoc.

Table 17 SFP+ Module Transmitter Input Jitter Specifications at B"

Parameters- B'	*Symbol*	*Conditions*	*Min*	*Target*	*Max*	*Units*
Input AC Common Mode Voltage Tolerance		See D.14			12.5	mV (RMS)
Total Jitter	TJ	See 1, D.5			0.28	UI (p-p)
Data Dependent Jitter	DDJ	See D.3			0.10	UI (p-p)
Pulse Width Shrinkage Jitter	PWS				TBD	UI (p-p)
Uncorrelated Jitter	UJ	See D.4			0.023	UI (RMS)
Eye Mask	X1	See D.2			0.14	UI
Eye Mask	X2				0.35	UI
Eye Mask	Y1		90			mV
Eye Mask	Y2				350	mV

1. The data pattern for the Total Jitter Measurement is one of IEEE 802.3 CL52.9 Pattern 1, Pattern 3, or valid 64B/66B data traffic.

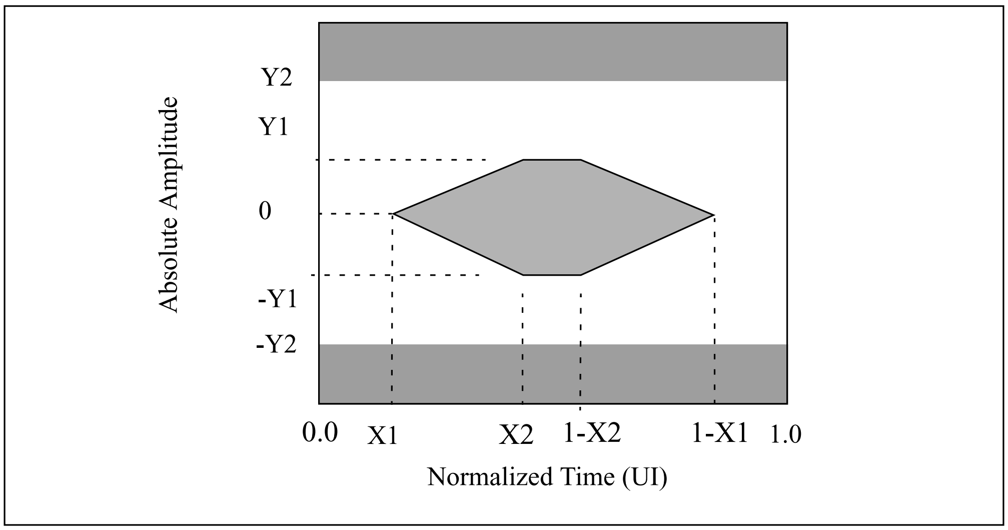

Figure 22 SFP+ Module Transmitter Differential Input Compliance Mask at B"

3.6.2 SFP+ MODULE RECEIVER OUTPUT SPECIFICATIONS AT C’

The SFI receiver electrical output specifications at compliance point C’ are given in Table 18. The module must provide differential termination and common mode termination for quality signal termination and low EMI, as given in Table 18.

Table 18 SFP+ Module Receiver Output Electrical Specifications at C’

Parameter - C’	*Symbol*	*Conditions*	*Min*	*Target*	*Max*	*Units*
Termination Mismatch at 1 MHz	ΔZ_M	See D.15, Figure 46			5	%
Single Ended Output Voltage Tolerance			-0.3		4.0	V
Output AC Common Mode Voltage		see D.13			7.5	mV (RMS)
Output Rise and Fall time (20% to 80%)	Tr, Tf	See 1	30			ps
Differential Output S-parameter [2]	SDD22	0.01-3.9 GHz			-10	dB
		3.9-11.1 GHz			see 3	dB
Common Mode Output Reflection Coefficient [4,5]	SCC22	0.01-2.5 GHz			-6	dB
		2.5-11.1 GHz			-3	dB

1. Measured with Module Compliance Test Board and OMA test pattern. Use of four 1’s and four 0’s sequence in the PRBS 9 is an acceptable alternative.
2. Reference differential impedance is 100 Ω.
3. Reflection Coefficient given by equation SDD22(dB)= $-8 + 13.33 \, \mathrm{Log}_{10}(f/5.5)$, with f in GHz.
4. Common mode reference impedance is 25 Ω.
5. Common Mode Output Reflection Coefficient helps absorb reflection and noise improving EMI.

Jitter specifications for limiting modules are listed in Table 19. Figure 23 gives the compliance eye mask for limiting modules output. Requirements for linear modules are given in Table 20.

Editor Notes

See editor’s notes for TJ for Table 14. See also D0.5/AT32 and D1.1/AT82.

Editor Notes

See editor’s notes for DJ for Table 14. See also D1.1/AT81.

Editor Notes

Response to D1.2/AT11: DJ and TJ are as defined by MJSQ CL 8.3. Low probability RJ from the SRS tester may be calibrated out in the TJ measurement. Piers will provide a write up for the new D.3 for measurement of jitter (DJ, TJ).

Editor Notes

D1.1/AT57 says eye mask X1 should keep in step with TJ_max/2 but at a realistic threshold of statistical significance >10^-12. Referred to ad hoc." Change could lead to changes in methodology in D.2.

Table 19 SFP+ Module Receiver Output Jitter and Eye Mask Specifications at C' for Limiting Module

Parameters - C'	*Symbol*	*Conditions*	*Min*	*Target*	*Max*	*Units*
Total Jitter	TJ	See 1, D.5			0.70	UI (p-p)
Deterministic Jitter	DJ	See D.5,			0.42	UI (p-p)
Eye Mask	X1	See D.2, D.7			0.35	UI
Eye Mask	Y1		150			mV
Eye Mask	Y2				425	mV

1. The data pattern for the total jitter measurement is one of IEEE 802.3 CL52.9 Pattern 1, Pattern 3, or valid 64B/66B data traffic.

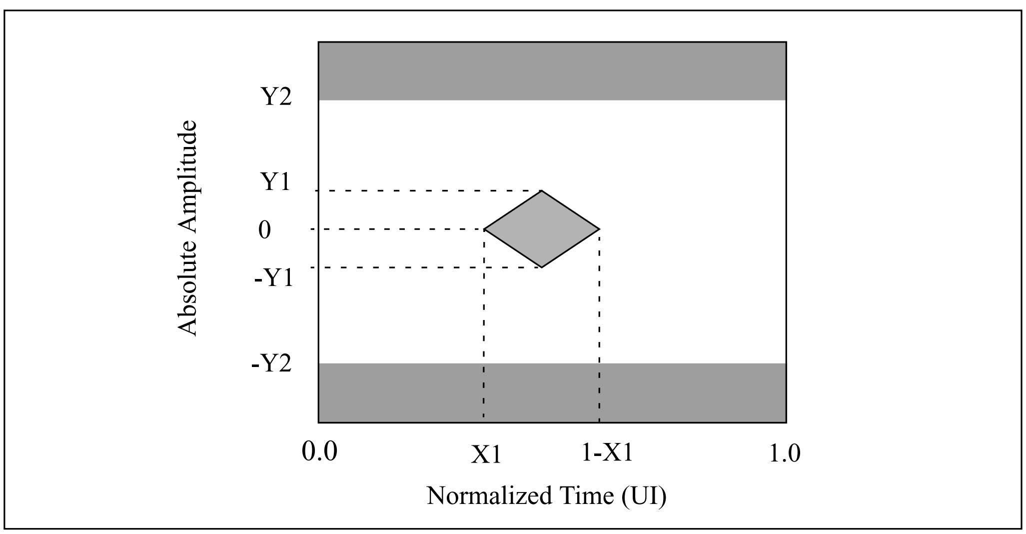

Figure 23 SFI Limiting Module Receiver Differential Output Compliance Mask at C'

Linear module test parameters are given by Table 20. Compliance methods for a linear module are given Appendix D.12.

Editor Notes

Trade off regions for SR and LR are under development.

An upper limit for dRN for low dWDP is under investigation.

An equation has been proposed for crosstalk for LRM

- dRNx <= sqrt[(0.041-0.022*dWDP)^2+0.0292^2]

Editor's note: The crosstalk rise/fall time may be closer to 30-32 ps. It should be based on the min rise/fall from the host ASIC Tx as measured through a minimum loss host channel and host compliance test board.

The dRN values are currently for module noise only. Inclusion of TP3 tester noise in the test conditions and the corresponding limits is being considered.

The crosstalk rise/fall time may be closer to 30-32 ps. It should be based on the min rise/fall from the host ASIC Tx as measured through a minimum loss host channel and host compliance test board.

Table 20 SFP+ Linear Module Receiver Specifications at C'

Parameters - C	*Symbol*	*Conditions*	*Min*	*Target*	*Max*	*Units*
Relative Noise SR Links wihout crosstalk	dRN	See D.11.1			TBD equation	RMS
Relative Noise LR Links wihout crosstalk					TBD equation	
Relative Noise LRM Links wihout crosstalk					0.041-0.022*dWDP	
Relative Noise SR Links with crosstalk	dRNx	See D.11.1			TBD equation	RMS
Relative Noise LR Links with crosstalk					TBD equation	
Relative Noise LRM Links with crosstalk					TBD equation	
Difference Waveform Distortion Penalty	dWDP	See 1 and D.12.2			1.5	dB
Differential Voltage Modulation Amplitude	VMA	See 2	180		600	mV
Crosstalk source rise/fall time (20%-80%)	Tr/Tf	See 3 and D.12.1		35		ps

1. Defined with reference receiver with 14 T/2 spaced FFE taps and 5 T spaced DFE taps.
2. Editor's note: LR minimum VMA is under study.
3. For dRNx compliance test condition. Crosstalk is not used for dRN.

Appendix D.12.1 defines dRN and dRNx. dRN is defined without crosstalk in the test system. dRNx is defined with crosstalk.

The limits for dRN and dRNx are functions of measured dWDP for the module, expressed in optical decibels. An example of the trade off for LRM between the parameters is shown in Figure 24. To pass, both dRN and dRNx must be below their respective limit lines.

dWDP and dRN must meet the specifications in Table 20 for each TP3 test condition for which compliance is required. For example, if compliance is required for LRM, the module must meet specifications under the six test conditions specified in IEEE Std 802.3 68.6.9.

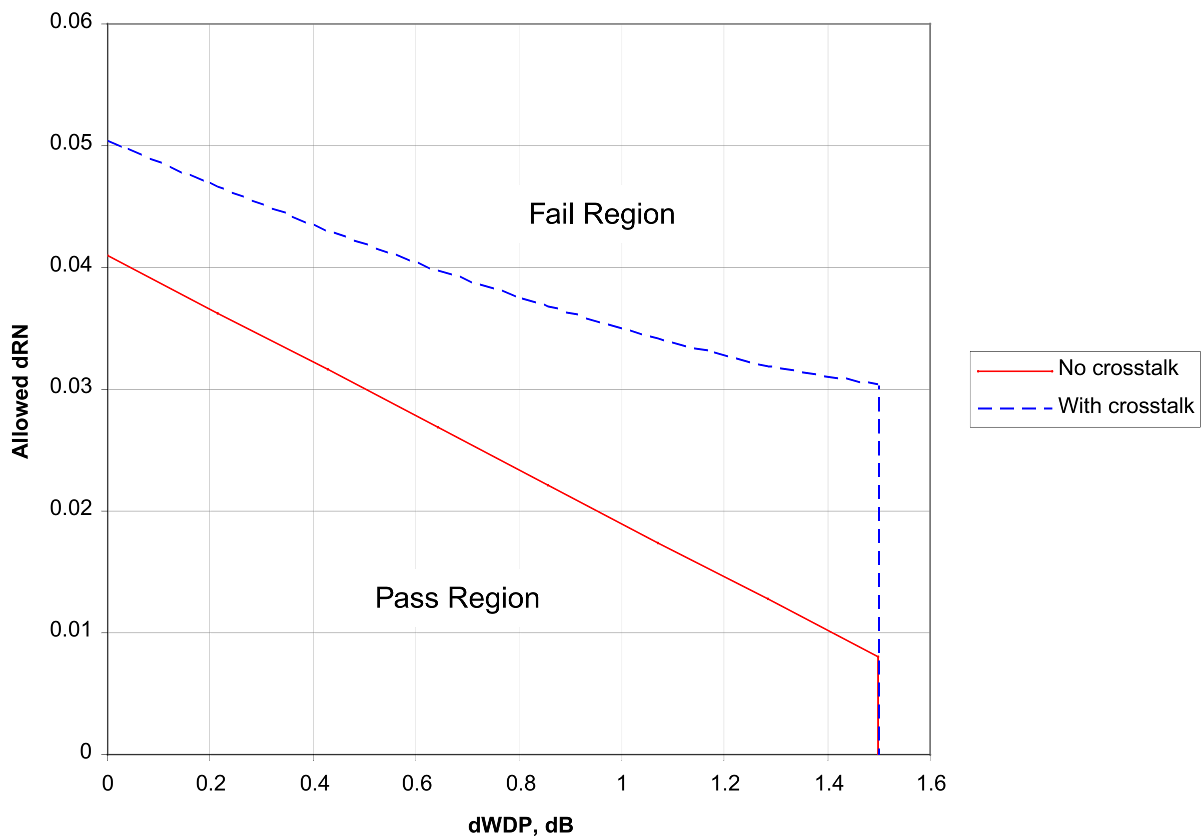

Figure 24 LRM example trade off between dRN vs. dWDP and dRNx vs. dWDP

CHAPTER 4: SFP+ 2-WIRE INTERFACE

4.1 INTRODUCTION

The SFP+ management interface is a two-wire interface, similar to I2C. SFP+ management memory map is based on SFF-8472. Nomenclature for all registers more than 1 bit long are MSB-LSB.

4.2 2-WIRE ELECTRICAL SPECIFICATIONS

The SFP+ 2-wire interface is based on Low Voltage TTL (LVTTL) operating with a supply of 3.3V ± 5% and the specifications are given in Table 21. This specification ensures compatibility between host masters and SFP+ SCL/SDA lines and compatibility with I^2C. All voltages are referenced to VeeT.

Table 21 2-Wire Interface Electrical Specifications

Parameter	Symbol	Min.	Max.	Unit	Conditions
Host 2-wire Vcc	Vcc_Host_2w	3.14	3.46	V	
SCL and SDA	V_{OL}	0.0	0.40	V	Rp2w[1] pulled to host_2w_Vcc, measured at host side of connector.
	V_{OH}	host_2w_Vcc - 0.5	host_2w_Vcc + 0.3	V	Rp2w[1] pulled to host_2w_Vcc, measured at host side of connector.
SCL and SDA	V_{IL}	-0.3	VccT*0.3	V	
	V_{IH}	VccT*0.7	VccT + 0.5	V	
Input current on the SCL and SDA Pins	I_I	-10	10	µA	
Capacitance on SCL and SDA I/O pin	C_i [2]		14	pF	
Total bus capacitance for SCL and for SDA	C_b [3]		100	pF	At 400 kHz, 3.0 kΩ Rp2w, max At 100 kHz, 8.0 kΩ Rp2w, max
			290	pF	At 400 kHz, 1.1 kΩ Rp2w, max At 100 kHz, 2.75 kΩ Rp2w, max

1. Rp2w is the pull up resistor. Active bus termination may be used by the host in place of a pullup resistor. Pull ups can be connected to multiple power supplies, however the host board design shall ensure that no module pin has voltage exceeding module VccT/R + 0.5 V nor requires the module to sink more than 3.0 mA current.
2. C_i is the capacitance looking into the module SCL and SDA pins
3. C_b is the total bus capacitance on the SCL or SDA bus.

4.3 SFP+ 2-wire Timing Diagram

SFP+ 2-wire bus timing is shown in Figure 25. SFP+ AC specifications are given in Table 22.

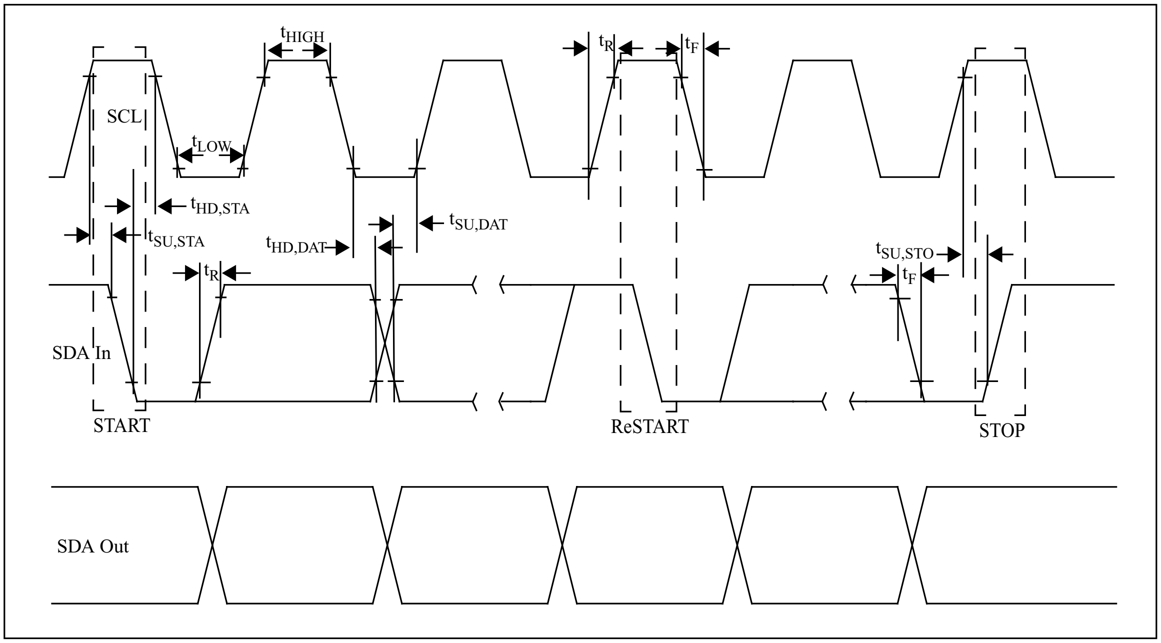

Figure 25 SFP+ Timing Diagram

Before initiating a 2-wire serial bus communication, the host shall provide setup time and hold times as defined by Table 22. The 2-wire serial interface addresses of the SFP+ module are 1010000x (A0h) and 1010001x (A2h).

Table 22 SFP+ 2-wire Timing Specifications

Parameter	*Symbol*	*Min.*	*Max.*	*Unit*	*Conditions*
Clock Frequency	f_{SCL}	0	400	kHz	
Clock Pulse Width Low	t_{LOW}	1.3		µs	
Clock Pulse Width High	t_{HIGH}	0.6		µs	
Time bus free before new transmission can start	t_{BUF}	20		µs	Between STOP and START
START Hold Time	$t_{HD,STA}$	0.6		µs	
START Set-up Time	$t_{SU,STA}$	0.6		µs	
Data In Hold Time	$t_{HD,DAT}$	0		µs	

Table 22 SFP+ 2-wire Timing Specifications

Parameter	Symbol	Min.	Max.	Unit	Conditions
Data In Set-up Time	$t_{SU,DAT}$	0.1		µs	
Input Rise Time (100 kHz)	$t_{R,100}$		1000	ns	From ($V_{IL,MAX}$ - 0.15) to ($V_{IH,MIN}$ + 0.15)
Input Rise Time (400 kHz)	$t_{R,400}$		300	ns	From ($V_{IL,MAX}$ - 0.15) to ($V_{IH,MIN}$ + 0.15)
Input Fall Time (100 kHz)	$t_{F,100}$		300	ns	From ($V_{IH,MIN}$ + 0.15) to ($V_{IL,MAX}$ - 0.15)
Input Fall Time (400 kHz)	$t_{F,400}$		300	ns	From ($V_{IH,MIN}$ + 0.15) to ($V_{IL,MAX}$ - 0.15)
STOP Set-up Time	$t_{SU,STO}$	0.6		µs	

4.4 MEMORY TRANSACTION TIMING

SFP+ memory transaction timings are given in Table 23.

Table 23 SFP+ Memory Specifications

Parameter	Symbol	Min.	Max.	Unit	Conditions
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold		500	µs	Maximum time the SFP+ module may hold the SCL line low before continuing with a read or write operation
Complete Single or Sequential Write	t_{WR}		40	ms	Complete (up to) 8 Byte Write
Endurance (Write Cycles)		10 k		cycles	70 °C

4.5 DEVICE ADDRESSING AND OPERATION

Serial Clock (SCL): The host supplied SCL input to SFP+ transceivers is used to positively edge clock data into each SFP+ device and negative edge clock data out of each device. The SCL line may be pulled low by an SFP+ module during clock stretching.

Serial Data (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain or open-collector driven and may be wire-ORed with any number of open-drain or open collector devices.

Master/Slave: SFP+ transceivers operate only as slave devices. The host must provide a bus master for SCL and initiate all read/write communication.

Device Address: Each SFP+ is hard wired at the device addresses A0h and A2h. See SFF-8472 for memory structure within each transceiver.

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods indicate a START or STOP condition. All addresses and data words are serially transmitted to and from the SFP+ in 8-bit words. Every byte on the SDA line must be 8-bits long. Data is transferred with the most significant bit (MSB) first.

START Condition: A high-to-low transition of SDA with SCL high is a START condition, which must precede any other command.

STOP Condition: A low-to-high transition of SDA with SCL high is a STOP condition.

Acknowledge: After sending each 8-bit word, the transmitter releases the SDA line for one bit time, during which the receiver is allowed to pull SDA low (zero) to acknowledge (ACK) that it has received each word. Device address bytes and write data bytes initiated by the host shall be acknowledged by SFP+ transceivers. Read data bytes transmitted by SFP+ transceivers shall be acknowledged by the host for all but the final byte read, for which the host shall respond with a STOP instead of an ACK.

Memory (Management Interface) Reset: After an interruption in protocol, power loss or system reset the SFP+ management interface can be reset. Memory reset is intended only to reset the SFP+ transceiver management interface (to correct a hung bus). No other transceiver functionality is implied.

1) Clock up to 9 cycles.
2) Look for SDA high in each cycle while SCL is high.
3) Create a START condition as SDA is high

Device Addressing: SFP+ devices require an 8 bit device address word following a start condition to enable a read or write operation. The device address word consists of a mandatory one zero sequence for the first seven most significant bits Table 24. This is common to all SFP+ devices.

Table 24 SFP+ Device Address

1	0	1	0	0	0	1 or 0	R/W bit
MSB							LSB

The eighth bit of the device address is the read/write operating select bit. A read operation is initiated if this bit is set high and a write operation is initiated if this bit is set low.

4.6 READ/WRITE FUNCTIONALITY

The methods for reading from and writing to the two different SFP+ addresses A0h and A2h are described in this section. They are identical for the two different addresses except that the appropriate address is used for each read and write. For simplicity in the figures the address is labelled 101000x where the x is 0 for the A0h address and 1 for the A2h address. Note that the address here is only seven bits. In order to complete the full 8 bit byte a one or zero is added to the end of the address depending on whether a read or a write operation is taking place.

4.6.1 SFP+ MEMORY ADDRESS COUNTER (READ AND WRITE OPERATIONS)

SFP+ devices maintain two internal data word address counters one for each address. These counters contain the last address accessed during the latest read or write operation, incremented by one. The address counter is incremented whenever a data word is received or sent by the transceiver. This address stays valid between operations as long as SFP+ power is maintained. The address “roll over” during read and write operations is from the last byte of the 128 byte memory page to the first byte of the same page.

4.6.2 READ OPERATIONS (CURRENT ADDRESS READ)

A current address read operation requires only the device address read word (10100001 or 10100011) be sent, Figure 26. Once acknowledged by the SFP+, the current address data word is serially clocked out. The host does not respond with an acknowledge, but does generate a STOP condition once the data word is read.

		< ---- SFP+ ADDRESS --->																		
HOST	START	MSB						LSB	READ										NACK	STOP
		1	0	1	0	0	0	x	1	0	x	x	x	x	x	x	x	x	1	
SFP+										ACK	MSB							LSB		
											<------ DATA WORD ------>									

Figure 26 SFP+ Current Address Read Operation

4.6.3 READ OPERATIONS (RANDOM READ)

A random read operation requires a “dummy” write operation to load in the target byte address Figure 27. This is accomplished by the following sequence: The target 8-bit data word address is sent following the device address write word (10100000 or 10100010) and acknowledged by the SFP+. The host then generates another START condition (aborting the dummy write without incrementing the counter) and a current address read by sending a device read address (10100001 or 10100011). The SFP+ acknowledges the device address and serially clocks out the requested data word. The host does not respond with an acknowledge, but does generate a STOP condition once the data word is read.

		< ---- SFP+ ADDRESS --->								<--- MEMORY ADDRESS -->										< ---- SFP+ ADDRESS --->																		
HOST	START	MSB						LSB	WRITE		MSB							LSB		START	MSB						LSB	READ										NACK	STOP
		1	0	1	0	0	0	x	0	0	x	x	x	x	x	x	x	x	0		1	0	1	0	0	0	x	1	0	x	x	x	x	x	x	x	x	1	
SFP+										ACK									ACK										ACK	MSB							LSB		
																														<------ DATA WORD ------>									

Figure 27 SFP+ Random Read

4.6.4 Read Operations (Sequential Read)

Sequential reads are initiated by either a current address read Figure 28 or a random address read Figure 29. To specify a sequential read, the host responds with an acknowledge (instead of a STOP) after each data word. As long as the SFP+ receives an acknowledge, it shall serially clock out sequential data words. The sequence is terminated when the host responds with a NACK and a STOP instead of an acknowledge.

		< ---- SFP+ ADDRESS --->																																				
HOST	START	MSB						LSB	READ										ACK									ACK									NACK	STOP
		1	0	1	0	0	0	x	1	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	1	
SFP+										ACK	MSB							LSB		MSB							LSB		MSB							LSB		
											<---- DATA WORD n ---->									<---- DATA WORD n+1 ---->									<---- DATA WORD n+x --->									

Figure 28 Sequential Address Read Starting at SFP+ Current Address

		< ---- SFP+ ADDRESS --->									<--- MEMORY ADDRESS -->										< ---- SFP+ ADDRESS --->																																				
HOST	START	MSB						LSB	WRITE		MSB							LSB		START	MSB						LSB	READ										ACK									ACK									NACK	STOP
		1	0	1	0	0	0	x	0	0	x	x	x	x	x	x	x	x	0		1	0	1	0	0	0	x	1	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	1	
SFP+										ACK									ACK										ACK	MSB							LSB		MSB							LSB		MSB							LSB		
																														<---- DATA WORD n ---->									<---- DATA WORD n+1 ---->									<---- DATA WORD n+x ---->									

Figure 29 Sequential Address Read Starting with Random SFP+ Read

4.6.5 WRITE OPERATIONS (BYTE WRITE)

A write operation requires an 8-bit data word address following the device address write word (10100000 or 10100010) and acknowledgement Figure 30. Upon receipt of this address, the SFP+ shall again respond with a zero (ACK) to acknowledge and then clock in the first 8 bit data word. Following the receipt of the 8 bit data word, the SFP+ shall output a zero (ACK) and the host master must terminate the write sequence with a STOP condition for the write cycle to begin. If a START condition is sent in place of a STOP condition (i.e. a repeated START per the I^2C specification) the write is aborted and the data received during that operation is discarded. Upon receipt of the proper STOP condition, the SFP+ enters an internally timed write cycle, t_{WR}, to internal memory. The SFP+ disables it's management interface input during this write cycle and shall not respond or acknowledge subsequent commands until the write is complete. Note that I^2C "Combined Format" using repeated START conditions is not supported on SFP+ write commands.

		< ---- SFP+ ADDRESS --->									<--- MEMORY ADDRESS -->									<-------- DATA WORD ------>									
HOST	START	MSB						LSB	WRITE		MSB							LSB		MSB							LSB		STOP
		1	0	1	0	0	0	x	0	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	
SFP+										ACK									ACK									ACK	

Figure 30 SFP+ Write Byte Operation

4.6.6 WRITE OPERATIONS (SEQUENTIAL WRITE)

SFP+ shall support up to an 8 sequential byte write without repeatedly sending SFP+ address and memory address information. A “sequential” write is initiated the same way as a single byte write, but the host master does not send a stop condition after the first word is clocked in. Instead, after the SFP+ acknowledges receipt of the first data word, the host can transmit up to seven more data words. The SFP+ shall send an acknowledge after each data word received. The host must terminate the sequential write sequence with a STOP condition or the write operation shall be aborted and data discarded. Note that I2C “combined format” using repeated START conditions is not supported on SFP+ write commands.”

.

		< ---- SFP+ ADDRESS --->									<--- MEMORY ADDRESS -->									<------ DATA WORD 1 ------>									<------ DATA WORD 2 ------>									<------ DATA WORD 3 ------>									<------ DATA WORD 4 ------>									
HOST	START	MSB						LSB	WRITE		MSB							LSB		MSB							LSB		MSB							LSB		MSB							LSB		MSB							LSB		STOP
		1	0	1	0	0	0	x	0	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	
SFP+										ACK									ACK									ACK									ACK									ACK									ACK	

Figure 31 SFP+ Sequential Write Operation

4.6.7 WRITE OPERATIONS (ACKNOWLEDGE POLLING)

Once the SFP+ internally timed write cycle has begun (and inputs are being ignored on the bus) acknowledge polling can be used to determine when the write operation is complete. This involves sending a START condition followed by the device address word. Only if the internal write cycle is complete shall the SFP+ respond with an acknowledge to subsequent commands, indicating read or write operations can continue.

APPENDIX A: SFI CHANNEL RECOMMENDATION (INFORMATIVE)

A.1 SFI CHANNEL GENERAL RECOMMENDATIONS

The purpose of the recommended SFI channel is to provide guidelines for host designers. The recommended SFI host channel consists of PCB traces, Vias, and the 20 position enhanced connector defined by SFF-8083. The PCB traces are recommended to meet 100 ±10 Ω differential impedance with nominal 7% differential coupling.

A.2 SFI CHANNEL TRANSFER RECOMMENDATIONS

The SFI maximum channel loss budget is 8.5 dB allocated as shown in Table 25.

Table 25 SFI Interconnect Budget

Parameter	*Symbol*	*Conditions*	*Min*	*Max*	*Units*
Channel Loss Including Connector measured with Host Compliance Board C.2	- SDD21	at 5.5 GHz, see 1	1.5	6.0	dB
Margin for Channel Crosstalk and Reflection				2.5	dB
Total Channel Budget				8.5	dB
1.Maximum channel loss include ripple.					

To mitigate multiple reflections, SFI also recommends a minimum channel insertion loss. This requirement for both a minimum and maximum channel insertion loss results in a mask that is shown approximately by Figure 32.

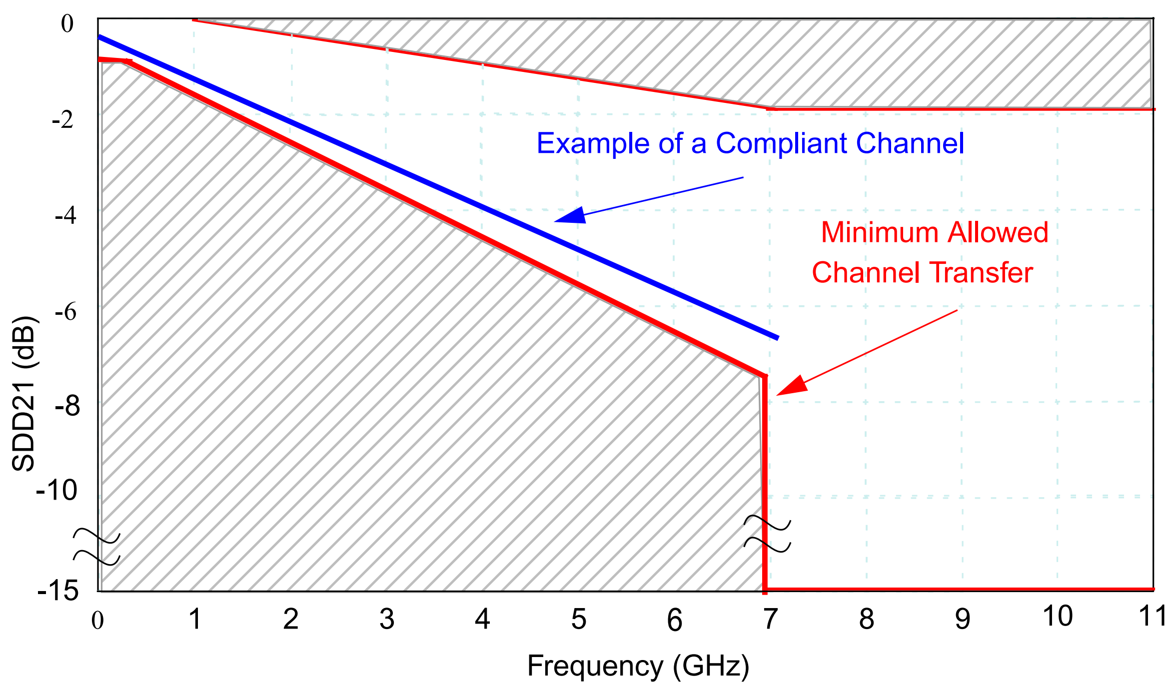

Figure 32 Example of SFI Recommended Channel

The minimum channel transfer SDD21 (maximum loss) mask contour is given by:

$$SDD21(dB) = (-0.1 - 0.78 \times \sqrt{f} - 0.74 \times f) \qquad \text{f from 0.25 to 7 GHz}$$

$$SDD21(dB) = -15 \qquad \text{f from 7 to 11.1 GHz}$$

variable *f* (frequency) is in GHz.

The SFI channel minimum insertion loss is given by.

$$SDD21(dB) = \frac{1}{3} \times (1 - f) \qquad \text{f from 1 GHz to 7 GHz}$$

$$SDD21(dB) = -2 \qquad \text{f from 7 GHz to 11.1 GHz}$$

where the variable *f* (frequency) is in GHz.

Please see SFF INF-8077i for differential S-parameters measurements and conversions.

A.3 SFI CHANNEL RETURN LOSS RECOMMENDATIONS

The reflection coefficients, SDD11 and SDD22, of the SFI channel are recommended to meet the following equations:

$$SDDxx(dB) \le -10 \qquad \text{f from 0.01 to 7 GHz}$$

$$SDD11(dB) \le -10 + 25Log_{10}\left(\frac{f}{7}\right) \qquad \text{f from 7 to 15 GHz}$$

where variable *f* (frequency) is in GHz.

The SFI recommended channel is measured with the ASIC removed and measured with the host compliance board of section C.2. SDD11 and SDD22 are measured by connecting 4 ports network analyzer to the ASIC pads and the SMA connectors on the host compliance test board.

Editor Notes
The equation for channel return loss is under study.

A.4 SFI CHANNEL RIPPLE RECOMMENDATIONS

SFI channel ripple is defined as the difference between the measured insertion loss (SDD21m) and the fitted insertion loss (SDD21f) and both are in dB magnitude:

$$Ripple(dB) = SDD21_m - SDD21_f$$

The channel ripple magnitude should conform to the equation:

$$|Ripple(dB)| \le 0.15 + 0.1 \times f$$

where the variable *f* (frequency) is in GHz. The above equation must be satisfied over the frequency range of 0.25 GHz to 5.5 GHz.

SFI channel ripple amount must be met over the frequency range of 0.25 GHz to 5.5 GHz. $SDD21_m$ is the measured channel differential insertion loss. $SDD21_f$ is the fitted channel differential insertion loss and is given by

$$SDD21_F = [-a - b \times \sqrt{f} - c \times f]$$

Where a, b, and c are determined by the least squares fit over the frequency range of 250 MHz to 5.5 GHz as defined below. Frequency steps should be of equal size and not greater than 50 MHz.

Measured data will provide a frequency vector, *f*, and gain vector, *G* defined by

$$G = 20 \times Log_{10}[|SDD21|]$$

Create an input vector array called X from frequency variable f

$$X = \begin{bmatrix} 1 & \sqrt{f0} & f0 \\ 1 & \sqrt{f1} & f1 \\ . & . & . \\ 1 & \sqrt{fn} & fn \end{bmatrix}$$

Next calculate the coefficient vector using matrix math

$$C = [X^T \times X]^{-1} X^T \times G$$

Where the calculated coefficient values are given by

- a = -C(1)
- b = -C(2)
- c = -C(3).

APPENDIX B: SFI ASIC/SERDES SPECIFICATION (INFORMATIVE)

B.1 INTRODUCTION

SFI ASIC/SerDes specifications are informative. SFI ASIC/SerDes Transmitter specifications at reference point A are given in B.2. SFI ASIC/SerDes Receiver specifications at reference point D are given in B.3. ASIC/SerDes meeting the specifications in this appendix when used with the recommended channel of Appendix A: are expected to meet the host specifications at B 3.5.1 and C 3.5.2, however any implementation that meets these host specifications is a compliant SFP+ implementation, independent of whether the ASIC/SerDes and/or channel meet the specifications in Appendix A: and this appendix.This allows flexibility between channel and SerDes performances and costs.

B.2 SFI ASIC/SERDES TRANSMITTER OUTPUT SPECIFICATIONS AT A (INFORMATIVE)

The SFI driver is based on low voltage high speed driver logic with a nominal differential impedance of 100 Ω. The SFI transmitter electrical specifications at reference point A are given in Table 26. The source must provide both differential and common mode termination for quality signal termination and low EMI.

Pre-compensation such as de-emphasis may be required to mitigate data dependent jitter at compliance point B.

All parameters at A are measured with the ASIC/SerDes Test Board as shown in C.1.3.

Editor Notes

changes to relax the Output AC common mode voltage specification is under consideration.

Table 26 SFI ASIC/SerDes Transmitter Output Electrical Specifications at A

Parameter - A	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Differential Output Voltage	V_{diff}				see 1	mV (p-p)
Termination Mismatch at 1 MHz	ΔZ_M	See D.15, Figure 18			5	%
Single Ended Output Voltage Range	Vcm		-0.3		4.0	V
Output Rise and Fall time (20% to 80%)	Tr,Tf	see 2	24			ps
Output AC Common Mode Voltage		See D.13			7.5	mV (RMS)
Differential Output S-parameter [3]	SDD22	0.01-2.8 GHz			-12	dB
		2.8-11.1 GHz			see 4	dB
Common Mode Output S-parameter [5]	SCC22	0.01-4.74 GHz			-9	dB
		4.74-11.1 GHz			see 4	dB

1.Host ASIC output must be set in combination of host channel to meet Y1 and Y2 levels of Table 12.
2. Measured with an OMA test pattern. Use of 4 1's and 4'0 sequence in the PRBS 9 is an acceptable alternative.
3. Reference differential impedance is 100 Ω
4. Reflection coefficent is given by equation Sxx22(dB)= -8.15 + 13.33 Log_{10}(f/5.5), with f in GHz.
5. Reference common mode impedance is 25 Ω

Jitter specifications at A are not provided, the host transmitter in conjunction with the host SFP+ channel must deliver jitter specifications as given by reference point B, Table 12.

B.3 SFI ASIC/SerDes Receiver Input Specifications at D (Informative)

SFI ASIC/SerDes receiver electrical specifications are given in Table 27 and measured at reference point D. All specifications at D are measured with the SerDes on a DUT board C.1.3. The nominal receiver input impedance is 100 Ω differential. The load must provide differential termination and avoid significant differential to common mode conversion for high quality signal termination and low EMI, as given by Table 27.

Table 27 SFI ASIC/SerDes Receiver Electrical Input Specifications at D

Parameter - D	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Differential Input Voltage for Limiting Host	Vdiff	see 1			850	mV (p-p)
Differential Input Voltage for Linear Host	VMA				600	mV
AC Common Mode Voltage		See D.13			12.5	mV (RMS)
Differential Input S-parameter [2]	SDD11	0.01-2.8 GHz			-12	dB
		2.8-11.1 GHz			see 3	dB
Differential to Common Mode Input Conversion S-parameter [4]	SCD11	0.01-11.1 GHz			-15	dB

1. Maximum value represents maximum input level to be tolerated by receiver.
2. Reference differential impedance is 100 Ω
3. Return Loss given by equation SDD11(dB)= -8.15 + 13.33 Log_{10}(f/5.5), with f in GHz.
4. The test set common mode reference impedance is 25 Ω.

The necessary jitter performance at D is to be determined by the implanter based on the specifications at C.

APPENDIX C: APPLICATION REFERENCE BOARDS (NORMATIVE)

In order to provide test results that are reproducible and easily measured SFP+ has defined 3 test cards that have SMA interfaces for easy connection to test equipment. One is designed for mounting ASICs, one for insertion into a host, and one for inserting SFP+ modules. Specifications in this document are defined at the SMA interfaces. This appendix describes these test cards in detail. The reference test boards objectives are:

- Satisfy the need for interoperablity at the electrical level.
- Allow for independent validation of ASIC/SerDes, host, and Module.
- The PCB traces are targeted at 100 Ω differential impedance with nominal 7% differential coupling.

Testing compliance to specifications in a high-speed system is delicate and requires thorough consideration. Using a common Host Test Board that allows predictable, repeatable and consistent results among system vendors will help to ensure consistency and true compliance in the testing of Host.

C.1 COMPLIANCE TEST BOARD

Compliance test boards are made of manufacturable length of PCB trace with specific properties for construction of the Host Compliance Test Board, the Module Compliance Test Board, and the ASIC/SerDes Test Board. Compliance test boards are intended to ease building practical test boards with non-zero loss. SFI specifications incorporate the effect of non-zero loss reference test board, which improve the return loss and slightly slows down edges.

C.1.1 HOST COMPLIANCE BOARD LOSS

The recommended response of the Host Compliance Test Board PCB excluding the SFP+ connector is given by.

$$SDD21(dB) = (-0.02 - 0.073 \times \sqrt{f} - 0.088 \times f)$$ from 0.25 to 11.1 GH

variable *f* (frequency) unit is in GHz. Over the range of frequencies specified any discrepancy between measured insertion loss and the specified SDD21(dB) shall be +/-15% insertion loss in dB or +/-0.1 dB, whichever larger. The channel transfer characteristic is shown approximately in Figure 33.

Editor Notes

SDD21 loss equation is under study and based on early measurements results of the compliance boards the loss for the PCB trace need to be increased by about 35% to meet practical board construction.

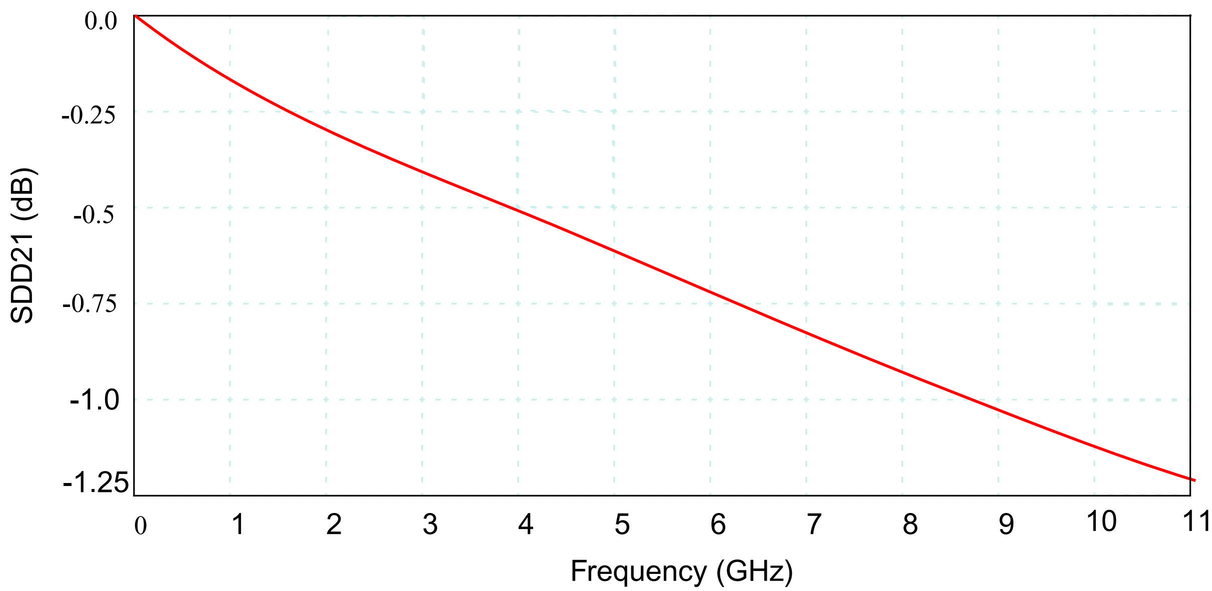

Figure 33 Host Compliance Test Board Loss

SFP+ connector response is defined by SFF-8083:

C.1.2 MODULE COMPLIANCE TEST BOARD LOSS

The recommended response of the Module Compliance Board PCB excluding the SFP+ connector is given by:

$$SDD21(dB) = (-0.01 - 0.0365 \times \sqrt{f} - 0.044 \times f) \text{ from 0.25 to 11.1 GHz}$$

variable *f* (frequency) unit is in GHz. Over the range of frequencies specified any discrepancy between measured insertion loss and the specified

SDD21(dB) shall be <+/-15% insertion loss in dB or +/-0.1 dB, whichever larger. The channel transfer loss is shown approximately in Figure 34.

> **Editor Notes**
>
> SDD21 loss equation is under study and based on early measurements results of the compliance boards the loss for the PCB trace needs to be increased by about 35% to meet practical board construction.

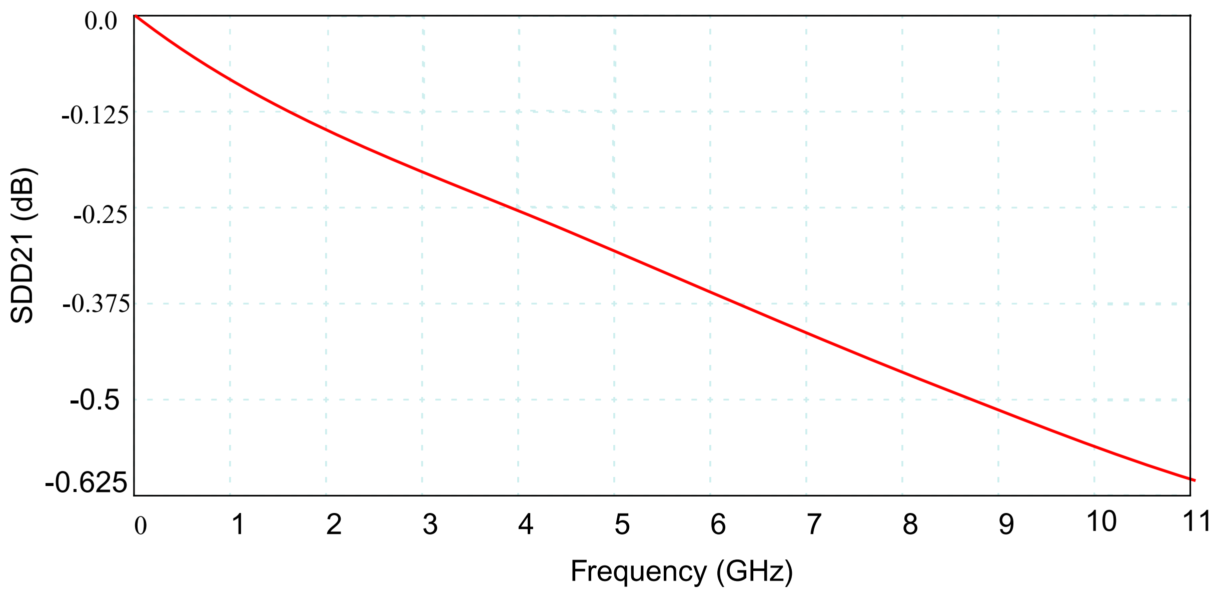

Figure 34 Module Compliance Test Board Loss

SFP+ connector response is defined by SFF-8083.

C.1.3 ASIC/SERDES TEST BOARD LOSS

The recommended response of the ASIC/SerDes test Board PCB is given by:

$$SDD21(dB) = (-0.01 - 0.0365 \times \sqrt{f} - 0.044 \times f) \text{ from 0.25 to 11.1 GHz}$$

variable *f* (frequency) unit is in GHz. Over the range of frequencies specified any discrepancy between measured insertion loss and the specified SDD21(dB) shall be < +/-15% of the dB values. The channel transfer loss drawn by an approximate diagram is shown in Figure 34.

C.2 HOST COMPLIANCE TEST BOARD

Host Compliance Test Board provided courtesy of Spirent Communication.

Editor Notes

The final board layout files full Gerber will be put on the SFF website.

C.2.1 HOST COMPLIANCE TEST BOARD MATERIAL AND LAYER STACK-UP

Host Compliance Test Board stack-up shown in Figure 35 is based on Roger4350B/ FR4-6 with six layers. The board is compliant with requirements of SFF-8432.

1. Top Layer	Signal	0.5 oz Cu + Plating
6.6 mils Rogers 4350B		
2. Layer	Ground	0.5 oz Cu
5.5 mils FR4-6		
3. Layer	Signal 1	0.5 oz Cu
7 mils FR4-6		
4. Layer	Signal 2	0.5 oz Cu
0.0055" FR4-6		
5. Layer	Power	0.5 oz Cu
0.066" Rogers 4350B		
6. Bottom Layer	Signal	0.5 oz Cu + Plating

Figure 35 Host Compliance Test Board stack-up

C.2.2 HOST COMPLIANCE TEST BOARD PARTLIST

The host compliance test board part list is given below.

Table 28 Host Compliance Test Board Part List

Qty	*RefDes*	*Value*	*Description*
2	C5, C6	0.1 UF	CAP 0.1UF 10% X7R 10V 0402 SMT LFR
3	D1, D2, D3	GREEN	LED SINGLE GREEN 120 DEG 0603 SMT LFR
2	D4, D5	Blue	LED SINGLE BLUE 120 DEG 0603 SMT LFR
1	J3	Conn3	LED SINGLE BLUE 120 DEG 0603 SMT LFR
4	J2, J3, J4, J5	EDGE SMA	CON SMA JACK R/A 50 OHM 18GHZ GOLD LFR - Rosenberger PN# 32K243-40ME3
1	J6	CONN1X3P	CON HDR 1X3 100MIL PITCH LOCKING THT LFR - Molex PN# 22-23-203
5	R1, R2, R3, R4, R5	1.0 KΩ	RES 1.00K 1% 1/10W 0603 SMT LFR
1	SW1	SPST	SWT DIP SWITCH 4POS SMT LFR - ITT Cannon PN# TDA04H0SB1

C.2.3 GERBER FILE AND S-PARAMETER MEASUREMENTS

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Editor Notes

The final board layout files full Gerber will be put on the SFF website.

C.2.4 SCHEMATIC OF HOST COMPLIANCE TEST BOARD

Schematic of host compliance test board is shown in Figure 36.

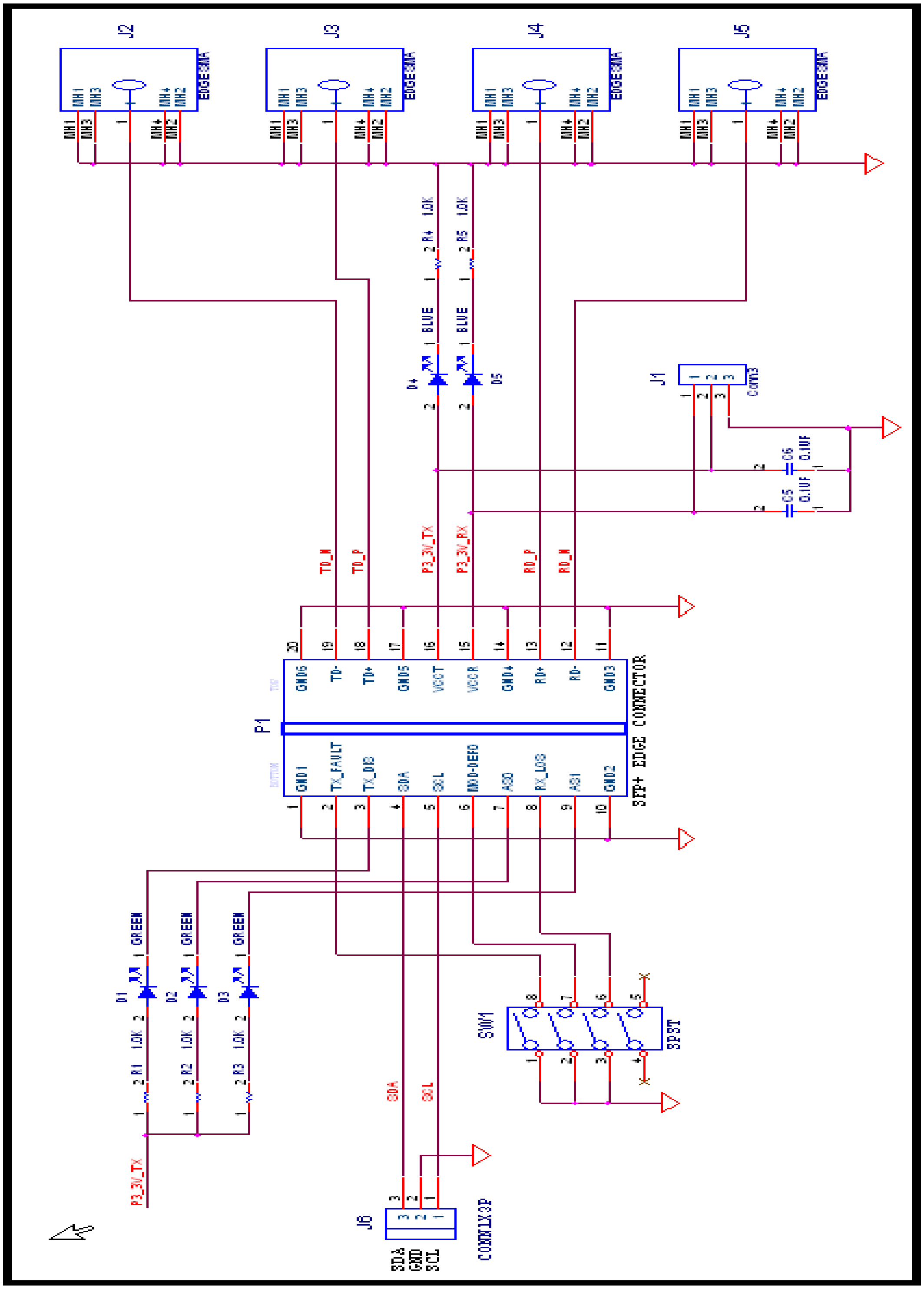

Figure 36 Host Compliance Test Board

C.3 Module Compliance Test Board

The Module Compliance Test Board allows predictable, repeatable and consistent results among module vendors and will help to ensure consistency and true compliance in the testing of modules. Module Compliance Test Board provided courtesy of Broadcom Corporation.

C.3.1 Module Compliance Test Board Material and Layer Stack-up

Module Compliance Test Board stack-up shown in Figure 37 is based on ten layers Rogers 4350B / FR4-6 material.

1. Top Layer	Signal	0.5 oz Cu + Plating
6.6 mils Rogers 4350B		
2. Layer	Gnd	0.5 oz Cu
15 mils FR4-6		
3. Layer	Gnd	1 oz Cu
3 mils FR-4		
4. Layer	VccR	1 oz Cu
3 mils FR4-6		
5. Layer	Gnd	1 oz Cu
3 mils FR4-6		
6. Layer	VccT	1 oz Cu
3 mils FR4-6		
7. Layer	Gnd	1 oz Cu
3 mils FR4-6		
8. Layer	Signal	1 oz Cu
15 mils FR4-6		
9. Layer	Gnd	0.5 oz Cu
6.6 mils Rogers 4350B		
10. Bottom Layer	Signal	0.5 oz Cu + Plating

Figure 37 Module Compliance Test Board stack up

C.3.2 SCHEMATIC OF HOST COMPLIANCE TEST BOARD

Schematic of module compliance test board is shown in Figure 38.

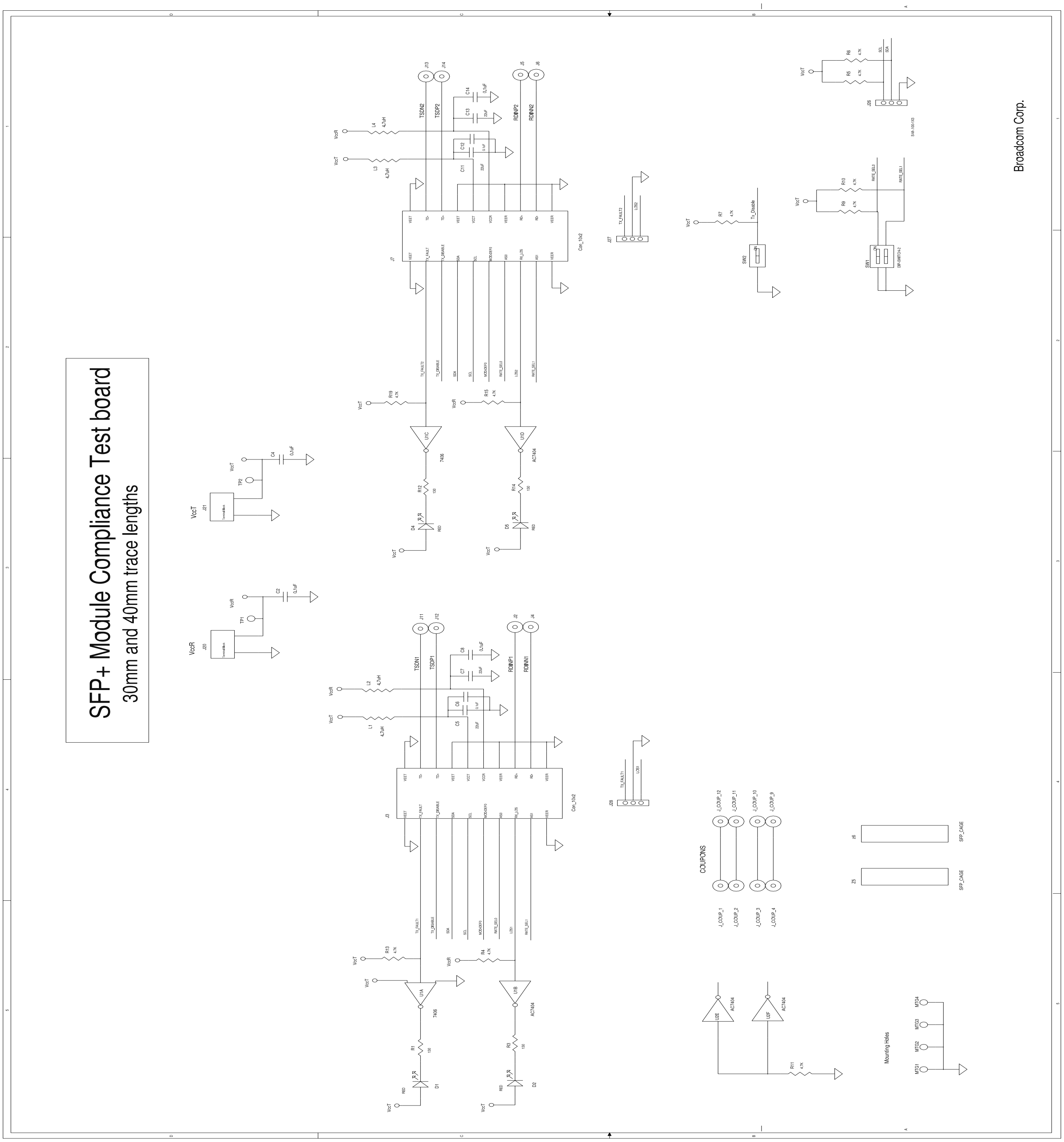

Figure 38 Schematic of module compliance test board

C.3.3 MODULE COMPLIANCE TEST BOARD PARTLIST TBD

Component part list for the SFP+ compliance test board is given below.

Table 29 SFP+ Module Compliance Test Board Part List

Qty	*RefDes*	*Value*	*Description*
6	C2, C4, C6, C8, C12, C14	0.1uF	Murata/GRM188R71C104MA01D
4	C5, C7, C11, C13	22 uF	Murata/GRM21BR60J226ME39K
4	D1, D2, D4, D5	RED	Panasonic/LNJ208R8ARA
12	J_COUP_2, J2, J_COUP_4, J4, J5,J6, J_COUP_9, J_COUP_11, J12, J14J_COUP_1, J_COUP_3, J_COUP_10, J11, J_COUP_12, J13	SMA	Huber&Suhner/92_SK-U50-0-3/199_NE
2	J3, J7	Con_10x2	Amp/1367073-2
2	J20, J21	Terminal Block	On-Shore-Tech/EDZ5002DS
3	J26, J27, J28	S-M-.100-1X3	Molex/22-10-2031
4	L1, L2, L3, L4	4.7 uH	Toko/A914BYW-4R7M
4	R1, R3, R12, R14	130 Ω	Walsin/WR06X131JTL
10	R4, R5, R6, R7, R9, R10, R11, R13, R15, R19	4.7 kΩ	Walsin/WR06X472JTL
1	SW1	DIP-SWITCH-2	Digi-key/CT2062-ND
1	SW2	sw_pb_ck-k	C&K/ET01MD1AVBE
1	U1	74AC04	Fairchild/530438-00
2	Z5, Z6	SFP_CAGE	Tyco/AMP/1489962-1

C.3.4 GERBER FILE AND S-PARAMETER MEASUREMENTS

Editor Notes

The final board layout files full Gerber will be put on the SFF website.

C.4 MEASUREMENT RESULTS OF MATED HOST AND MODULE COMPLIANCE TEST BOARDS (TBD)

It will include SDD21, SDD11, SCC11, SCC22, and SDD22. Also include crosstalk response.

APPENDIX D: TEST METHODOLOGY AND MEASUREMENT (NORMATIVE)

D.1 INTRODUCTION

This appendix defines metrics for SFP+ high-speed and power electrical interfaces and provides practical guidance for test implementation. Each parameter is defined in terms of a measurement procedure. The instruments for measurement are assumed to be ideal: accurate, precise, with infinite or defined bandwidth, zero or defined noise and so on. In practice, the necessary level of instrument performance and the approach to calibration and margining must be considered. Some guidance is given in the following sections.

All measurements are made differentially, with the exception of D.13 AC Common Mode Generation Test, D.15 Termination Mismatch, D.16 Module Power Supply Tolerance Filtering, and D.16 Power supply noise testing methodology.

D.2 EYE MASK COMPLIANCE

Editor Notes

Eye masks are currently defined at 1E-12 probability limits. All known practical measurement methods require some degree of jitter and noise breakdown and extrapolation (i.e., uncertainty) to evaluate 1E-12 compliance. Alternative probability limits are being considered, which could lead to associated changes in some mask coordinates and/or pass/fail criteria in chapter 3 and/or methodology in D.2.

This section defines what is meant by eye mask compliance and gives guidance for its determination. Mask templates and coordinates are given in subclauses in 3.5 SFP+ Host System Specifications and 3.6 SFP+ Module Specifications .

- The output being tested should comply over the range of operating conditions while the opposing direction traffic operates with the fastest edge rate and maximum allowed input signal strength.
- The pattern(s) for eye mask testing is according to the relevant optical standard(s).
- The opposite link data traffic for10GbE shall be as defined by IEEE 802.3 CL52.9 Pattern 1, Pattern 3, or valid 64B/66B data traffic.
- Traffic in the other direction (than the one being tested) must use an asynchronous clock.

Editor Notes

D0.5/AT33 says statistical significance of 10^-12 is not appropriate.

- Testing may include guard banding, extrapolation, or other methods, but must ensure that mask violations do not occur at a rate > 1E-12.
- AC coupling is required for testing the host output. The 3 dB corner frequency shall be set sufficiently low so that baseline wander does not affect the outcome of the measurement.
- All loads are specified at 100 Ω differential.
- Zero “0” and one “1” on the unit interval scale are defined by the eye crossing means at the average value (zero volts) of the signal. The average value might not be at the jitter waist.

A clock recovery unit (CRU) is used to trigger the scope for mask measurements as shown in Figure 39. The reference CRU has a high frequency corner bandwidth of 4 MHz and a slope of -20 dB/decade with peaking of 0.1 dB or less.

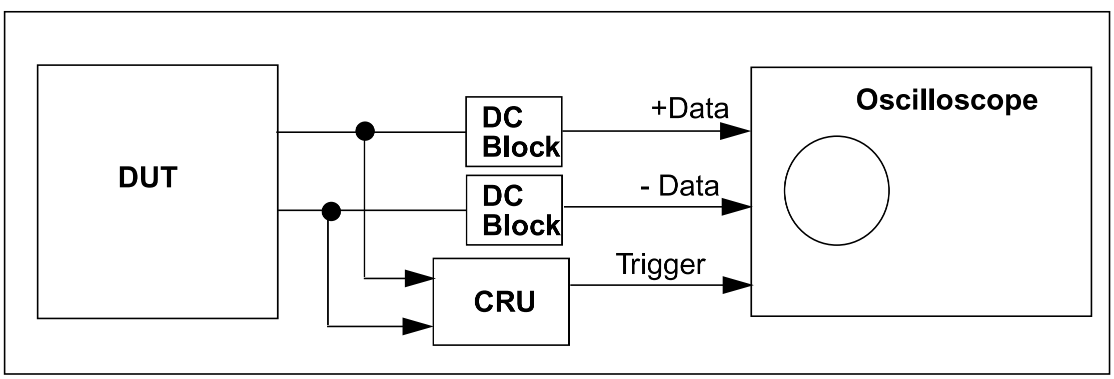

Figure 39 Eye mask measurement setup - block diagram.

D.3 DATA DEPENDENT JITTER (DDJ) AND PULSE WIDTH SHRINKAGE (PWS) MEASUREMENT

A high-resolution oscilloscope, time interval analyzer, or other instrument with equivalent capability may be used to measure DDJ. A repeating pseudo-random test pattern consisting of at least 511 bits (PRBS9) is used. For electrical jitter measurements, the measurement bandwidth is at least 12 GHz. If the measurement bandwidth affects the result, it can be corrected for by post-processing. However, a bandwidth above 12 GHz is expected to have little effect on the results.

DCD and Pulse Width Shrinkage (PWS) are components of DDJ.

Establish a crossing level equal to the average value of the entire waveform being measured. Synchronize the instrument to the pattern repetition frequency and average the waveforms or the crossing times sufficiently to remove the effects of random jitter and noise in the system. If the 511 bit pattern is used, there will be 128 positive-going transitions and 128 negative-going transitions. The mean time of each crossing is then compared to the expected time of the crossing, and a set of 256 timing variations is determined. DDJ is the range (max-min) of the timing variations. Keep track of the signs (early/late) of the variations. Note, it may be convenient to align the expected time of one of the crossings with the measured mean crossing.

The following Figure 40 illustrates the method. The vertical axis is in arbitrary units, and the horizontal axis is plotted in UI. The waveform is AC coupled to an average value of 0, therefore 0 is the appropriate crossing level. The rectangular waveform shows the ideal crossing times, and the other is the waveform with jitter that is being measured. Only 32 UI are shown (out of 511 if a 511 bit pattern is used). The waveforms have been arbitrarily aligned with ($\Delta t_2 = 0$) at 14 UI.

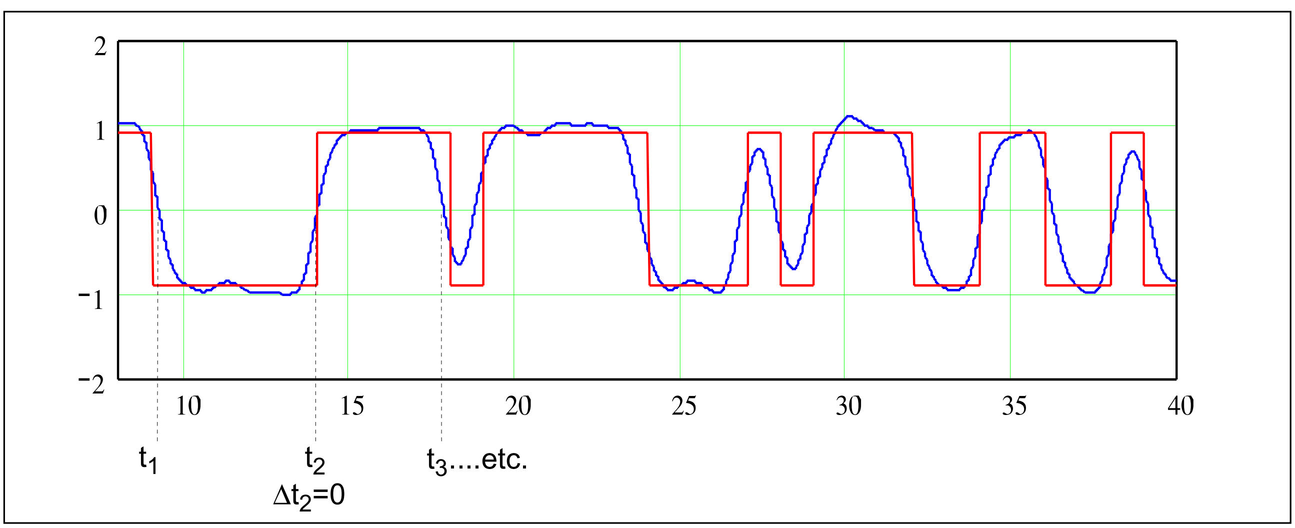

Figure 40 DDJ Test Method

DDJ is defined as

$$DDJ = max(\Delta t_1, \Delta t_2, \ldots \Delta t_n) - min(\Delta t_1, \Delta t_2, \ldots \Delta t_n)$$

Every edge, 1...n, in a complete repetition of the pattern is measured (n = 256 in a PRBS9 pattern).

PWS is determined as the difference between 1 UI and the minimum of all the differences between pairs of adjacent edges

$PWS = 1 - min(t_2-t_1, t_3-t_2, \ldots t_{n+1}-t_n)$

where t_2-t_1, etc. are expressed in UI. Note that the difference between the next edge in the repeating sequence, t_{n+1}, is also considered.

D.4 UNCORRELATED JITTER (UJ)

UJ as defined by IEEE 802.3 CL 68 is a measure of any jitter that is uncorrelated to the data stream. The definition and test procedure for UJ are identical to those defined in IEEE 802.3 CL 68.6.8 with following considerations:

- The host transmitter shall comply while the receiver is operating with asynchronous data and all other ports operating as in normal operation, including proper termination. The receive path input of the host system compliance test board is connected to a pattern generator and calibrated through a module compliance test board. The amplitude is set to the maximum value allowed by Y2 in Table 14 if the host is designed for limiting modules, and/or to the maximum value allowed for VMA in Table 16 if designed for linear modules. The rise and fall times measured through the compliance test board pair are equal to the minimum rise and fall time given in Table 18. The pattern for the crosstalk source is PRBS31.
- For purposes of this document the procedures defined for optical testing also applies to electrical testing. Optical terms (such as power) and units, such as in Figure 68-9 in IEEE 802.3, can be converted to corresponding electrical terms (such as voltage) and units, etc.
- The 4th-order Bessel-Thomson response is to be used only for optical measurements of UJ. UJ in the electrical domain is defined in a bandwidth of 12 GHz, unless specified by the application standard.

- PRBS9 is suitable as a test sequence for all applications unless specified otherwise.
- The bandwidth of the CRU is defined in IEEE 802.3 clause 68.6.8 or in the relevant standard for the application.

D.5 Deterministic, Random and Total Jitter

Using a dual-Dirac jitter model, FC-MJSQ (Fiber Channel - Methodologies for Jitter and Signal Quality Specification) defines extraction of jitter attributes from a cumulative distribution function, CDF, or bathtub curve that describes BER over the unit interval, UI. It's expected that the CDF provides accurate time values for CDF levels of 10^{-6} and 10^{-12}.

Editor Notes

The electrical jitter tolerance methodology ad hoc may provide a write up for the for measurement of jitter (DJ, TJ). Input in invited.

A dual-Dirac jitter model assumes the following. Jitter is a stationary phenomenon, i.e. measurement results for a given system for appropriate sample times are consistent. Jitter can be decomposed into two basic categories, random and deterministic. Random Jitter, RJ, follows a Gaussian distribution fully defined by the width, i.e. standard deviation, of the distribution. Deterministic Jitter, DJ, follows a bounded, i.e. finite, distribution. Only the low BER regions of the CDF away from the signal crossing points are of interest and need to be matched by the dual-Dirac model. For more on dual-Dirac jitter models see, “Jitter Analysis: The dual-Dirac Model, RJ/DJ, and Q-Scale” Agilent Technologies, June 21, 2005, publication 5989-3206EN.

FC-MJSQ Chapter 8 describes the extraction of jitter components, RJ and DJ and the calculation of total jitter, TJ. In FC-MJSQ Chapter 8 are additional assumptions that the test patterns used to generate the CDF have a transition density of 0.5 and do not generate signal pattern dependent effects at rates less than 10^{-12}.

FC-MJSQ uses terminology that is proprietary to particular mathematical software. Only generic terms are used in this document.

Total Jitter, TJ, used in this document is consistent with the Level 1 definition for TJ as described in FC-MJSQ where TJ is defined as the unit interval, UI, minus the jitter eye opening. TJ can be expressed as:

- TJ = UI - t_1, where t_1 is the jitter eye opening (eye-width) at the CDF = 10^{-12}.

In the above expression TJ is a peak-to-peak value.

Random Jitter, RJ, used in this document is consistent with the definition for RJ as described in FC-MJSQ where RJ is defined as a Gaussian function. RJrms is the standard deviation (1-sigma) value of the distribution. RJrms can be expressed as:

- RJ_{rms} = 0.2106 x $|t_1 - t_0|$ where t_0 is the jitter eye opening (eye-width) at the CDF = 10^{-6}.

Deterministic Jitter, DJ, used in this document is consistent with the Level 1 definition for DJ as described in FC-MJSQ where DJ is the time separation between two delta functions, half-magnitude Gaussian functions that represent RJ. In summary, DJ is derived by fitting the time separation between the delta functions to the CDF or bathtub curve that describes the BER over the unit interval. The expression for DJ is given as

- DJ = UI - t_0 - 8.93 x RJ_{rms}.

In the above expression DJ is a peak-to-peak value. The reader is cautioned that DJ as defined here is a term developed to fit the dual-Dirac model.

TJ can now be expressed as:

- TJ = UI - t1 = DJ + 13.68 RJrms.

In the above expressions units for DJ, UI, t_0, t_1, and RJrms can be in UI or ps.

D.6 Electrical compliance signal at B" for the SFP+ transmitter

Editor Notes

A test methodology for optical module transmitter compliance is under development.

D.7 TEST METHOD FOR A HOST RECEIVER FOR A LIMITING MODULE

Editor Notes

This test methodology for testing compliance of a host for limiting modules is still under development. The primary area of work is selecting the appropriate types and magnitudes of jitter within D.7.2 and D.7.3. The types and magnitudes must be representative of expected TP3 stresses and limiting module receiver properties.

The impact of crosstalk must be considered.

Other sub-clauses of D.7.5 may need to change in response to changes in D.7.2 and D.7.3 or to values in Chapter 3:.

D.7.1 INTRODUCTION

This clause provides guidance for jitter tolerance testing at the RX host compliance point C. Compliance is required with input jitter and vertical eye closure as specified respectively in Table 14 as given in Chapter 3:. Compliance is defined at the error rate(s) set by the appropriate optical standard.

FC-MJSQ and OIF-CEI both provide further information on definitions, setups, calibration and methods for stressed-eye jitter tolerance testing.

Editor Notes

D1.3/AT173 Readers are asked to recommend specific sections, otherwise we should remove the paragraph.

D.7.2 TEST EQUIPMENT & SETUP

A test source is used to continuously generate an appropriate test signal for application compliance. The test signal shall be appropriately conditioned within the guidelines outlined in D.7.3 to exhibit the appropriate jitter stress.

An RF attenuator or other output amplitude control of the test source may be required to set the vertical eye opening of the stressed eye.

The test signal has the characteristics specified in Table 13, and complies with any further specifications of 3.6.2. The test equipment shall have better than 20 dB return loss up to 12 GHz.

It is required that the receiver under test include a mechanism to allow measurement of BER performance.

D.7.3 Stressed-Eye Jitter Characteristics

he SFP+ specification in Table 14 places bounds on the expected jitter that needs to be tolerated as calibrated at point C". For limiting receiver application this jitter is expected to be predominantly non-equalizable. The jitter components consist of duty cycle distortion (DCD), random jitter (RJ), sinusoidal jitter (SJ), bounded uncorrelated jitter (BUJ), and other forms of periodic jitter (PJ). Additionally, non-equalizable jitter may also result after a limiting function is applied to equalizable ISI jitter.

This section describes required test signal characteristics along with considerations and suggested approaches for test signal generation. The test signal is generated by the functions shown in Figure 41 or by equivalent means. Figure 42 illustrates how the jitter parameters in Table 13 map to the jitter components in the stressed-eye test signal.

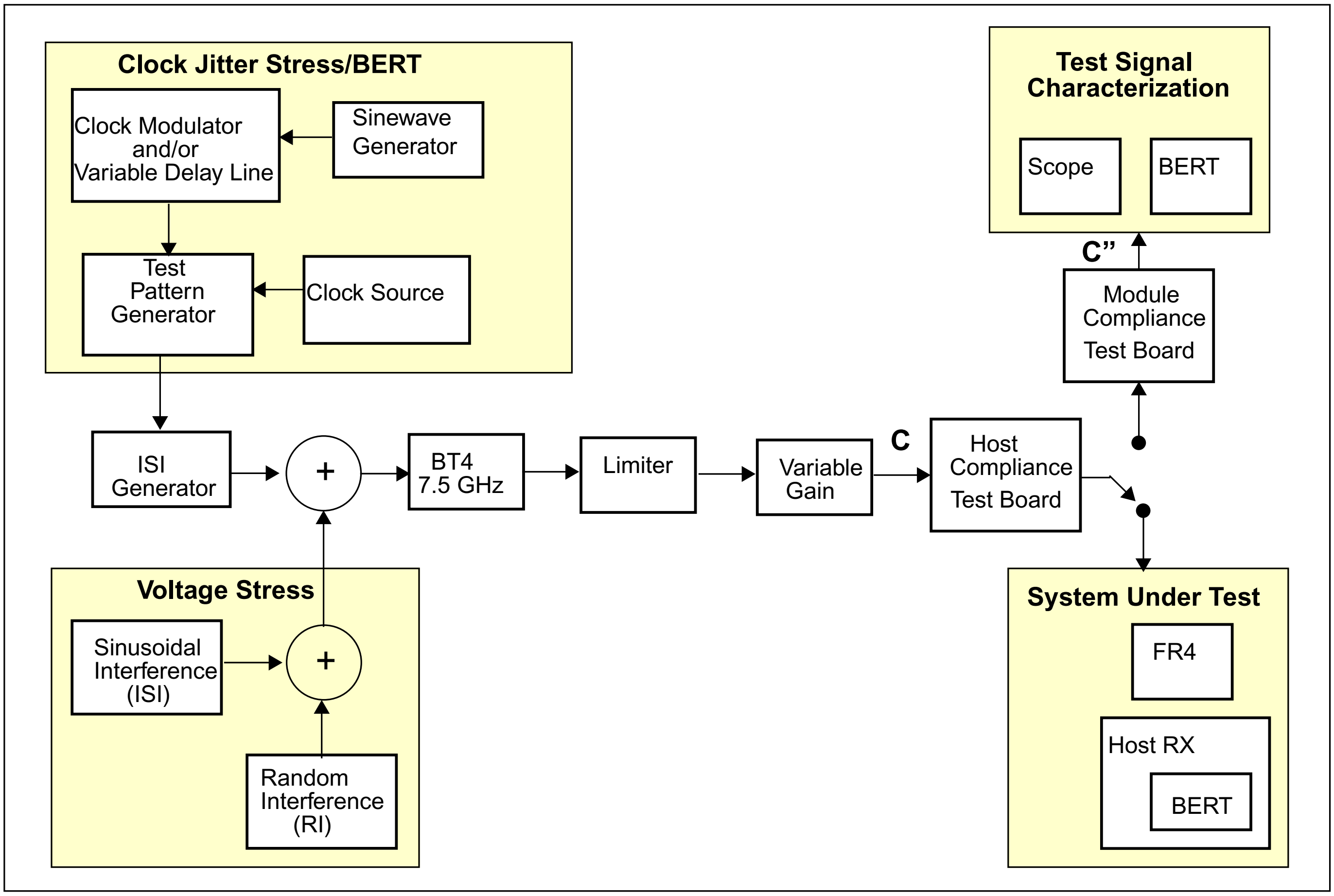

Figure 41 Sample Jitter Tolerance Test Configuration

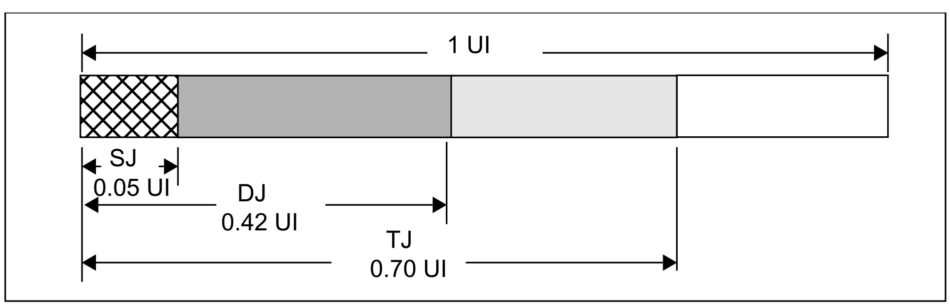

Figure 42 Partitioning of stressed eye jitter components

The 0.05 UI SJ component of DJ is defined for frequencies much higher than the CDR bandwidth (e.g. ~ 20 MHz). At lower frequencies the CDR must track additional applied SJ as detailed in the relevant specifications[1].

The balance of the DJ is comprised of a combination of the following forms of jitter: ISI jitter passed through a limiting function, and DCD.

Editor Notes

D1.3/AMCC69, 73 propose specifying the probability distribution function. Agreed in principle.

Editor Notes

D1.3/AT18 Readers are asked to compare DCD metrics from inbuilt scope algorithm and derived from averaged PRBS9 waveform.

The signal at C" shall have TBD UI PWS as defined by Table 14. Any DCD in the test shall not exceed 0.02 UI.

ISI jitter creation may be achieved through the use of a low pass filter, length of FR4 trace, length of coax cable or other equivalent method. It is required that this jitter be passed through a limiter function to ensure that the resulting jitter is not totally equalizable jitter. A suitable limiter function may be implemented using a discrete amplifier followed by an attenuator. In this scenario, the amplification function should have a minimum 3 dB bandwidth of 10 GHz. The attenuator is used to set the output amplitude to minimum and maximum values allowed by the eye mask of Figure 18.

A voltage stress before the limiter function is to be applied. This stress is comprised of a single tone sinusoidal interferer (SI) in the frequency range 100 MHz to 2 GHz and a broadband noise source (RI) with a minimum 6 GHz BW and minimum 7σ crest factor. It is the intent that this combination of voltage stress and limiting function introduce pulse-shrinkage jitter behavior. However no more than 20% of the DJ should be created by the sinusoidal interferer.

Editor Notes

Note 20% is under investigation.

1. At lower frequencies, additional sinusoidal jitter must be added to meet the jitter tolerance of relevant application. At any frequency TJ= (0.7UI- high frequency tolerance mask) + tolerance mask.

Jitter generation mechanisms for the pattern generator are typically based on phase modulation of the clock source, edge modulation of a variable delay line or a combination thereof.

Any approach that modulates or creates the appropriate levels and frequencies of the jitter components is acceptable.

D.7.4 CALIBRATION

Calibration of the test signal is to be performed using the guidelines for test setup in D.7.2 and illustrated in Figure 41. The aim of the calibration is to achieve a test signal exhibiting jitter stress in accordance with Table 14.

The test signal should be calibrated differentially into standard instrumentation loads. If complementary single-ended signals are used; they should be carefully matched in both amplitude and phase.

For improved visibility for calibration, it is imperative that all elements in the signal path (cables, DC blocks, etc.) have wide and flat frequency response as well as linear phase response throughout the spectrum of interest. Baseline wander and overshoot/undershoot should be minimized.

Jitter requirements are defined for a probability level of 1E-12. To calibrate the jitter, methods given in MJSQ and CEI are recommended. Given random jitter and the nature of the long test patterns, low probability jitter events will likely be present. It is recommended for jitter calibration that a technique that can accurately measure low probability events should be used to avoid overly stressful test conditions.

It is recommended that the actual compliance test pattern be used during calibration. For jitter stress calibration it is permissible, however, to use any appropriate test pattern which still results in the creation of a compliance test pattern with the appropriate jitter stress.

D.7.5 CALIBRATION PROCEDURE

The vertical eye opening should be set approximately to its minimum allowed level specified in Table 14.

With an applied calibration test pattern and no additional jitter stress applied; the intrinsic jitter of the test source due to intrinsic noise and finite bandwidth effects should be measured and calibrated. This jitter should be decomposed into DJ and TJ components according to the definition D.5.

SJ should be added until the DJ component of jitter increases by 0.05 UI above the measured reference level. This should be high frequency SJ well above the CDR bandwidth. The SJ frequency should be asynchronous with the data clock.

Next, additional DJ should be added as specified in D.7.3 with the FR4/filter etc. until at least 80% of the DJ has been created. The Sine Interferer amplitude should then be turned on and adjusted until the required level of DJ is achieved. The frequency of any Sine interferer should be asynchronous with the data clock.

Editor Notes

The 80% DJ is under investigation.

Once the required level of DJ has been achieved RI voltage stress should be added until the required value of TJ is achieved at a probability of $1E^{-12}$.

Low probability RJ from the SRS tester may be calibrated out in the TJ measurement.

If necessary, the vertical eye opening should be readjusted to its minimum allowed level.

A verification shall be made that any low probability vertical closure present occurs at a probability level of < $1E^{-12}$.

A compliant test signal exhibits data dependent pulse width shrinkage as specified in Table 14 or Table 17 as appropriate. Data dependent pulse width shrinkage is defined in D.3. This is measured with noise and clock-jitter sources turned off.

Care must be taken when characterizing the signal used to make receiver tolerance measurements. The intrinsic noise and jitter introduced by the test system (e.g. filters, oscilloscope and BERT) must be accounted for and controlled. If equipment imperfections affect the results materially, corrections such as RSS deconvolution of Gaussian noise and jitter should be used.

D.7.6 TEST PROCEDURE

Testing should be performed differentially through a Host Compliance Test Board (see C.2).

Using a test signal calibrated conforming to D.7.2 and calibrated as per D.7.5, operate the system with an appropriate compliance test pattern for the relevant application (10G Ethernet, 10GFC, or 10G Ethernet with FEC).

All signals and reference clocks that operate during normal operation shall be active during the test including the other host signal path in the duplex pair. The other signal path shall be asynchronous.

The sinusoidal jitter is stepped across frequency and amplitude range according to Figure 21 while monitoring the BER. The BER shall remain < $1E^{-12}$.

D.8 VOLTAGE MODULATION AMPLITUDE (VMA)

The definition and test procedure for VMA are identical to those defined in the OMA clause IEEE 802.3 CL 68.6.2 with consideration of these comments:

- For purposes of this document, the definitions and procedures apply to both optical and electrical signals. Optical terms (such as Optical Modulation Amplitude (OMA)) and units, such as in Figure 68-4, are converted to corresponding electrical terms (such as Voltage Modulation Amplitude (VMA)) and units, etc.
- The 4th-order Bessel-Thomson response is to be used only for optical measurements of OMA, such as calibration of an optical receiver test system. The bandwidth of the Bessel-Thomson response is called out in the relevant standard for the application. Electrical measurements of VMA do not require a Bessel-Thomson filter. The bandwidth of the measurement system is at least 3/T where T is the time at high or low (0000000011111111) gives approximately 4 GHz of bandwidth for this pattern at 10.3125 Gbd.
- VMA is defined with the optical signal (OMA) test pattern defined in IEEE 802.3 CL 68.6.1 (this is a subset of allowed patterns in IEEE 802.3 CL 52), or in the case of a non-802.3 application, a test pattern defined by relevant standard.
- An estimate of the OMA or VMA value is provided by the variable MeasuredOMA of IEEE Std 802.3aq 68.6.8.

D.9 RELATIVE NOISE (RN)

RN is a measure of reciprocal SNR for a signal. Generically,

$$RN = \frac{2 \times noise(RMS)}{(xMA)}$$

where for this document, xMA is OMA if an optical signal is being measured, or VMA if an electrical signal is being measured, and noise(rms) is measured on the same optical signal or electrical signal, respectively.

Important parts of the measurement procedure for RN can be found in clause IEEE Std. 802.3 CL 68.6.7 (LRM). Some comments:

- For purposes of this document, the definitions and procedures generally apply to both optical and electrical signals. Optical terms (such as power) and units can be converted to corresponding electrical terms (such as voltage) and units, etc.
- The test pattern defined for OMA in IEEE 802.3 CL 68, or other standard relevant for the application, shall be used regardless if the RN measurement is being done on an optical or an electrical signal.
- The 4th-order Bessel-Thomson response is to be used only for optical measurements of RN. The bandwidth of the Bessel-Thomson response is called out in the relevant standard for the application. RN in the electrical domain is defined in a noise bandwidth of 12 GHz
- Control of optical reflections and polarization, if necessary, should be employed to minimize optical noise, as no optical noise is the most accurate input condition for determining the relative noise contributed by the module.
- Location of histograms are shown in Figure 68-4 in 802.3 CL 68.
- Noises at both logic levels should be measured: logicONEnoise(rms) and logicZEROnoise(rms). Apply the rms technique according to the equation:

$$noise(RMS) = \sqrt{(logicONEnoise(rms)^2 + logicZEROnoise(RMS)^2)/2}$$

- The equation for RN is given above. A calculation of Qsq is not required, nor is a calculation in units of dB/Hz, such as for transmitter RIN. If logicONEnoise(RMS) equals logicZEROnoise(RMS) then RN equals 1/Qsq

D.10 WAVEFORM DISTORTION PENALTY (WDP)

WDP is a waveshape metric for waveform filtering or other. WDP uses the same procedure and code as defined by TWDP in clause IEEE 802.3 CL 68.6.6 (LRM) with consideration of these comments:

- For purposes of this document, the definitions and procedures generally apply to both optical and electrical signals. Optical terms (such as power) and units can be converted to corresponding electrical terms (such as voltage) and units, etc.
- WDP is not restricted to transmitter measurements (hence, the “T” is dropped).
- The 4th-order Bessel-Thomson response is to be used only for optical measurements of WDP, such as calibration of an optical receiver test system. The bandwidth of the Bessel-Thomson response is called out in the relevant standard for the application.
- The definition of electrical WDP assumes a measurement bandwidth of 12 GHz. A different measurement bandwidth can be corrected for by processing the captured waveform before the WDP calculation. However, a higher bandwidth is expected to have little effect on the result.
- PRBS9 is suitable as a test sequence for all applications unless specified otherwise.
- Code details:
    - WDP does not use the three emulated reference multi-mode fibers in the TWDP code. The three fibers (the last three rows in FiberResp) are replaced with a single identity channel [0 1 0 0], and therefore, only one penalty value is calculated for each measurement (only one pass of the ii loop).
    - In the TWDP code the number of feed-forward taps (EqNf) and the number of feedback taps (EqNb) are as given in Table 15 and Table 20.
    - The unit interval (one symbol period) must reflect the signaling rate of the signal being measured.
    - The output variable (TWDP) is the measured value for WDP.

D.11 TEST METHOD FOR A HOST RECEIVER WITH A LINEAR MODULE

An example compliance method for host for use with a linear module receiver is shown in Figure 43. The host input at point C can be tested for BER compliance with test signals that represent the worst case waveshape and noise properties expected from the output of a module during compliant operation.

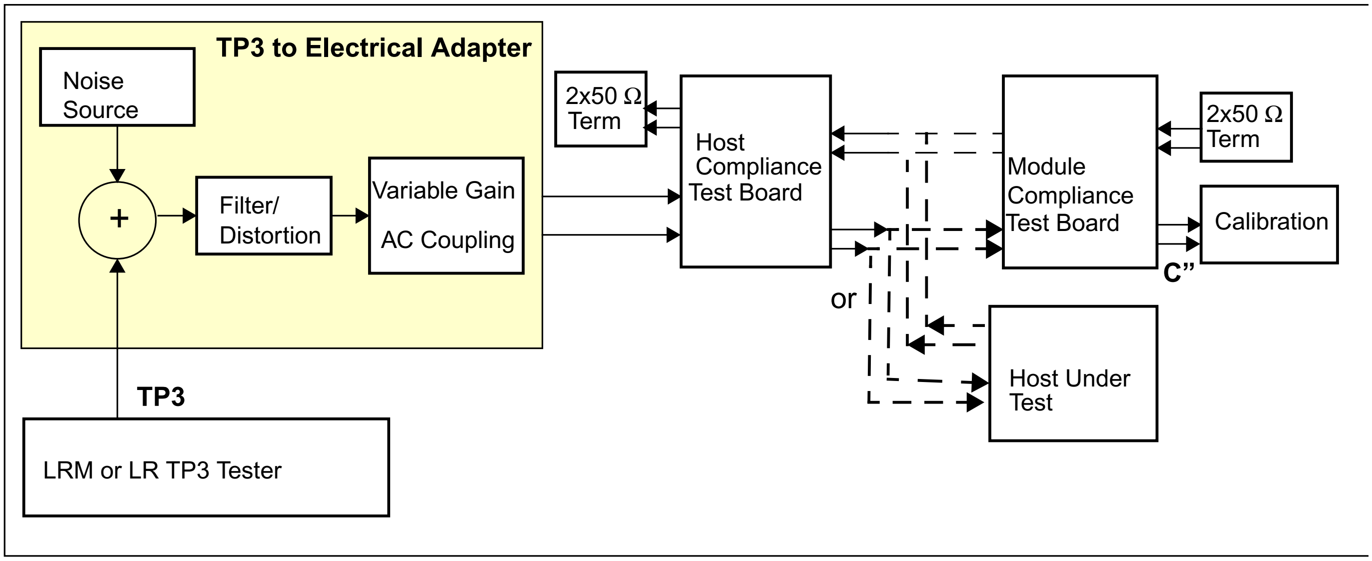

Figure 43 TP3 to electrical adaptor for host that operates with linear modules

D.11.1 TEST DESCRIPTION AND PROCEDURE FOR HOST RECEIVER FOR LINEAR MODULE

A summary description of the test method is given below:

- The TP3 tester block is the same test system as defined by the LRM or LR standard for testing the TP3 compliance point. LRM and LR are chosen because this combination of tests includes both high distortion with low noise, and low distortion with high noise. Testing with an SR equivalent input is not required as the noise and distortion are between those for LR and LRM. Compliance shall be achieved for each of the three TP3 pulse shapes defined for 10GBASE-LRM in IEEE 802.3 CL 68.6.9 and for the 10GBASE-LR stressed receiver conformance test signal defined in IEEE Std 802.3 52.9.9. Compliance over a range of optical power levels is not required, but see text regarding VMA below.
- The TP3 to electrical adapter as shown in Figure 43 converts the TP3 test signal(s) into electrical signal(s) with output VMA, noise (RN) and distortion (WDP) properties defined for the Host RX input
- The specifications given in Table 15 are as measured during calibration through the Module Compliance Test Board.

- The noise source, in conjunction with the other blocks, is intended to represent the additive noise properties of a worst-case linear module. The magnitude of the noise is calibrated such that the RN values at C" are consistent with Table 15. The spectrum of the Noise source at the summing point is white with a 3 dB frequency of at least 10 GHz. The noise measured at C" represents the noise of module and the optical signal combined.
- The filter and gain/AC coupling blocks are intended to represent the deterministic dWDP and gain properties of a worst-case linear module. For the LR, LRM pre-cursor, and LRM post-cursor conditions, the frequency response of the filter is set such that the overall response of the adapter has a Bessel-Thomson response and produces the WDP values specified in Table 15 at C". The bandwidth of the filter in these cases will be approximately 7.5 GHz. For the LRM split-symmetrical condition, the bandwidth of the adaptor is 7.5 GHz, and additional non-linearity is adjusted to produce a WDP value consistent with Table 15 at C".

Editor Notes

The details for the non-linearity are still under development. An Arbitrary Waveform Generator approach is being investigated.

- The gain block and/or the input optical power level can be used to adjust VMA. The minimum and maximum VMA conditions of Table 15 should be tested.
- Care must be taken to not induce greater than 0.02 UI of DCD in the TP3 to C" adapter.
- A balun or other means provides a differential signal.
- The test signal output shall be AC coupled.
- The output return loss properties of the test system when measured with module compliance test board shall be at least 2 dB better than the specification of Table 18.
- The output of the tester is plugged through the Module Compliance Test Board into laboratory equipment for calibration
- After calibration, the tester is plugged into the Host Receiver Under Test for compliance testing.

Any implementation of the measurement configuration may be used, provided that the resulting signal and noise match those defined in Table 15.

Under all specified test conditions, a BER of better than 1E-12 shall be achieved. The transmitter of the port under test and all other ports operate in normal operation, including termination. The transmitter of the port being tested is terminated through the Host compliance test board with a

DC block and 50 Ω at each Tx SMA connector Table 15. Compliance shall be met during asynchronous transmission from the system under test. The transmitter test pattern should be the same as the pattern used for receiver testing.

D.11.2 HOST LINEAR TESTER CALIBRATION

Calibration should be done with all tester elements in place, although some components may be shut down, such as jitter and noise, while other elements are being calibrated - see below. After calibration is completed, all components are set to their calibrated levels for testing.

RN of the host test system is adjusted via the magnitude of the adapter's noise source. Calibration should use the RN measurement methods given in section D.9. There are no crosstalk sources in the Tx path during calibration of RN. Each SMA port on the Tx path of the module and host compliance test boards is terminated with 50 Ω.

WDP of the host test system is set via the filter or distortion in the adapter. If the calibration is off by a small amount, the ISI generator in the TP3 tester can be adjusted to obtain the required values.

D.12 LINEAR MODULE RECEIVER COMPLIANCE TESTS

Linear module receiver compliance tests ensure that noise generation, waveform filtering and other distortion due to the module are kept within acceptable bounds.

D.12.1 LINEAR MODULE RECEIVER ADDED NOISE COMPLIANCE TEST

The module receiver can be tested for compliance by measuring how much noise it adds to an input test signal. Figure 44 is a block diagram of a test system that defines the module receiver added noise test.

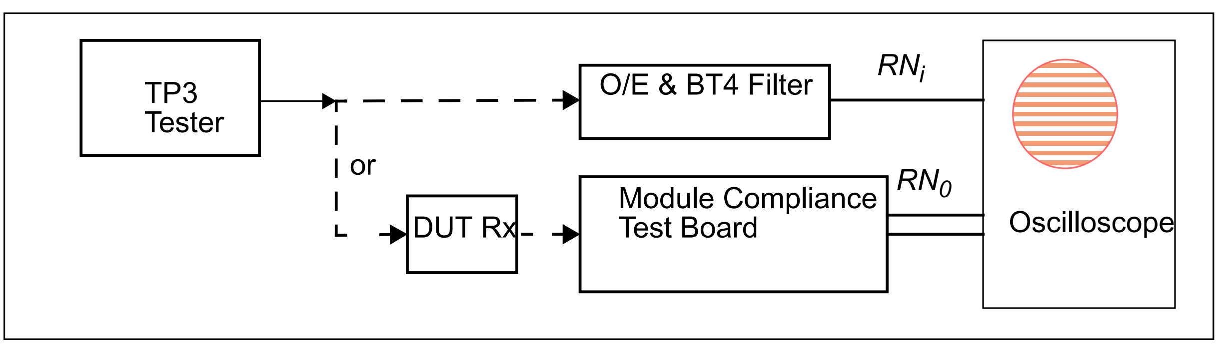

Figure 44 Linear Module receiver added noise test

To bound both module receiver noise and Tx to Rx crosstalk, there are two different test conditions for the module for each optical input condition.

- Without crosstalk. This test determines the module's receiver noise only. The module transmit path is turned off and no data is injected on the Tx input of the module compliance test board. Each Tx input of the module compliance test board is terminated with 50 Ω.
- With crosstalk. This test includes the effects of crosstalk within the module and within the module compliance test board. The module transmit path is operational. The transmit path input of the module compliance test board is connected to a pattern generator and calibrated through a host compliance test board. The amplitude is set to the maximum value allowed by Y2 in Table 17, and the rise/fall times are given in Table 20. The pattern for the crosstalk source is PRBS31. The crosstalk source is asynchronous to the TP3 test source.

Relative noise module test setup:

- Compliance must be met over the range of optical power specified by standards supported by the module.
- The TP3 tester should be set to the OMA/VMA pattern for this test as defined in D.9.
- For better accuracy the Noise of the TP3 tester should be disabled or set to very low magnitudes for this test.
- Relative noise of the TP3 test signal RN_i is first characterized through an O/E converter and 4th-order Bessel Thomson filter and a digital oscilloscope. The relative noise measurement method is described in D.9.
- The TP3 tester is removed from the O/E converter and connected into the module under test. The module in turn is plugged into the Module Compliance Test Board which in turn is connected to the oscilloscope. The relative noise of the module output signal RN_o is then measured.
- The relative noise contributed by the module is determined by:.

$$dRN = \sqrt{(RN_o)^2 - (RN_i)^2}$$

where *dRN* is the noise added by the module RN_o is the measurement result for the module output, and RN_i is the RN of the optical signal from the tester. The resulting noise result is to be compared against the compliance limit specified in Table 20.

This procedure is described for a noiseless O/E converter, Bessel-Thomson filter and oscilloscope. However, noise generated by a practical noise source, OE converter, and scope system can affect the result. The noise due to these sources is calibrated out of the result by adding and subtracting the squares of the observable relative noises as appropriate, so as to obtain the relative noise due to the module under test.

D.12.2 Linear Module Receiver Distortion Penalty Compliance Test

This section defines dWDP, a measure of waveform filtering and other distortion associated with the linear optical receiver. The block diagram dWDP test system that defines linear module receiver distortion test is shown in Figure 45.

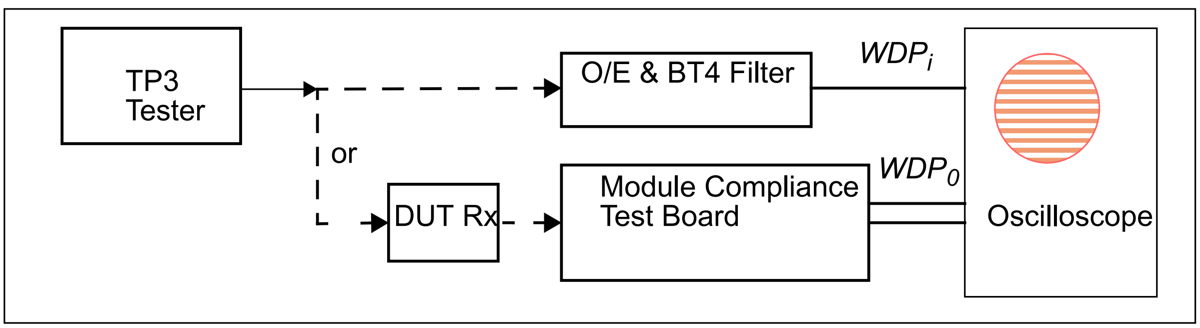

Figure 45 Module receiver waveform penalty compliance test

The measurement procedure for dWDP is similar to TWDP procedure as defined by IEEE 802.3 CL 68.6.6. WDP module test setup:

- The pattern generator is set to the PRBS9.
- To improve measurement accuracy, uncorrelated jitter and noise should be reduced. For IEEE 802.3 CL 52, sinusoidal interference and sinusoidal jitter are turned off.
- Averaging should be used to further reduce instrumentation and measurement noise so their effect on the results are negligible.
- WDP_i of the TP3 test signal is first characterized through an O/E converter and 4th-order Bessel Thomson filter and a digital oscilloscope. For 10GBASE-LRM, this signal should represent the waveforms described in IEEE Std. 802.3 CL 68.6.9, and for 10GBASE-LR, this signal represents the waveform described in IEEE Std. 802.3 CL 52.9.9. For LR and SR modules, the sinusoidal jitter and sinusoidal interference are switched off during the WDP test

- The TP3 tester is removed from the O/E converter and connected into the module under test. The module in turn is plugged into a Module Compliance Test Board which in turn is connected to the oscilloscope. WDP_o of the module output signal is then measured.
- The distortion contributed by the module is determined by the following equation:

$$dWDP = WDP_o - WDP_i$$

dWDP is to be compared against the compliance limit specified in Table 20. Each dWDP must comply for each specified TP3 condition. The TP3 tester is the same test system as defined by the relevant standard for testing the TP3 compliance point.

D.13 AC Common Mode Generation Test

To limit generation of common mode noise and associated EMI, SFI limits the maximum common mode voltage at the compliance point. The common mode voltage at any time is the average of signal+ and signal- at that time. The RMS value is calculated by applying the histogram function over one UI to the common mode signal.

The test pattern for AC common mode generation is either pattern 1 (BnBi) or pattern 3 (PRBS31) as defined in IEEE CL 52.9.1.1. It is expected that any 64B/66B scrambled signal should give a similar result.

D.14 AC Common Mode Tolerance Test

The SFI transmitter and channel limit but do not eliminate AC common mode voltage generation. SFI receivers, both module and host, must operate fully with the maximum allowed input common mode voltage. Common mode voltage often gets generated due to the crossing points of the driver outputs (P and N) being shifted from 50%, impedance mismatch, mismatch of the PCB traces, or mode conversion. AC common mode voltage for tolerance purposes may be generated by adjusting the P and N output crossing or introducing differential delay in the transmission lines. AC common mode voltage is measured and calibrated as defined in D.13.

The test pattern for AC common mode tolerance is either pattern 1 (BnBi) or pattern 3 (PRBS31) as defined in IEEE CL 52.9.1.1. It is expected that any 64B/66B coded signal should give a similar result.

D.15 TERMINATION MISMATCH

Termination mismatch is defined as the percent difference between the complimentary Z_p and Z_n resistors as shown in Figure 18. Termination mismatch is defined as:

$$\Delta Z_M = 2 \times \frac{Z_p - Z_n}{Z_p + Z_n} \times 100$$

Alternatively, the termination mismatch can be measured by applying a low frequency test tone to the differential inputs as shown in Figure 46. The test frequency must be high enough to overcome the high pass effects of the AC coupling capacitor. Differential output or input impedance is designated by Z_{diff}.

Editor Notes

Differential impedance Zdiff can be determined by any standard methods an example will be included in the next draft.

Low frequency termination mismatch is then given by:

$$\Delta Z_M = 2 \times \frac{I_p - I_n}{I_p + I_n} \cdot \frac{Z_{diff} + 100}{Z_{diff}} \cdot 100$$

where I_p and I_n are the current flowing in to the SFI port as shown in Figure 46. Z_s is the effective series impedance between the driver termination Z_p and Z_n and the AC Ground.

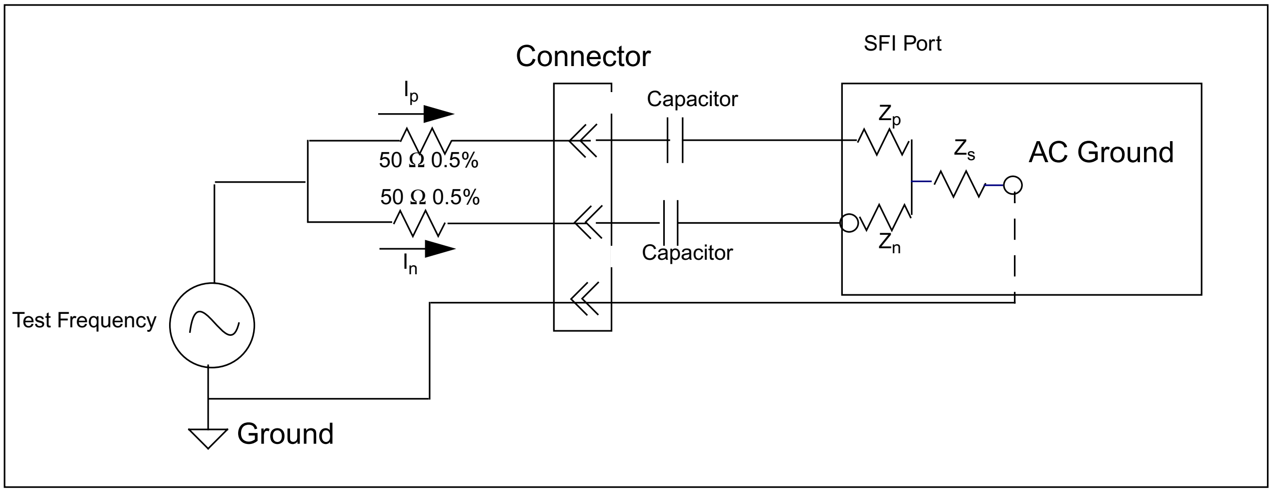

Figure 46 AC Termination Mismatch Measurement

D.16 POWER SUPPLY TESTING METHODOLOGY

This section defines power supply noise output as given in 2.8.2 and power supply noise tolerance as in 2.8.3. This methodology covers test methods to ensure compliance to the SFP+ specification.

The example host board power supply filtering shown in Figure 47 is provided for module power supply tolerance testing. This power supply filter example will meet the noise filtering requirements in most host systems. Other filtering implementations or local regulation may be used to meet the power noise output requirements described in section 2.8.2, without use of large bulk components.

Any voltage drop across a filter network on the host is counted against the host DC setpoint accuracy specification in Table 8. For this reason, the example filter illustrated in Figure 47 may not be appropriate for a host powering multiple SFP+ and/or other host components from a shared voltage supply.

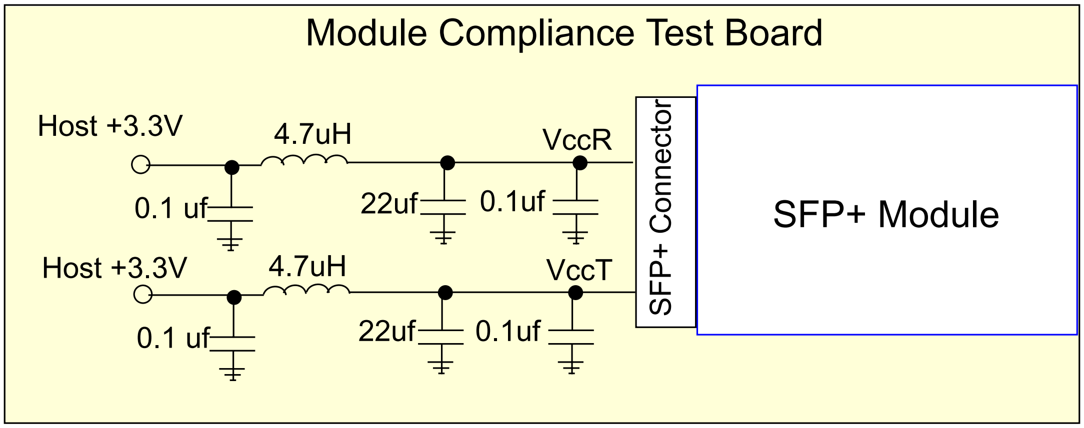

Figure 47 Module Power Supply Tolerance Filter

D.16.1 HOST POWER SUPPLY NOISE OUTPUT

The SFP+ port on a host board is tested with a resistive load in place of the SFP+ module, each voltage rail at maximum current supported by the host. Voltage is measured at the module side of the SFP+ connector. The test is performed with all other portions of the host board/system active. Hosts with multiple SFP+ modules shall test ports one at a time, with active SFP+ in all the remaining ports.

D.16.2 SFP+ MODULE POWER SUPPLY NOISE OUTPUT

The SFP+ module is tested with a high quality power supply connected through the sample filter Figure 47. Voltage is measured at the host side of the SFP+ connector, between the sample host filter network and the SFP+ connector. The module must pass this test in all operating modes. This test ensures the module will not couple excessive noise from inside the module back onto the host board. Maximum allowed noise amplitudes are listed in Table 9.

D.16.3 MODULE POWER SUPPLY TOLERANCE TESTING

In this test noise is injected to the power supply rail from a function generator generating a sine wave. The noise measurement set up is shown in . Maximum allowed noise amplitudes are listed in Table 9. The noise is AC coupled into the test board and the DC power is coupled in through an inductor to keep the noise from sinking into the power supply. The amplitude of the sinewave generator should be calibrated at each frequency at the host side of the SFP+ connector with the module replaced with a 10 Ω load between Vcc and Gnd. Note that the DC block and Toroidal inductor should have adequate frequency performance such that the required amplitude of the sinewave generator for a given calibrated amplitude is approximately constant as a function of frequency.

The test should be performed separately for VccT and VccR with the other supply connected to a separate power supply with the filtering shown for the module compliance test board.

Tests for power supply noise compliance should include optical receiver sensitivity, which can be measured with IEEE802.3 Clause 52 and 68 methodologies. Also optical transmitter jitter with a worst-case electrical eye as an input (Table 12) should be measured. Transmitter jitter testing can be done with IEEE802.3ae eyemask and TDP measurements, or LRM UJ. Testing should look at the difference of these parameters with and without the noise present. The noise source frequency is varied over the range specified by Figure 11 to determine if any frequency causes a parameter to fall out of the specification limit. In all cases, the parameters measured shall pass the optical standards with the noise present over all frequencies specified.

Editor Notes

Investigations are being made to determine whether the values in section 2.8.3 for the supply noise filter tolerance are appropriate with this revised test methodology.

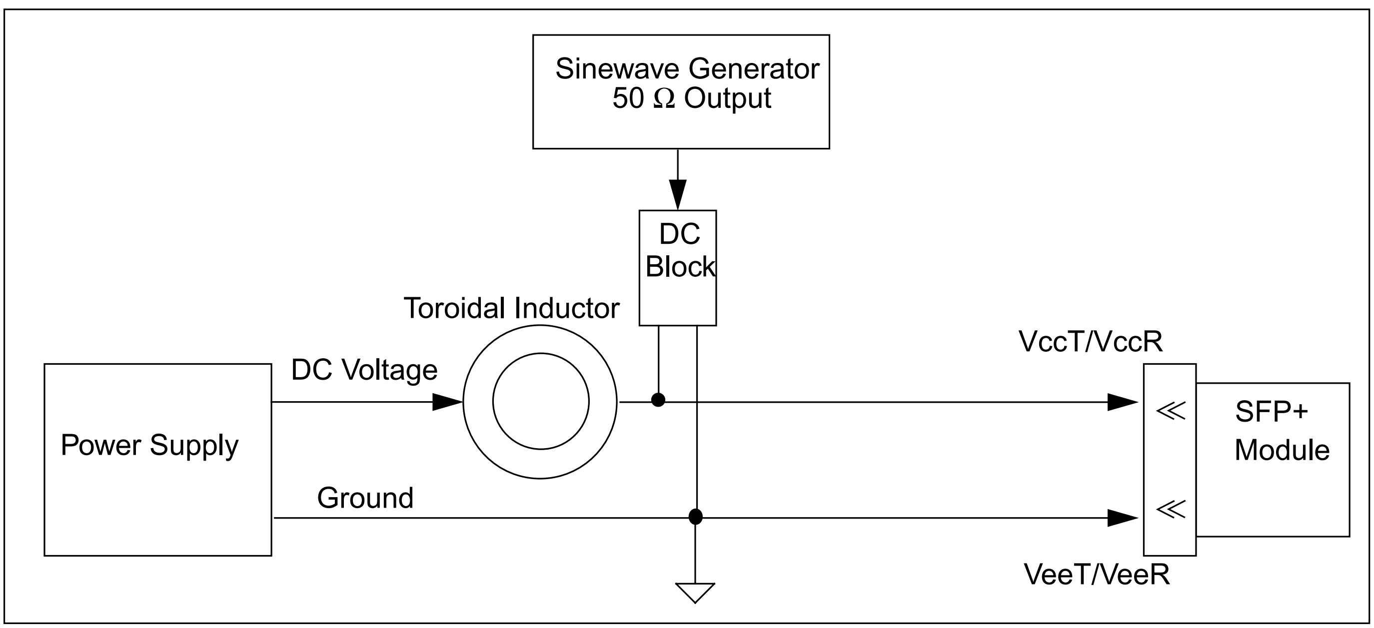

Figure 48 Power Supply Noise Tolerance Test Setup