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DDR2 SDRAM SPECIFICATION

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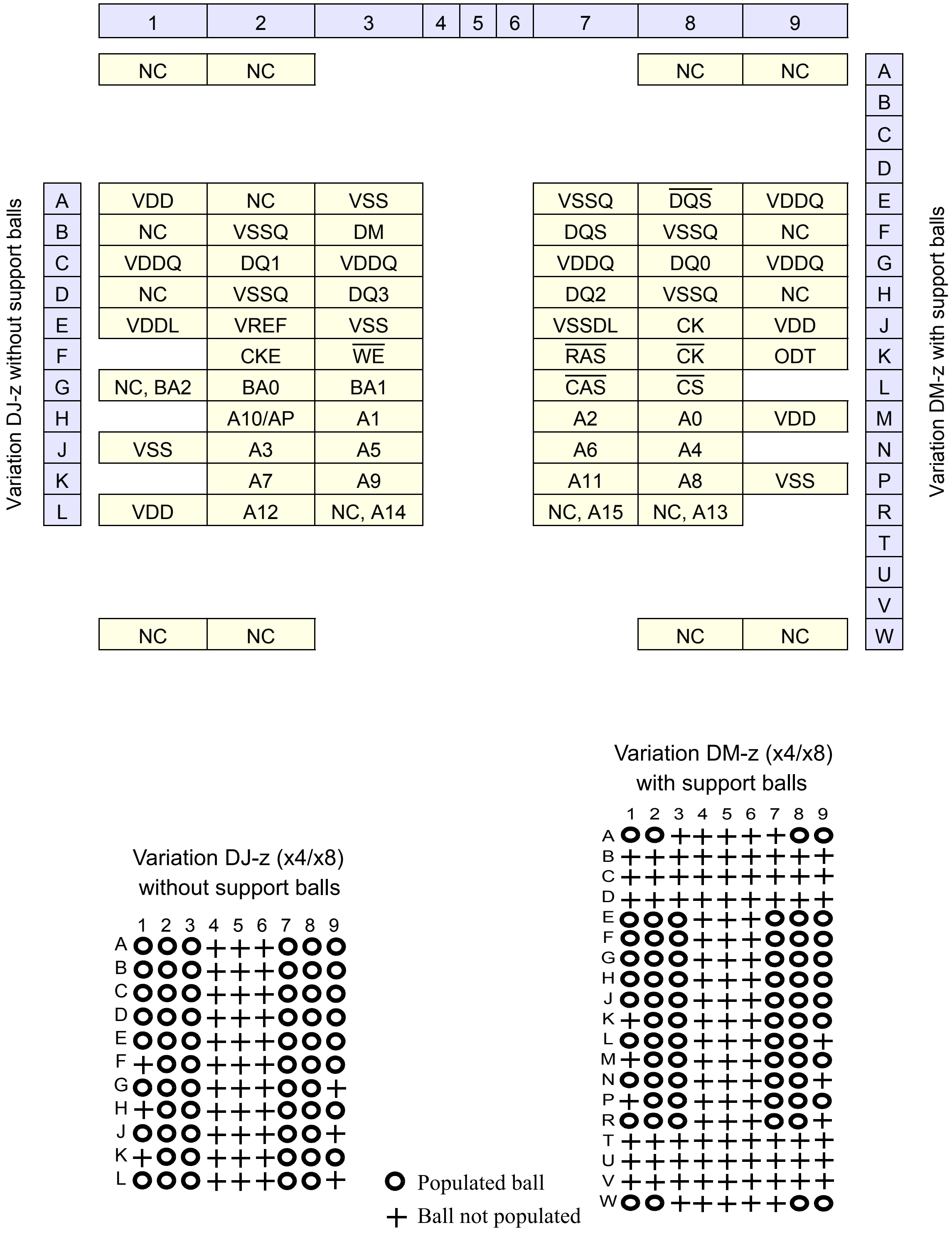
(Top view: see balls through package)



Variation DJ-z without support balls	1	2	3	4	5	6	7	8	9	Variation DM-z with support balls
	NC	NC						NC	NC	A
										B
										C
										D
A	VDD	NC	VSS				VSSQ	$\overline{\text{DQS}}$	VDDQ	E
B	NC	VSSQ	DM				DQS	VSSQ	NC	F
C	VDDQ	DQ1	VDDQ				VDDQ	DQ0	VDDQ	G
D	NC	VSSQ	DQ3				DQ2	VSSQ	NC	H
E	VDDL	VREF	VSS				VSSDL	CK	VDD	J
F		CKE	$\overline{\text{WE}}$				$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT	K
G	NC, BA2	BA0	BA1				$\overline{\text{CAS}}$	$\overline{\text{CS}}$		L
H		A10/AP	A1				A2	A0	VDD	M
J	VSS	A3	A5				A6	A4		N
K		A7	A9				A11	A8	VSS	P
L	VDD	A12	NC, A14				NC, A15	NC, A13		R
										T
										U
										V
	NC	NC						NC	NC	W

Variation DJ-z (x4/x8)
without support balls

	1	2	3	4	5	6	7	8	9
A	○	○	○	+	+	+	○	○	○
B	○	○	○	+	+	+	○	○	○
C	○	○	○	+	+	+	○	○	○
D	○	○	○	+	+	+	○	○	○
E	○	○	○	+	+	+	○	○	○
F	+	○	○	+	+	+	○	○	○
G	○	○	○	+	+	+	○	○	+
H	+	○	○	+	+	+	○	○	○
J	○	○	○	+	+	+	○	○	+
K	+	○	○	+	+	+	○	○	○
L	○	○	○	+	+	+	○	○	+

○ Populated ball
+ Ball not populated

Variation DM-z (x4/x8)
with support balls

	1	2	3	4	5	6	7	8	9
A	○	○	+	+	+	+	+	○	○
B	+	+	+	+	+	+	+	+	+
C	+	+	+	+	+	+	+	+	+
D	+	+	+	+	+	+	+	+	+
E	○	○	○	+	+	+	○	○	○
F	○	○	○	+	+	+	○	○	○
G	○	○	○	+	+	+	○	○	○
H	○	○	○	+	+	+	○	○	○
J	○	○	○	+	+	+	○	○	○
K	+	○	○	+	+	+	○	○	○
L	○	○	○	+	+	+	○	○	+
M	+	○	○	+	+	+	○	○	○
N	○	○	○	+	+	+	○	○	+
P	+	○	○	+	+	+	○	○	○
R	○	○	○	+	+	+	○	○	+
T	+	+	+	+	+	+	+	+	+
U	+	+	+	+	+	+	+	+	+
V	+	+	+	+	+	+	+	+	+
W	○	○	+	+	+	+	+	○	○

Figure 1 — DDR2 SDRAM x4 ballout using MO-207

1 Package ballout & addressing (cont'd)

1.1 DDR2 SDRAM package ballout (cont'd)

(Top view: see balls through package)

Variation DJ-z without support balls	1	2	3	4	5	6	7	8	9	Variation DM-z with support balls
	NC	NC						NC	NC	A
										B
										C
										D
A	VDD	NU/$\overline{\text{RDQS}}$	VSS				VSSQ	$\overline{\text{DQS}}$	VDDQ	E
B	DQ6	VSSQ	DM/RDQS				DQS	VSSQ	DQ7	F
C	VDDQ	DQ1	VDDQ				VDDQ	DQ0	VDDQ	G
D	DQ4	VSSQ	DQ3				DQ2	VSSQ	DQ5	H
E	VDDL	VREF	VSS				VSSDL	CK	VDD	J
F		CKE	$\overline{\text{WE}}$				$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT	K
G	NC, BA2	BA0	BA1				$\overline{\text{CAS}}$	$\overline{\text{CS}}$		L
H		A10/AP	A1				A2	A0	VDD	M
J	VSS	A3	A5				A6	A4		N
K		A7	A9				A11	A8	VSS	P
L	VDD	A12	NC, A14				NC, A15	NC, A13		R
										T
										U
										V
	NC	NC						NC	NC	W

NOTE 1 B1, B9, D1, D9 = NC for x4 organization per variation DJ-z.

NOTE 2 Pins B3 and A2 have identical capacitances as pins B7 and A8.

NOTE 3 For a Read, when enabled, strobe pair RDQS & $\overline{\text{RDQS}}$ are identical in function and timing to strobe pair DQS & $\overline{\text{DQS}}$ and input data masking function is disabled.

NOTE 4 The function of DM or RDQS/$\overline{\text{RDQS}}$ is enabled by EMRS command.

NOTE 5 VDDL and VSSDL are power and ground for the DLL. It is recommended that they be isolated on the device from VDD, VDDQ, VSS, and VSSQ. However as this is not required, users should refer to vendor data sheet for actual implementation information.

Variation DJ-z (x4/x8)
without support balls

	1	2	3	4	5	6	7	8	9
A	○	○	○	+	+	+	○	○	○
B	○	○	○	+	+	+	○	○	○
C	○	○	○	+	+	+	○	○	○
D	○	○	○	+	+	+	○	○	○
E	○	○	○	+	+	+	○	○	○
F	+	○	○	+	+	+	○	○	○
G	○	○	○	+	+	+	○	○	+
H	+	○	○	+	+	+	○	○	○
J	○	○	○	+	+	+	○	○	+
K	+	○	○	+	+	+	○	○	○
L	○	○	○	+	+	+	○	○	+

Variation DM-z (x4/x8)
with support balls

	1	2	3	4	5	6	7	8	9
A	○	○	+	+	+	+	+	○	○
B	+	+	+	+	+	+	+	+	+
C	+	+	+	+	+	+	+	+	+
D	+	+	+	+	+	+	+	+	+
E	○	○	○	+	+	+	○	○	○
F	○	○	○	+	+	+	○	○	○
G	○	○	○	+	+	+	○	○	○
H	○	○	○	+	+	+	○	○	○
J	○	○	○	+	+	+	○	○	○
K	+	○	○	+	+	+	○	○	○
L	○	○	○	+	+	+	○	○	+
M	+	○	○	+	+	+	○	○	○
N	○	○	○	+	+	+	○	○	+
P	+	○	○	+	+	+	○	○	○
R	○	○	○	+	+	+	○	○	+
T	+	+	+	+	+	+	+	+	+
U	+	+	+	+	+	+	+	+	+
V	+	+	+	+	+	+	+	+	+
W	○	○	+	+	+	+	+	○	○

○ Populated ball

+ Ball not populated

Figure 2 — DDR2 SDRAM x8 ballout using MO-207

1 Package ballout & addressing (cont'd)

1.1 DDR2 SDRAM package ballout (cont'd)

(Top view: see balls through package)

Variation DK-z without support balls	1	2	3	4	5	6	7	8	9	Variation DL-z with support balls
	NC	NC						NC	NC	A
										B
										C
A	VDD	NC	VSS				VSSQ	$\overline{UDQS}$	VDDQ	D
B	DQ14	VSSQ	UDM				UDQS	VSSQ	DQ15	E
C	VDDQ	DQ9	VDDQ				VDDQ	DQ8	VDDQ	F
D	DQ12	VSSQ	DQ11				DQ10	VSSQ	DQ13	G
E	VDD	NC	VSS				VSSQ	$\overline{LDQS}$	VDDQ	H
F	DQ6	VSSQ	LDM				LDQS	VSSQ	DQ7	J
G	VDDQ	DQ1	VDDQ				VDDQ	DQ0	VDDQ	K
H	DQ4	VSSQ	DQ3				DQ2	VSSQ	DQ5	L
J	VDDL	VREF	VSS				VSSDL	CK	VDD	M
K		CKE	$\overline{WE}$				$\overline{RAS}$	$\overline{CK}$	ODT	N
L	NC, BA2	BA0	BA1				$\overline{CAS}$	$\overline{CS}$		P
M		A10/AP	A1				A2	A0	VDD	R
N	VSS	A3	A5				A6	A4		T
P		A7	A9				A11	A8	VSS	U
R	VDD	A12	NC, A14				NC, A15	NC, A13		V
										W
										Y
	NC	NC						NC	NC	AA

NOTE VDDL and VSSDL are power and ground for the DLL. It is recommended that they be isolated on the device from VDD, VDDQ, VSS, and VSSQ. However as this is not required, users should refer to vendor data sheet for actual implementation information.

Variation DK-z (x16)
without support balls

	1	2	3	4	5	6	7	8	9
A	○	○	○	+	+	+	○	○	○
B	○	○	○	+	+	+	○	○	○
C	○	○	○	+	+	+	○	○	○
D	○	○	○	+	+	+	○	○	○
E	○	○	○	+	+	+	○	○	○
F	○	○	○	+	+	+	○	○	○
G	○	○	○	+	+	+	○	○	○
H	○	○	○	+	+	+	○	○	○
J	○	○	○	+	+	+	○	○	○
K	+	○	○	+	+	+	○	○	○
L	○	○	○	+	+	+	○	○	+
M	+	○	○	+	+	+	○	○	○
N	○	○	○	+	+	+	○	○	+
P	+	○	○	+	+	+	○	○	○
R	○	○	○	+	+	+	○	○	+

Variation DL-z (x16)
with support balls

	1	2	3	4	5	6	7	8	9
A	○	○	+	+	+	+	+	○	○
B	+	+	+	+	+	+	+	+	+
C	+	+	+	+	+	+	+	+	+
D	○	○	○	+	+	+	○	○	○
E	○	○	○	+	+	+	○	○	○
F	○	○	○	+	+	+	○	○	○
G	○	○	○	+	+	+	○	○	○
H	○	○	○	+	+	+	○	○	○
J	○	○	○	+	+	+	○	○	○
K	○	○	○	+	+	+	○	○	○
L	○	○	○	+	+	+	○	○	○
M	○	○	○	+	+	+	○	○	○
N	+	○	○	+	+	+	○	○	○
P	○	○	○	+	+	+	○	○	+
R	+	○	○	+	+	+	○	○	○
T	○	○	○	+	+	+	○	○	+
U	+	○	○	+	+	+	○	○	○
V	○	○	○	+	+	+	○	○	+
W	+	+	+	+	+	+	+	+	+
X	+	+	+	+	+	+	+	+	+
AA	○	○	+	+	+	+	+	○	○

○ Populated ball
+ Ball not populated

Figure 3 — DDR2 SDRAM x16 ballout using MO-207

1 Package ballout & addressing (cont’d)

1.1 DDR2 SDRAM package ballout (cont’d)

(Top view: see balls through package)

Variation AA without support balls	1	2	3	4	5	6	7	8	9	Variation AD with support balls
	NC	NC						NC	NC	A
										B
										C
										D
A	VDD	NC	VSS				VSSQ	$\overline{\text{DQS}}$	VDDQ	E
B	NC	VSSQ	DM				DQS	VSSQ	NC	F
C	VDDQ	DQ1	VDDQ				VDDQ	DQ0	VDDQ	G
D	NC	VSSQ	DQ3				DQ2	VSSQ	NC	H
E	VDDL	VREF	VSS				VSSDL	CK	VDD	J
F		CKE0	$\overline{\text{WE}}$				$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT0	K
G	NC, BA2	BA0	BA1				$\overline{\text{CAS}}$	$\overline{\text{CS0}}$	$\overline{\text{CS1}}$	L
H	CKE1	A10/AP	A1				A2	A0	VDD	M
J	VSS	A3	A5				A6	A4	ODT1	N
K		A7	A9				A11	A8	VSS	P
L	VDD	A12	NC, A14				NC, A15	NC, A13		R
										T
										U
										V
	NC	NC						NC	NC	W

NOTE This stacked ballot is intended for use only in stacked packages, and does not apply to any non-stacked package. This document (JESD79-2) focuses on non-stacked single-die devices with a few exceptions like the stacked ballout diagrams in Figures 4, 5, 6, 7 and 8.

Variation AA (x4/x8)
without support balls

	1	2	3	4	5	6	7	8	9
A	○	○	○	+	+	+	○	○	○
B	○	○	○	+	+	+	○	○	○
C	○	○	○	+	+	+	○	○	○
D	○	○	○	+	+	+	○	○	○
E	○	○	○	+	+	+	○	○	○
F	+	○	○	+	+	+	○	○	○
G	○	○	○	+	+	+	○	○	○
H	○	○	○	+	+	+	○	○	○
J	○	○	○	+	+	+	○	○	○
K	+	○	○	+	+	+	○	○	○
L	○	○	○	+	+	+	○	○	+

Variation AD (x4/x8)
with support balls

	1	2	3	4	5	6	7	8	9
A	○	○	+	+	+	+	+	○	○
B	+	+	+	+	+	+	+	+	+
C	+	+	+	+	+	+	+	+	+
D	+	+	+	+	+	+	+	+	+
E	○	○	○	+	+	+	○	○	○
F	○	○	○	+	+	+	○	○	○
G	○	○	○	+	+	+	○	○	○
H	○	○	○	+	+	+	○	○	○
J	○	○	○	+	+	+	○	○	○
K	+	○	○	+	+	+	○	○	○
L	○	○	○	+	+	+	○	○	○
M	○	○	○	+	+	+	○	○	○
N	○	○	○	+	+	+	○	○	○
P	+	○	○	+	+	+	○	○	○
R	○	○	○	+	+	+	○	○	+
T	+	+	+	+	+	+	+	+	+
U	+	+	+	+	+	+	+	+	+
V	+	+	+	+	+	+	+	+	+
W	○	○	+	+	+	+	+	○	○

○ Populated ball
+ Ball not populated

Figure 4 — Stacked/dual-die DDR2 SDRAM x4 ballout using MO-242

1 Package ballout & addressing (cont’d)

1.1 DDR2 SDRAM package ballout (cont’d)

(Top view: see balls through package)

Variation AA without support balls

Variation AD with support balls

	1	2	3	4	5	6	7	8	9	
	NC	NC						NC	NC	A
										B
										C
										D
A	VDD	NU/$\overline{\text{RDQS}}$	VSS				VSSQ	$\overline{\text{DQS}}$	VDDQ	E
B	DQ6	VSSQ	DM/RDQS				DQS	VSSQ	DQ7	F
C	VDDQ	DQ1	VDDQ				VDDQ	DQ0	VDDQ	G
D	DQ4	VSSQ	DQ3				DQ2	VSSQ	DQ5	H
E	VDDL	VREF	VSS				VSSDL	CK	VDD	J
F		CKE0	$\overline{\text{WE}}$				$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT0	K
G	NC, BA2	BA0	BA1				$\overline{\text{CAS}}$	$\overline{\text{CS0}}$	$\overline{\text{CS1}}$	L
H	CKE1	A10/AP	A1				A2	A0	VDD	M
J	VSS	A3	A5				A6	A4	ODT1	N
K		A7	A9				A11	A8	VSS	P
L	VDD	A12	NC, A14				NC, A15	NC, A13		R
										T
										U
										V
	NC	NC						NC	NC	W

NOTE This stacked ballot is intended for use only in stacked packages, and does not apply to any non-stacked package. This document (JESD79-2) focuses on non-stacked single-die devices with a few exceptions like the stacked ballout diagrams in Figures 4, 5, 6, 7 and 8.

Variation AD (x4/x8)
with support balls

	1	2	3	4	5	6	7	8	9
A	○	○	+	+	+	+	+	○	○
B	+	+	+	+	+	+	+	+	+
C	+	+	+	+	+	+	+	+	+
D	+	+	+	+	+	+	+	+	+
E	○	○	○	+	+	+	○	○	○
F	○	○	○	+	+	+	○	○	○
G	○	○	○	+	+	+	○	○	○
H	○	○	○	+	+	+	○	○	○
J	○	○	○	+	+	+	○	○	○
K	+	○	○	+	+	+	○	○	○
L	○	○	○	+	+	+	○	○	○
M	○	○	○	+	+	+	○	○	○
N	○	○	○	+	+	+	○	○	○
P	+	○	○	+	+	+	○	○	○
R	○	○	○	+	+	+	○	○	+
T	+	+	+	+	+	+	+	+	+
U	+	+	+	+	+	+	+	+	+
V	+	+	+	+	+	+	+	+	+
W	○	○	+	+	+	+	+	○	○

Variation AA (x4/x8)
without support balls

	1	2	3	4	5	6	7	8	9
A	○	○	○	+	+	+	○	○	○
B	○	○	○	+	+	+	○	○	○
C	○	○	○	+	+	+	○	○	○
D	○	○	○	+	+	+	○	○	○
E	○	○	○	+	+	+	○	○	○
F	+	○	○	+	+	+	○	○	○
G	○	○	○	+	+	+	○	○	○
H	○	○	○	+	+	+	○	○	○
J	○	○	○	+	+	+	○	○	○
K	+	○	○	+	+	+	○	○	○
L	○	○	○	+	+	+	○	○	+

○ Populated ball
+ Ball not populated

Figure 5 — Stacked/dual-die DDR2 SDRAM x8 ballout using MO-242

1 Package ballout & addressing (cont’d)

1.1 DDR2 SDRAM package ballout (cont’d)

(Top view: see balls through package)

Variation tbd without support balls

Variation tbd with support balls

	1	2	3	4	5	6	7	8	9	
	NC	NC						NC	NC	A
										B
										C
										D
A	VDD	NC	VSS				VSSQ	$\overline{\text{DQS}}$	VDDQ	E
B	NC	VSSQ	DM				DQS	VSSQ	NC	F
C	VDDQ	DQ1	VDDQ				VDDQ	DQ0	VDDQ	G
D	NC	VSSQ	DQ3				DQ2	VSSQ	NC	H
E	VDDL	VREF	VSS				VSSDL	CK	VDD	J
F		CKE0	$\overline{\text{WE}}$				$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT0	K
G	NC, BA2	BA0	BA1				$\overline{\text{CAS}}$	$\overline{\text{CS0}}$	$\overline{\text{CS1}}$	L
H	CKE1	A10/AP	A1				A2	A0	VDD	M
J	VSS	A3	A5				A6	A4	ODT1	N
K	NC, A15	A7	A9				A11	A8	VSS	P
L	VDD	A12	NC, A14				$\overline{\text{CS3}}$	NC, A13	$\overline{\text{CS2}}$	R
										T
										U
										V
	NC	NC						NC	NC	W

NOTE This stacked ballot is intended for use only in stacked packages, and does not apply to any non-stacked package. This document (JESD79-2) focuses on non-stacked single-die devices with a few exceptions like the stacked ballout diagrams in Figures 4, 5, 6, 7 and 8.

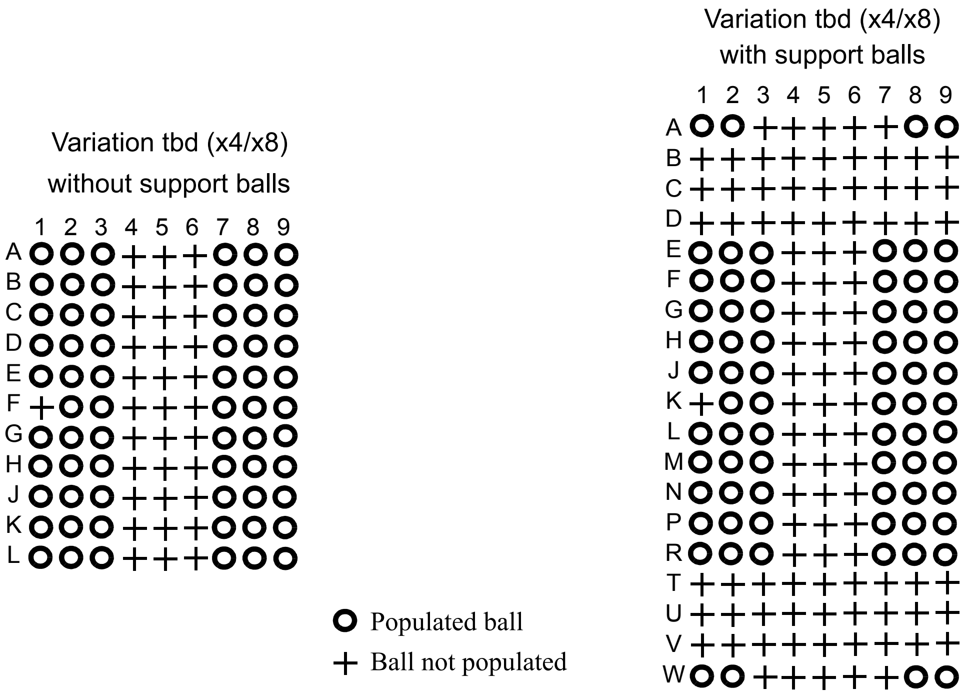


Figure 6 — Quad-stacked/quad-die DDR2 SDRAM x4 ballout using MO-242

1 Package ballout & addressing (cont'd)

1.1 DDR2 SDRAM package ballout (cont'd)

(Top view: see balls through package)

Variation tbd without support balls	1	2	3	4	5	6	7	8	9	Variation tbd with support balls
	NC	NC						NC	NC	A
										B
										C
										D
A	VDD	NU/$\overline{\text{RDQS}}$	VSS				VSSQ	$\overline{\text{DQS}}$	VDDQ	E
B	DQ6	VSSQ	DM/RDQS				DQS	VSSQ	DQ7	F
C	VDDQ	DQ1	VDDQ				VDDQ	DQ0	VDDQ	G
D	DQ4	VSSQ	DQ3				DQ2	VSSQ	DQ5	H
E	VDDL	VREF	VSS				VSSDL	CK	VDD	J
F		CKE0	$\overline{\text{WE}}$				$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT0	K
G	NC, BA2	BA0	BA1				$\overline{\text{CAS}}$	$\overline{\text{CS0}}$	$\overline{\text{CS1}}$	L
H	CKE1	A10/AP	A1				A2	A0	VDD	M
J	VSS	A3	A5				A6	A4	ODT1	N
K	NC, A15	A7	A9				A11	A8	VSS	P
L	VDD	A12	NC, A14				$\overline{\text{CS3}}$	NC, A13	$\overline{\text{CS2}}$	R
										T
										U
										V
	NC	NC						NC	NC	W

NOTE This stacked ballot is intended for use only in stacked packages, and does not apply to any non-stacked package. This document (JESD79-2) focuses on non-stacked single-die devices with a few exceptions like the stacked ballout diagrams in Figures 4, 5, 6, 7 and 8.

Variation tbd (x4/x8)
without support balls

	1	2	3	4	5	6	7	8	9
A	○	○	○	+	+	+	○	○	○
B	○	○	○	+	+	+	○	○	○
C	○	○	○	+	+	+	○	○	○
D	○	○	○	+	+	+	○	○	○
E	○	○	○	+	+	+	○	○	○
F	+	○	○	+	+	+	○	○	○
G	○	○	○	+	+	+	○	○	○
H	○	○	○	+	+	+	○	○	○
J	○	○	○	+	+	+	○	○	○
K	○	○	○	+	+	+	○	○	○
L	○	○	○	+	+	+	○	○	○

Variation tbd (x4/x8)
with support balls

	1	2	3	4	5	6	7	8	9
A	○	○	+	+	+	+	+	○	○
B	+	+	+	+	+	+	+	+	+
C	+	+	+	+	+	+	+	+	+
D	+	+	+	+	+	+	+	+	+
E	○	○	○	+	+	+	○	○	○
F	○	○	○	+	+	+	○	○	○
G	○	○	○	+	+	+	○	○	○
H	○	○	○	+	+	+	○	○	○
J	○	○	○	+	+	+	○	○	○
K	+	○	○	+	+	+	○	○	○
L	○	○	○	+	+	+	○	○	○
M	○	○	○	+	+	+	○	○	○
N	○	○	○	+	+	+	○	○	○
P	○	○	○	+	+	+	○	○	○
R	○	○	○	+	+	+	○	○	○
T	+	+	+	+	+	+	+	+	+
U	+	+	+	+	+	+	+	+	+
V	+	+	+	+	+	+	+	+	+
W	○	○	+	+	+	+	+	○	○

○ Populated ball

+ Ball not populated

Figure 7 — Quad-stacked/quad-die DDR2 SDRAM x8 ballout using MO-242

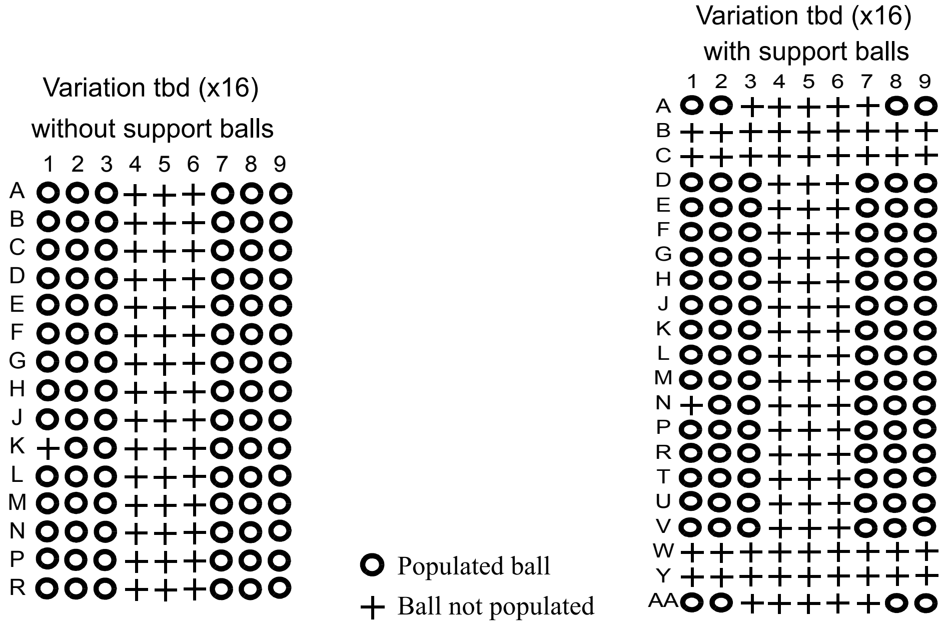
1 Package ballout & addressing (cont'd)

1.1 DDR2 SDRAM package ballout (cont'd)

(Top view: see balls through package)

Variation tbd without support balls	1	2	3	4	5	6	7	8	9	Variation tbd with support balls
	NC	NC						NC	NC	A
										B
										C
A	VDD	NC	VSS				VSSQ	$\overline{\text{UDQS}}$	VDDQ	D
B	DQ14	VSSQ	UDM				UDQS	VSSQ	DQ15	E
C	VDDQ	DQ9	VDDQ				VDDQ	DQ8	VDDQ	F
D	DQ12	VSSQ	DQ11				DQ10	VSSQ	DQ13	G
E	VDD	NC	VSS				VSSQ	$\overline{\text{LDQS}}$	VDDQ	H
F	DQ6	VSSQ	LDM				LDQS	VSSQ	DQ7	J
G	VDDQ	DQ1	VDDQ				VDDQ	DQ0	VDDQ	K
H	DQ4	VSSQ	DQ3				DQ2	VSSQ	DQ5	L
J	VDDL	VREF	VSS				VSSDL	CK	VDD	M
K		CKE0	$\overline{\text{WE}}$				$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT0	N
L	NC, BA2	BA0	BA1				$\overline{\text{CAS}}$	$\overline{\text{CS0}}$	$\overline{\text{CS1}}$	P
M	CKE1	A10/AP	A1				A2	A0	VDD	R
N	VSS	A3	A5				A6	A4	ODT1	T
P	NC, A15	A7	A9				A11	A8	VSS	U
R	VDD	A12	NC, A14				$\overline{\text{CS3}}$	NC, A13	$\overline{\text{CS2}}$	V
										W
										Y
	NC	NC						NC	NC	AA

NOTE This stacked ballot is intended for use only in stacked packages, and does not apply to any non-stacked package. This document (JESD79-2) focuses on non-stacked single-die devices with a few exceptions like the stacked ballout diagrams in Figures 4, 5, 6, 7 and 8.



Variation tbd (x16) without support balls

Variation tbd (x16) with support balls

Figure 8 — Quad-stacked/quad-die DDR2 SDRAM x16 ballout using MO-242

1 Package ballout & addressing (cont'd)

1.2 Quad-stacked/quad-die DDR2 SDRAM internal rank associations

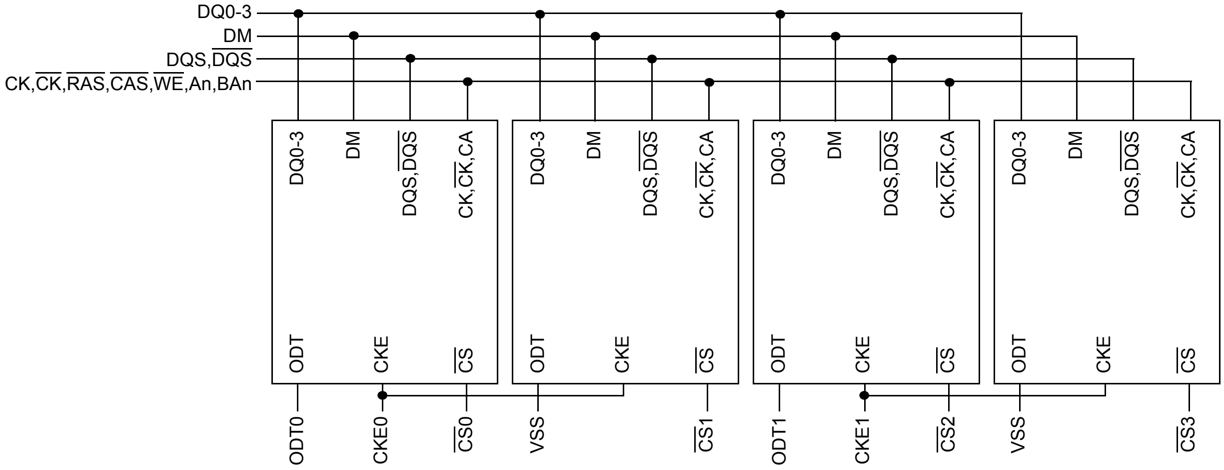


Figure 9 — Quad-stacked/quad-die DDR2 SDRAM x4 rank association

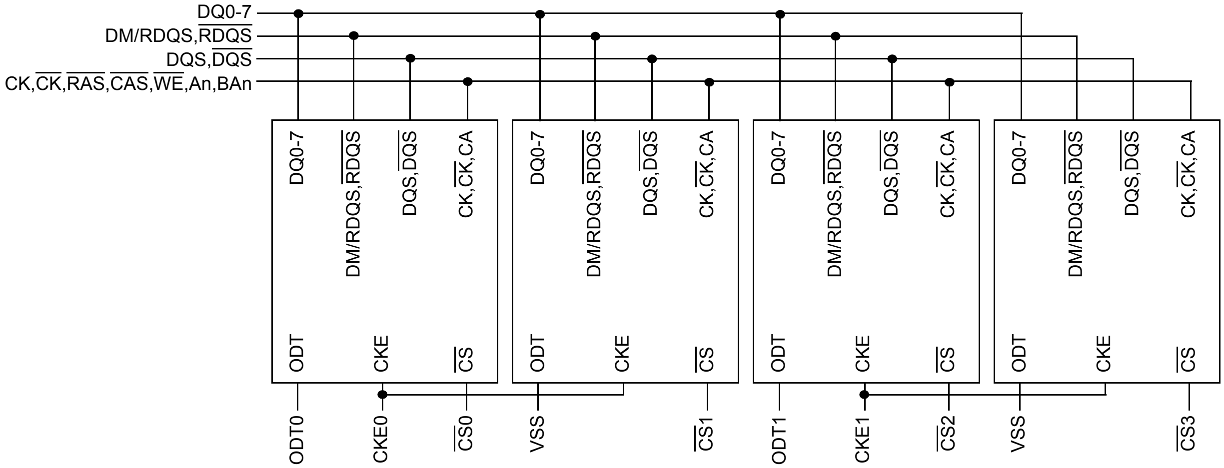


Figure 10 — Quad-stacked/quad-die DDR2 SDRAM x8 rank association

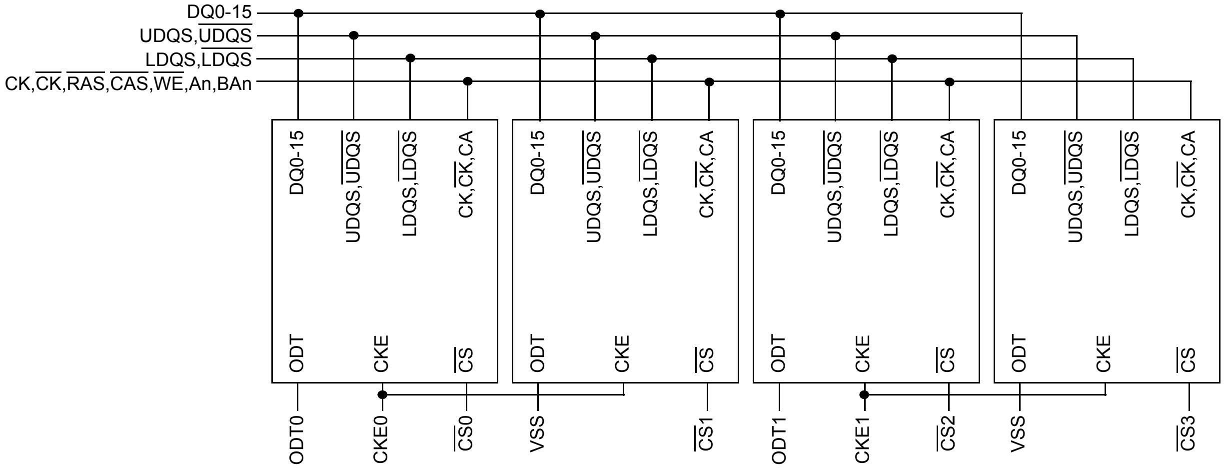


Figure 11 — Quad-stacked/quad-die DDR2 SDRAM x16 rank association

1 Package ballout & addressing (cont'd)

1.3 Input/output functional description

Table 1 — Ball descriptions

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE LOW deactivates, internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. After VREF has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must be maintained to this input. CKE must be maintained HIGH throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, and DM signal for x4/x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS/$\overline{UDQS}$, LDQS/$\overline{LDQS}$, UDM, and LDM signal. The ODT pin will be ignored if the EMR(1) is programmed to disable ODT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM (UDM), (LDM)	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For x8 device, the function of DM or RDQS/$\overline{RDQS}$ is enabled by EMRS command to EMR(1).
BA0 - BA2	Input	**Bank Address Inputs:** BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied (For 256Mb and 512Mb, BA2 is not applied). Bank address also determines if the mode register or one of the extended mode registers is to be accessed during a MRS or EMRS command cycle.
A0 - A15	Input	**Address Inputs:** Provide the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0 - BA2. The address inputs also provide the op-code during MRS or EMRS commands.
DQ	Input/Output	**Data Input/ Output:** Bi-directional data bus.
DQS, ($\overline{DQS}$) (UDQS), ($\overline{UDQS}$) (LDQS), ($\overline{LDQS}$) (RDQS), (RDQS)	Input/Output	**Data Strobe:** output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, LDQS corresponds to the data on DQ0-DQ7; UDQS corresponds to the data on DQ8-DQ15. For the x8, an RDQS option using DM pin can be enabled via the EMR(1) to simplify read timing. The data strobes DQS, LDQS, UDQS, and RDQS may be used in single ended mode or paired with optional complementary signals $\overline{DQS}$, $\overline{LDQS}$, $\overline{UDQS}$, and $\overline{RDQS}$ to provide differential pair signaling to the system during both reads and writes. A control bit at EMR(1)[A10] enables or disables all complementary data strobe signals. In this data sheet, "differential DQS signals" refers to any of the following with EMR(1)[A10] = 0 x4 DQS/$\overline{DQS}$ x8 DQS/$\overline{DQS}$ if EMR(1)[A11] = 0 x8 DQS/$\overline{DQS}$, RDQS/$\overline{RDQS}$, if EMR(1)[A11] = 1 x16 LDQS/$\overline{LDQS}$ and UDQS/$\overline{UDQS}$ "single-ended DQS signals" refers to any of the following with EMR(1)[A10] = 1 x4 DQS x8 DQS if EMR(1)[A11] = 0 x8 DQS, RDQS, if EMR(1)[A11] = 1 x16 LDQS and UDQS
NC		**No Connect:** No internal electrical connection is present.
V_{DDQ}	Supply	**DQ Power Supply:** 1.8 V +/- 0.1 V
V_{SSQ}	Supply	**DQ Ground**
V_{DDL}	Supply	**DLL Power Supply:** 1.8 V +/- 0.1 V

1 Package ballout & addressing (cont'd)

1.3 Input/output functional description (cont'd)

Table 1 — Ball descriptions (cont'd)

Symbol	Type	Function
V_{SSDL}	Supply	**DLL Ground**
V_{DD}	Supply	**Power Supply:** 1.8 V +/- 0.1 V
V_{SS}	Supply	**Ground**
V_{REF}	Supply	**Reference voltage**

1.4 DDR2 SDRAM addressing

Table 2 — 256 Mb addressing

Configuration	64 Mb x 4	32 Mb x 8	16 Mb x 16
# of Banks	4	4	4
Bank Address	BA0, BA1	BA0, BA1	BA0, BA1
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 - A12	A0 - A12	A0 - A12
Column Address	A0 - A9, A11	A0 - A9	A0 - A8
Page size*1	1 KB	1 KB	1 KB

Table 3 — 512 Mb addressing

Configuration	128 Mb x 4	64 Mb x 8	32 Mb x 16
# of Banks	4	4	4
Bank Address	BA0, BA1	BA0, BA1	BA0, BA1
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 - A13	A0 - A13	A0 - A12
Column Address	A0 - A9, A11	A0 - A9	A0 - A9
Page size *1	1 KB	1 KB	2 KB

Table 4 — 1 Gb addressing

Configuration	256 Mb x 4	128 Mb x 8	64 Mb x 16
# of Banks	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 - A13	A0 - A13	A0 - A12
Column Address	A0 - A9, A11	A0 - A9	A0 - A9
Page size *1	1 KB	1 KB	2 KB

Table 5 — 2 Gb addressing

Configuration	512 Mb x 4	256 Mb x 8	128 Mb x 16
# of Banks	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 - A14	A0 - A14	A0 - A13
Column Address	A0 - A9, A11	A0 - A9	A0 - A9
Page size *1	1 KB	1 KB	2 KB

1 Package ballout & addressing (cont’d)

1.4 DDR2 SDRAM addressing (cont’d)

Table 6 — 4 Gb addressing

Configuration	1 Gb x 4	512 Mb x 8	256 Mb x 16
# of Banks	8	8	8
Bank Address	BA0 - BA2	BA0 -BA2	BA0 - BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 - A15	A0 - A15	A0 - A14
Column Address	A0 - A9, A11	A0 - A9	A0 - A9
Page size [*1]	1 KB	1 KB	2 KB

NOTE 1 Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered. Page size is per bank, calculated as follows:

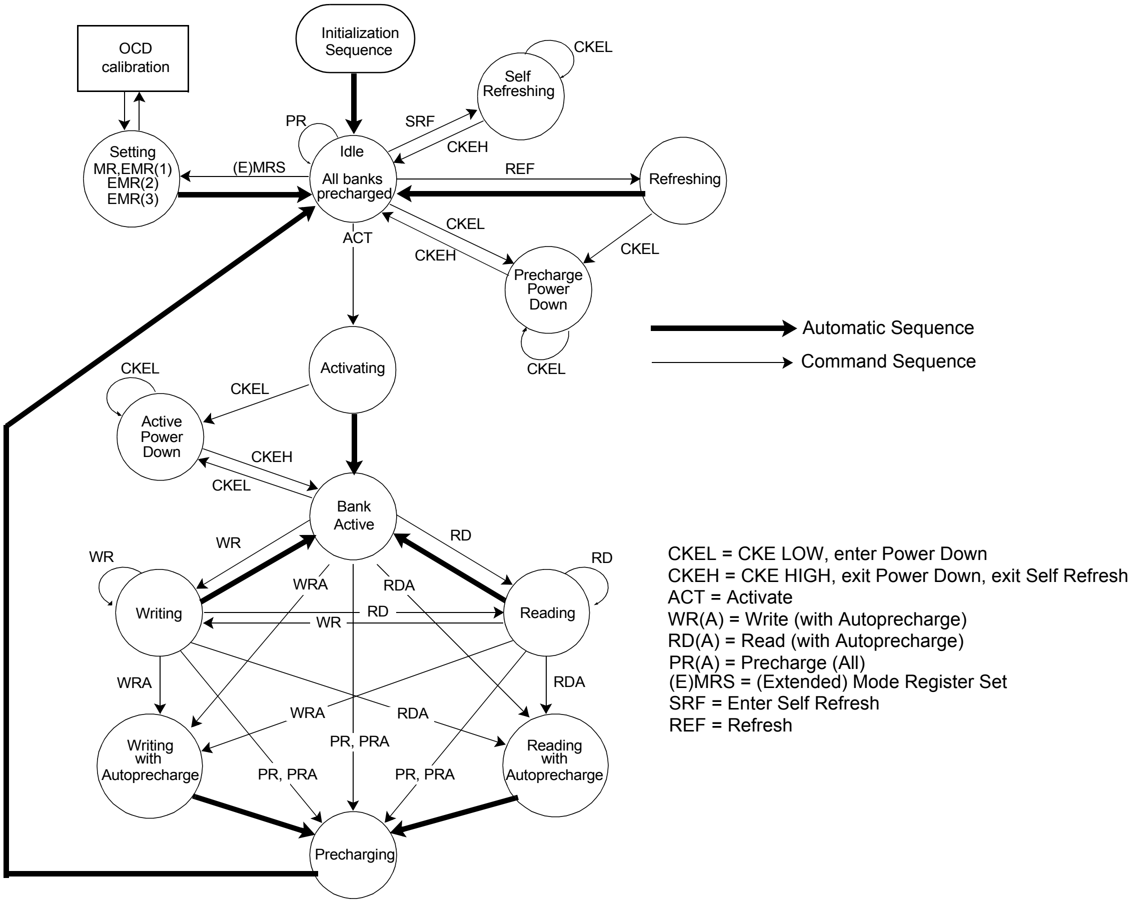
page size = $2^{COLBITS}$ x ORG ÷ 8

where

COLBITS = the number of column address bits
ORG = the number of I/O (DQ) bits

2 Functional description

2.1 Simplified state diagram



NOTE Use caution with this diagram. It is intended to provide a floorplan of the possible state transitions and the commands to control them, not all details. In particular situations involving more than one bank, enabling/disabling on-die termination, Power Down entry/exit, timing restrictions during state transitions, among other things, are not captured in full detail.

Figure 12 — DDR2 SDRAM simplified state diagram

2 Functional description (cont'd)

2.2 Basic functionality

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for a burst length of four or eight in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the active command are used to select the bank and row to be accessed (BA0-BA2 select the bank; A0-A15 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access and to determine if the auto precharge command is to be issued.

Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

2.3 Power-up and initialization

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

For DDR2 SDRAMs, both bits BA0 and BA1 must be decoded for Mode/Extended Mode Register Set (MRS/EMRS) commands. Users must initialize all four Mode Registers. The registers may be initialized in any order.

2.3.1 Power-up and initialization sequence

The following sequence is required for Power-up and Initialization.

a) Either one of the following sequence is required for Power-up.

a1) While applying power, attempt to maintain CKE below 0.2 x VDDQ and ODT^{*1} at a LOW state (all other inputs may be undefined.) The VDD voltage ramp time must be no greater than 200 ms from when VDD ramps from 300 mV to VDD min; and during the VDD voltage ramp, |VDD-VDDQ| ≤ 0.3 volts. Once the ramping of the supply voltages is complete (when VDDQ crosses VDDQ min), the supply voltage specifications provided in section 5, Table 16 Recommended DC operating conditions (SSTL_1.8), prevail.

- VDD, VDDL and VDDQ are driven from a single power converter output, AND
- VTT is limited to 0.95 V max, AND
- Vref tracks VDDQ/2, VREF must be within +/- 300 mV with respect to VDDQ/2 during supply ramp time.
- VDDQ ≥ VREF must be met at all times.

a2) While applying power, attempt to maintain CKE below 0.2 x VDDQ and ODT^{*1} at a LOW state, all other inputs may be undefined, voltage levels at I/Os and outputs must be less than VDDQ during voltage ramp time to avoid DRAM latch-up. During the ramping of the supply voltages, VDD ≥ VDDL ≥ VDDQ must be maintained and is applicable to both AC and DC levels until the ramping of the supply voltages is complete, which is when VDDQ crosses VDDQ min. Once the ramping of the supply voltages is complete, the supply voltage specifications provided in section 5, Table 16 Recommended DC operating conditions (SSTL_1.8), prevail.

- Apply VDD/VDDL before or at the same time as VDDQ.
- VDD/VDDL voltage ramp time must be no greater than 200 ms from when VDD ramps from 300 mV to VDD min
- Apply VDDQ before or at the same time as VTT.
- The VDDQ voltage ramp time from when VDD min is achieved on VDD to when VDDQ min is achieved on VDDQ must be no greater than 500 ms.
  (Note: While VDD is ramping, current may be supplied from VDD through the DRAM to VDDQ.)
- Vref must track VDDQ/2, Vref must be within +/- 300 mv with respect to VDDQ/2 during supply ramp time.
- VDDQ ≥ VREF must be met at all times.
- Apply VTT.
- The VTT voltage ramp time from when VDDQ min is achieved on VDDQ to when VTT min is achieved on VTT must be no greater than 500 ms.

b) Start clock and maintain stable condition.

c) For the minimum of 200 us after stable power (VDD, VDDL, VDDQ, VREF and VTT are between their minimum and maximum values as stated in section 5, Table 16 Recommended DC operating conditions (SSTL_1.8)) and stable clock (CK, $\overline{\text{CK}}$), then apply NOP or Deselect & take CKE HIGH.

2.3 Power-up and initialization (cont'd)

2.3.1 Power-up and initialization sequence (cont'd)

d) Wait minimum of 400 ns then issue precharge all command. NOP or Deselect applied during 400 ns period.

e) Issue an EMRS command to EMR(2). (To issue EMRS command to EMR(2), provide LOW to BA0 and BA2, HIGH to BA1.)

f) Issue an EMRS command to EMR(3). (To issue EMRS command to EMR(3), provide LOW to BA2, HIGH to BA0 and BA1.)

g) Issue EMRS to enable DLL. (To issue DLL Enable command, provide LOW to A0, HIGH to BA0 and LOW to BA1-BA2 and A13-A15. And A9=A8=A7=LOW must be used when issuing this command.)

h) Issue a Mode Register Set command for DLL reset.
(To issue DLL Reset command, provide HIGH to A8 and LOW to BA0-BA2, and A13-A15.)

i) Issue a precharge all command.

j) Issue 2 or more auto-refresh commands.

k) Issue a MRS command with LOW to A8 to initialize device operation. (i.e. to program operating parameters without resetting the DLL.)

l) At least 200 clocks after step h, execute OCD Calibration (Off Chip Driver impedance adjustment).
If OCD calibration is not used, EMRS to EMR(1) to set OCD Calibration Default (A9=A8=A7=HIGH) followed by EMRS to EMR(1) to exit OCD Calibration Mode (A9=A8=A7=LOW) must be issued with other operating parameters of EMR(1).

m) The DDR2 SDRAM is now ready for normal operation.

*1: To guarantee ODT off, VREF must be valid and a LOW level must be applied to the ODT pin.

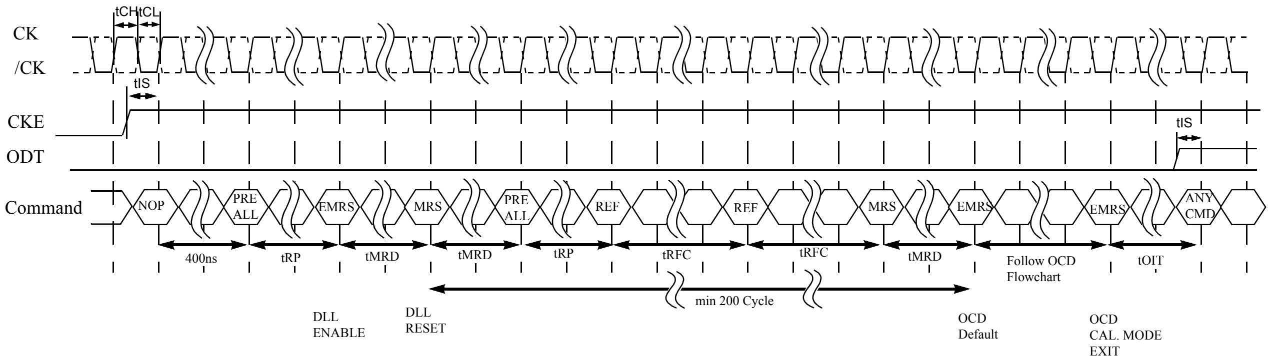


Figure 13 — Initialization sequence after power-up

2.4 Programming the mode and extended mode registers

For application flexibility, burst length, burst type, $\overline{CAS}$ latency, DLL reset function, write recovery time (WR) are user defined variables and must be programmed with a Mode Register Set (MRS) command. Additionally, DLL disable function, driver impedance, additive CAS latency, ODT (On Die Termination), single-ended strobe, and OCD (off chip driver impedance adjustment) are also user defined variables and must be programmed with an Extended Mode Register Set (EMRS) command. Contents of the Mode Register (MR) or Extended Mode Registers (EMR(#)) can be altered by re-executing the MRS or EMRS Commands. Even if the user chooses to modify only a subset of the MR or EMR(#) variables, all variables within the addressed register must be redefined when the MRS or EMRS commands are issued.

MRS, EMRS and Reset DLL do not affect array contents, which means re-initialization including those can be executed at any time after power-up without affecting array contents.

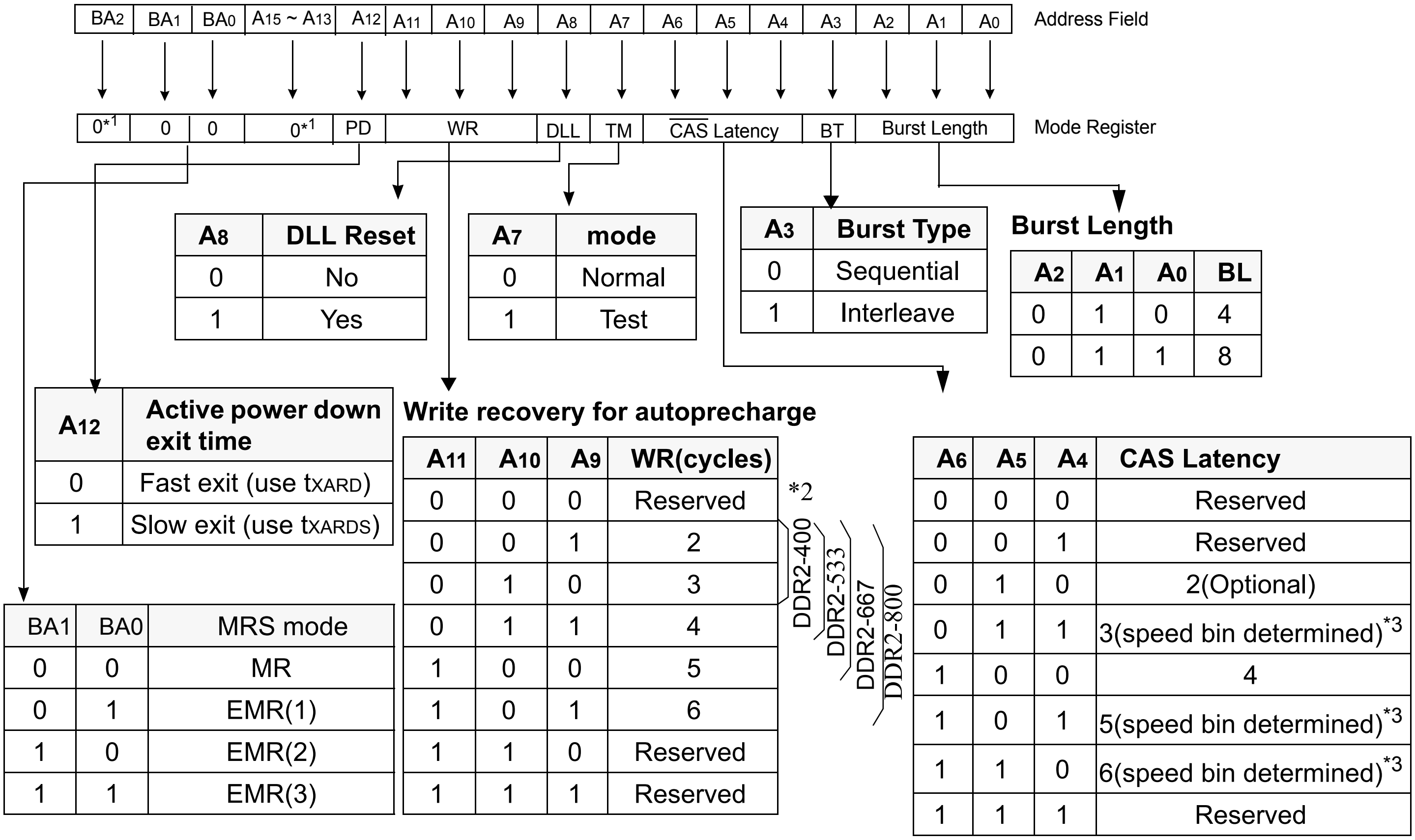
2.4.1 DDR2 SDRAM mode register (MR)

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It controls $\overline{CAS}$ latency, burst length, burst sequence, test mode, DLL reset, WR and various vendor specific options to make DDR2 SDRAM useful for various applications. The default value of the mode register is not defined, therefore the mode

2.4 Programming the mode and extended mode registers (cont'd)

2.4.1 DDR2 SDRAM mode register (MR) (cont'd)

register must be programmed during initialization for proper operation. The mode register is written by asserting LOW on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0 and BA1, while controlling the state of address pins A0 - A15. The DDR2 SDRAM should be in all bank precharge state with CKE already HIGH prior to writing into the mode register. The mode register set command cycle time (tMRD) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. The mode register is divided into various fields depending on functionality. Burst length is defined by A0 - A2 with options of 4 and 8 bit burst lengths. The burst length decodes are compatible with DDR SDRAM. Burst address sequence type is defined by A3, $\overline{CAS}$ latency is defined by A4 - A6. The DDR2 does not support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to LOW for normal MRS operation. Write recovery time WR is defined by A9 - A11. Refer to the table for specific codes.



A8	DLL Reset
0	No
1	Yes

A7	mode
0	Normal
1	Test

A3	Burst Type
0	Sequential
1	Interleave

Burst Length

A2	A1	A0	BL
0	1	0	4
0	1	1	8

A12	Active power down exit time
0	Fast exit (use tXARD)
1	Slow exit (use tXARDS)

Write recovery for autoprecharge

A11	A10	A9	WR(cycles)
0	0	0	Reserved
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	Reserved
1	1	1	Reserved

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2(Optional)
0	1	1	3(speed bin determined)*3
1	0	0	4
1	0	1	5(speed bin determined)*3
1	1	0	6(speed bin determined)*3
1	1	1	Reserved

BA1	BA0	MRS mode
0	0	MR
0	1	EMR(1)
1	0	EMR(2)
1	1	EMR(3)

NOTE 1 BA2 and A13-A15 are reserved for future use and must be set to 0 when programming the MR.
NOTE 2 For DDR2-400/533, WR (write recovery for autoprecharge) min is determined by tCK max and WR max is determined by tCK min. WR in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer (WR[cycles] = RU{ tWR[ns] / tCK[ns] }, where RU stands for round up). For DDR2-667/800, WR min is determined by tCK(avg) max and WR max is determined by tCK(avg) min. WR[cycles] = RU{ tWR[ns] / tCK(avg)[ns] }, where RU stands for round up. The mode register must be programmed to this value. This is also used with tRP to determine tDAL.
NOTE 3 Speed bin determined. Not required on all speed bins.

Figure 14 — DDR2 SDRAM mode register set (MRS)

2.4.2 DDR2 SDRAM extended mode registers (EMR(#))

2.4.2.1 EMR(1)

The extended mode register(1) stores the data for enabling or disabling the DLL, output driver strength, additive latency, ODT, $\overline{DQS}$ disable, OCD program, RDQS enable. The default value of the extended mode register(1) is not

2.4.2 DDR2 SDRAM extended mode registers (EMR(#)) (cont’d)

2.4.2.1 EMR(1) (cont’d)

defined, therefore the extended mode register(1) must be programmed during initialization for proper operation. The extended mode register(1) is written by asserting LOW on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, HIGH on BA0 and LOW on BA1, while controlling the states of address pins A0 - A15. The DDR2 SDRAM should be in all bank precharge with CKE already HIGH prior to writing into the extended mode register(1). The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register(1). Extended mode register(1) contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. A0 is used for DLL enable or disable. A1 is used for enabling a reduced strength output driver. A3 - A5 determines the additive latency, A7 - A9 are used for OCD control, A10 is used for $\overline{DQS}$ disable and A11 is used for RDQS enable. A2 and A6 are used for ODT setting.

2.4.2.2 DLL enable/disable

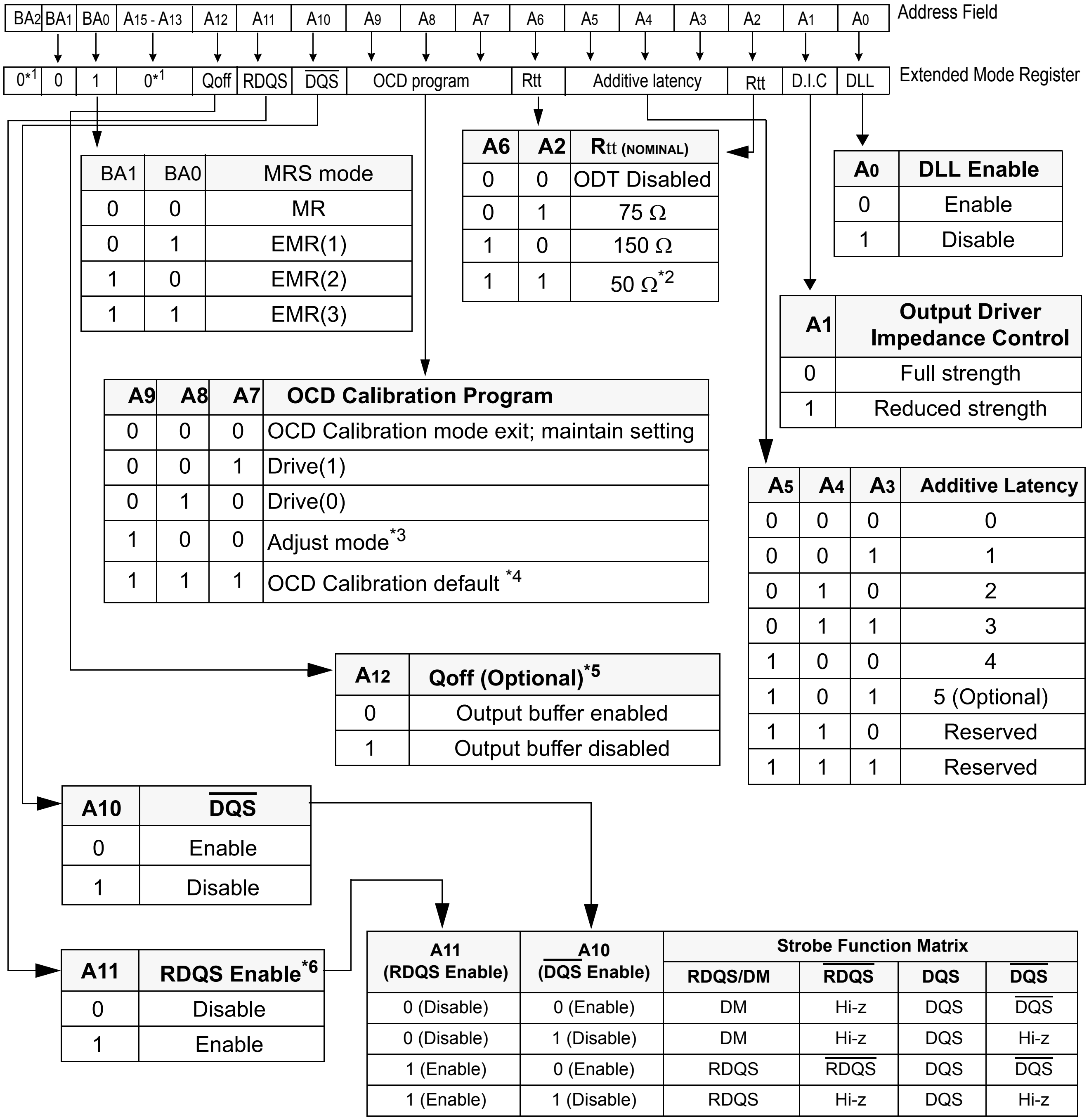
The DLL must be enabled for normal operation. DLL enable is required during power-up and initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tAC or tDQSCK parameters.

2.4.2.3 EMR(1) programming

Figure 15 shows the EMR(1) programming.

2.4.2 DDR2 SDRAM extended mode registers (EMR(#)) (cont'd)

2.4.2.3 EMR(1) programming (cont'd)



BA1	BA0	MRS mode
0	0	MR
0	1	EMR(1)
1	0	EMR(2)
1	1	EMR(3)

A6	**A2**	**Rtt (NOMINAL)**
0	0	ODT Disabled
0	1	75 Ω
1	0	150 Ω
1	1	50 Ω*2

A0	**DLL Enable**
0	Enable
1	Disable

A1	**Output Driver Impedance Control**
0	Full strength
1	Reduced strength

A9	**A8**	**A7**	**OCD Calibration Program**
0	0	0	OCD Calibration mode exit; maintain setting
0	0	1	Drive(1)
0	1	0	Drive(0)
1	0	0	Adjust mode*3
1	1	1	OCD Calibration default *4

A5	**A4**	**A3**	**Additive Latency**
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5 (Optional)
1	1	0	Reserved
1	1	1	Reserved

A12	**Qoff (Optional)*5**
0	Output buffer enabled
1	Output buffer disabled

A10	**$\overline{\text{DQS}}$**
0	Enable
1	Disable

A11	**RDQS Enable*6**
0	Disable
1	Enable

A11 (RDQS Enable)	**$\overline{\text{A10}}$ (DQS Enable)**	**Strobe Function Matrix**			
		RDQS/DM	**$\overline{\text{RDQS}}$**	**DQS**	**$\overline{\text{DQS}}$**
0 (Disable)	0 (Enable)	DM	Hi-z	DQS	$\overline{\text{DQS}}$
0 (Disable)	1 (Disable)	DM	Hi-z	DQS	Hi-z
1 (Enable)	0 (Enable)	RDQS	$\overline{\text{RDQS}}$	DQS	$\overline{\text{DQS}}$
1 (Enable)	1 (Disable)	RDQS	Hi-z	DQS	Hi-z

NOTE 1 BA2 and A13-A15 are reserved for future use and must be set to 0 when programming the EMR(1).
NOTE 2 Optional for DDR2-400/533/667, mandatory for DDR2-800.
NOTE 3 When Adjust mode is issued, AL from previously set value must be applied.
NOTE 4 After setting to default, OCD calibration mode needs to be exited by setting A9-A7 to 000. Refer to section 2.4.3 for detailed information.
NOTE 5 Output disabled - DQs, DQSs, $\overline{\text{DQS}}$s, RDQS, $\overline{\text{RDQS}}$. This feature is used in conjunction with DIMM IDD measurements when IDDQ is not desired to be included.
NOTE 6 If RDQS is enabled, the DM function is disabled. RDQS is active for reads and don't care for writes.

Figure 15 — EMR(1) programming

2.4.2 DDR2 SDRAM extended mode registers (EMR(#)) (cont’d)

2.4.2.4 EMR(2)

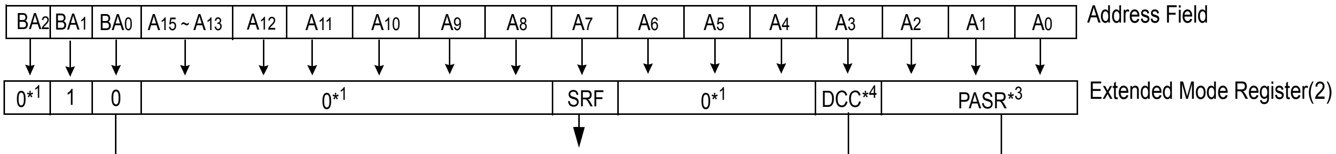
The extended mode register(2) controls refresh related features. The default value of the extended mode register(2) is not defined, therefore the extended mode register(2) must be programmed during initialization for proper operation. The extended mode register(2) is written by asserting LOW on $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, HIGH on BA1 and LOW on BA0, while controlling the states of address pins A0 - A15. The DDR2 SDRAM should be in all bank precharge state with CKE already HIGH prior to writing into the extended mode register(2). The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register(2). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state.

2.4.2.5 EMR(2) programming

Figure 16 shows the EMR(2) programming.

2.4.2 DDR2 SDRAM extended mode registers (EMR(#)) (cont'd)

2.4.2.5 EMR(2) programming



A7	High Temperature Self-Refresh Rate Enable
0	Disable
1	Enable (Optional)*2

BA1	BA0	MRS mode
0	0	MR
0	1	EMR(1)
1	0	EMR(2)
1	1	EMR(3)

A3	DCC Enable (Optional)*4
0	Disable
1	Enable

A2	A1	A0	Partial Array Self Refresh for 8 Banks (Optional)
0	0	0	Full array
0	0	1	Half Array(BA[2:0]=000,001,010&011)
0	1	0	Quarter Array(BA[2:0]=000&001)
0	1	1	1/8th array (BA[2:0] = 000)
1	0	0	3/4 array(BA[2:0]=010,011,100,101,110&111)
1	0	1	Half array(BA[2:0]=100,101,110&111)
1	1	0	Quarter array(BA[2:0]=110&111)
1	1	1	1/8th array(BA[2:0]=111)

A2	A1	A0	Partial Array Self Refresh for 4 Banks (Optional)
0	0	0	Full array
0	0	1	Half Array(BA[1:0]=00&01)
0	1	0	Quarter Array(BA[1:0]=00)
0	1	1	Not defined
1	0	0	3/4 array(BA[1:0]=01, 10&11)
1	0	1	Half array(BA[1:0]=10&11)
1	1	0	Quarter array(BA[1:0]=11)
1	1	1	Not defined

NOTE 1 BA2 and A4-A6, A8-A15 are reserved for future use and must be set to 0 when programming the EMR(2).

NOTE 2 As industry adoption of high temperature parts proceeds, users need to determine if a DRAM supports High Temperature Self-Refresh Rate Enable mode before attempting to use it in that mode. JEDEC standard DDR2 SDRAM Module user can look at DDR2 SDRAM Module SPD field Byte 49 bit [0]. If the high temperature self-refresh mode is supported then controller can set the EMR(2)[A7] bit to enable the self-refresh rate in case of higher than 85 °C temperature self-refresh operation. For the loose part user, please refer to DRAM Manufacturer's part number and data sheet to check the high temperature self-refresh rate availability.

NOTE 3 Optional in DDR2 SDRAM. If PASR (Partial Array Self Refresh) is enabled, data located in areas of the array beyond the specified address range will be lost if self refresh is entered. Data integrity will be maintained if tREF conditions are met and no Self Refresh command is issued. If the PASR feature is not supported, EMR(2)[A0-A2] must be set to 000 when programming EMR(2).

NOTE 4 Optional in DDR2 SDRAM. JEDEC standard DDR2 SDRAM may or may not have DCC (Duty Cycle Corrector) implemented, and in some of the DRAMs implementing DCC, user may be given the controllability of DCC thru EMR(2)[A3] bit. JEDEC standard DDR2 SDRAM users can look at manufacturer's data sheet to check if the DRAM part supports DCC controllability. If Optional DCC Controllability is supported, user may enable or disable the DCC by programming EMR(2)[A3] accordingly. If the controllability feature is not supported, EMR(2)[A3] must be set to 0 when programming EMR(2).

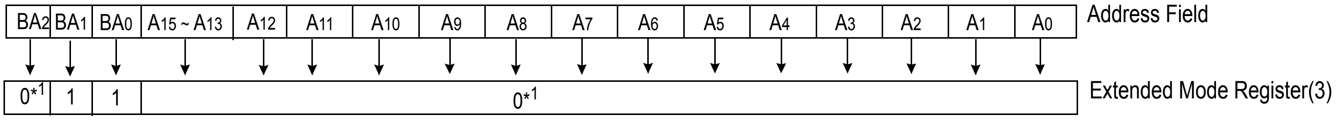
Figure 16 — EMR(2) programming

2.4.2 DDR2 SDRAM extended mode registers (EMR(#)) (cont'd)

2.4.2.6 EMR(3)

No function is defined in extended mode register(3). The default value of the extended mode register(3) is not defined, therefore the extended mode register(3) must be programmed during initialization for proper operation.

2.4.2.7 EMR(3) programming



NOTE 1 All bits in EMR(3) except BA0 and BA1 are reserved for future use and must be set to 0 when programming the EMR(3).

Figure 17 — EMR(3) programming

2.4.3 Off-chip driver (OCD) impedance adjustment

DDR2 SDRAM supports driver calibration feature and the flow chart in Figure 18 is an example of sequence. Every calibration mode command should be followed by "OCD calibration mode exit" before any other command being issued. All MR should be programmed before entering OCD impedance adjustment and ODT (On Die Termination) should be carefully controlled depending on system environment.

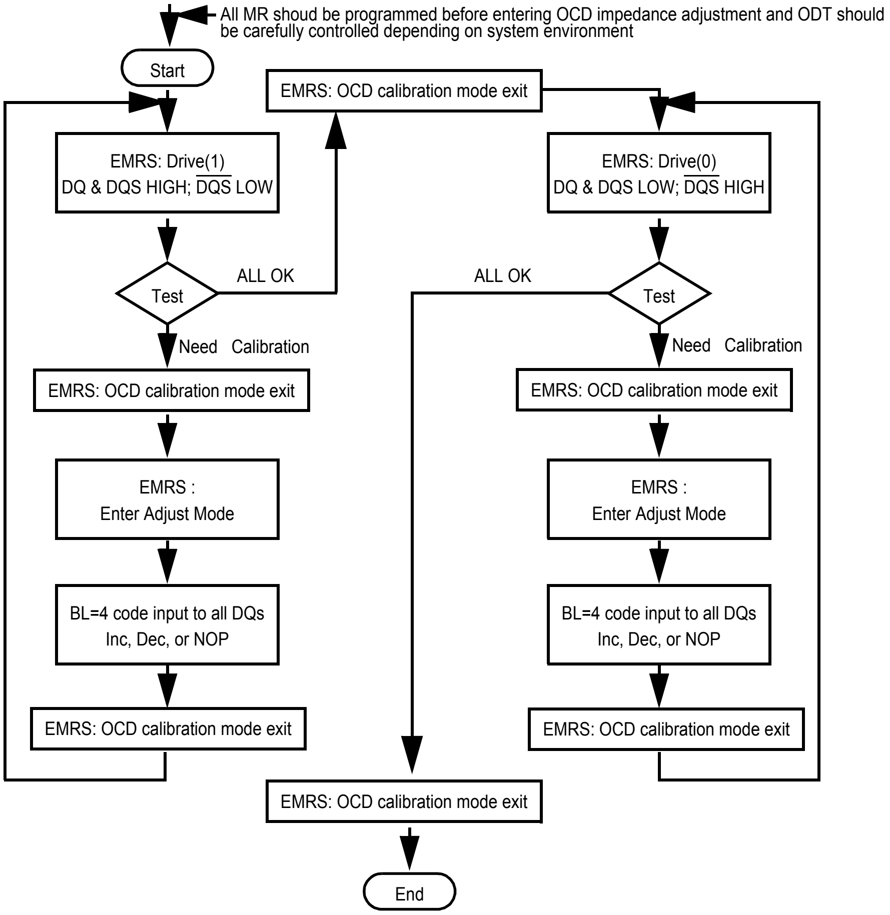


Figure 18 — OCD impedance adjustment

2.4.3.1 Extended mode register for OCD impedance adjustment

OCD impedance adjustment can be done using the following EMRS mode. In drive mode all outputs are driven out by DDR2 SDRAM and drive of RDQS is dependent on $\overline{\text{EMR}}$ bit enabling RDQS operation. In Drive(1) mode, all DQ, DQS (and RDQS) signals are driven HIGH and all $\overline{\text{DQS}}$ signals are driven LOW. In drive(0) mode, all DQ, DQS

2.4.3 Off-chip driver (OCD) impedance adjustment (cont'd)

2.4.3.1 Extended mode register for OCD impedance adjustment (cont'd)

(and RDQS) signals are driven LOW and all $\overline{\text{DQS}}$ signals are driven HIGH. In adjust mode, BL = 4 of operation code data must be used. In case of OCD calibration default, output driver characteristics have a nominal impedance value of 18 Ω during nominal temperature and voltage conditions. Output driver characteristics for OCD calibration default are specified in Tables 30 and 31. OCD applies only to normal full strength output drive setting defined by EMR(1) and if reduced strength is set, OCD default output driver characteristics are not applicable. When OCD calibration adjust mode is used, OCD default output driver characteristics are not applicable. After OCD calibration is completed or driver strength is set to default, subsequent EMRS commands not intended to adjust OCD characteristics must specify A9-A7 as '000' in order to maintain the default or calibrated value.

Table 7 — OCD drive mode program

A9	A8	A7	Operation
0	0	0	OCD calibration mode exit
0	0	1	Drive(1) DQ, DQS, (RDQS) HIGH and $\overline{\text{DQS}}$ LOW
0	1	0	Drive(0) DQ, DQS, (RDQS) LOW and $\overline{\text{DQS}}$ HIGH
1	0	0	Adjust mode
1	1	1	OCD calibration default

2.4.3.2 OCD impedance adjust

To adjust output driver impedance, controllers must issue the ADJUST EMRS command along with a 4bit burst code to DDR2 SDRAM as in Table 8. For this operation, Burst Length has to be set to BL = 4 via MRS command before activating OCD and controllers must drive this burst code to all DQs at the same time. DT0 in table 8 means all DQ bits at bit time 0, DT1 at bit time 1, and so forth. The driver output impedance is adjusted for all DDR2 SDRAM DQs simultaneously and after OCD calibration, all DQs and DQS's of a given DDR2 SDRAM will be adjusted to the same driver strength setting. The maximum step count for adjustment is 16 and when the limit is reached, further increment or decrement code has no effect. The default setting may be any step within the 16 step range. When Adjust mode command is issued, AL from previously set value must be applied.

Table 8 — OCD adjust mode program

4bit burst code inputs to all DQs				Operation	
D_{T0}	D_{T1}	D_{T2}	D_{T3}	Pull-up driver strength	Pull-down driver strength
0	0	0	0	NOP (No operation)	NOP (No operation)
0	0	0	1	Increase by 1 step	NOP
0	0	1	0	Decrease by 1 step	NOP
0	1	0	0	NOP	Increase by 1 step
1	0	0	0	NOP	Decrease by 1 step
0	1	0	1	Increase by 1 step	Increase by 1 step
0	1	1	0	Decrease by 1 step	Increase by 1 step
1	0	0	1	Increase by 1 step	Decrease by 1 step
1	0	1	0	Decrease by 1 step	Decrease by 1 step
Other Combinations				Reserved	

For proper operation of adjust mode, WL = RL - 1 = AL + CL - 1 clocks and tDS/tDH should be met as shown in Figure 19. For input data pattern for adjustment, DT0 - DT3 is a fixed order and is not affected by burst type (i.e., sequential or interleave).

2.4.3 Off-chip driver (OCD) impedance adjustment (cont'd)

2.4.3.2 OCD impedance adjust (cont'd)

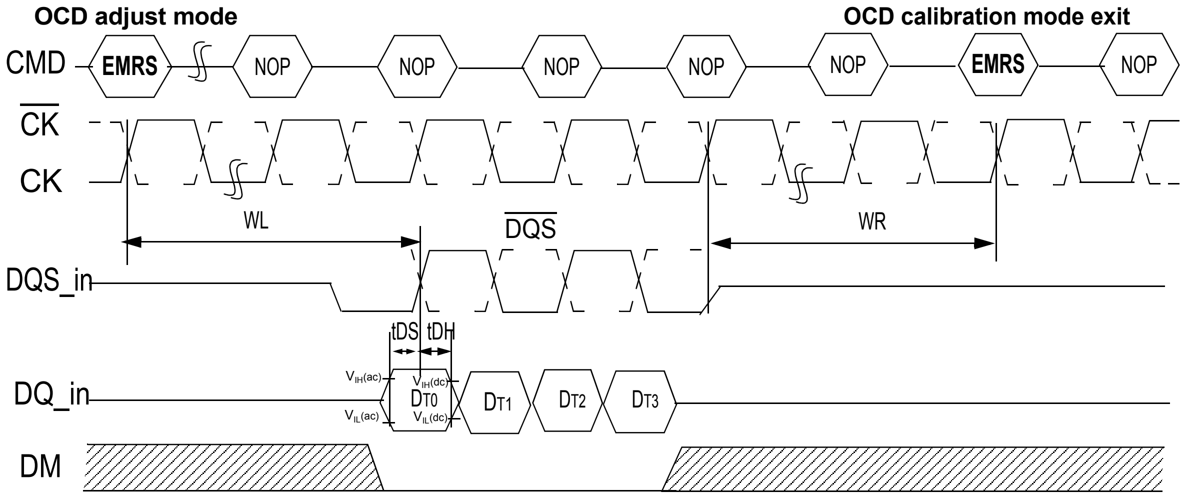


Figure 19 — OCD adjust mode

2.4.3.3 Drive mode

Drive mode, both Drive(1) and Drive(0), is used for controllers to measure DDR2 SDRAM Driver impedance. In this mode, all outputs are driven out tOIT after "enter drive mode" command and all output drivers are turned-off tOIT after "OCD calibration mode exit" command as shown in Figure 20..

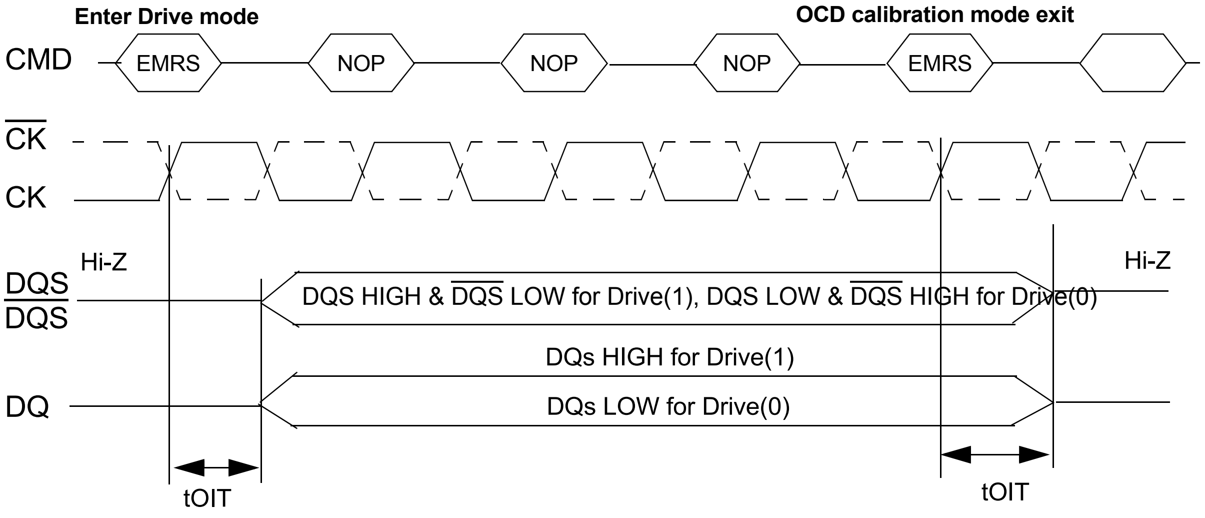


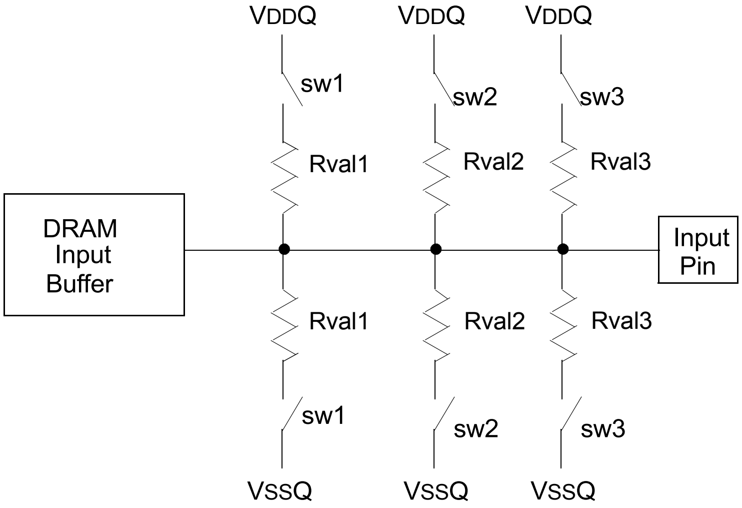
Figure 20 — OCD drive mode

2.4 Programming the mode and extended mode registers (cont'd)

2.4.4 ODT (on-die termination)

On Die Termination (ODT) is a feature that allows a DRAM to turn on/off termination resistance for each DQ, DQS/$\overline{\text{DQS}}$, RDQS/$\overline{\text{RDQS}}$, and DM signal for x4/x8 configurations via the ODT control pin. For x16 configuration ODT is applied to each DQ, UDQS/$\overline{\text{UDQS}}$, LDQS/$\overline{\text{LDQS}}$, UDM, and LDM signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT function is supported for ACTIVE and STANDBY modes. ODT is turned off and not supported in SELF REFRESH mode.



Switch (sw1, sw2, sw3) is enabled by ODT pin.
Selection among sw1, sw2, and sw3 is determined by "Rtt (nominal)" in EMR.
Termination included on all DQs, DM, DQS, $\overline{\text{DQS}}$, RDQS, and $\overline{\text{RDQS}}$ pins.

Figure 21 — Functional representation of ODT

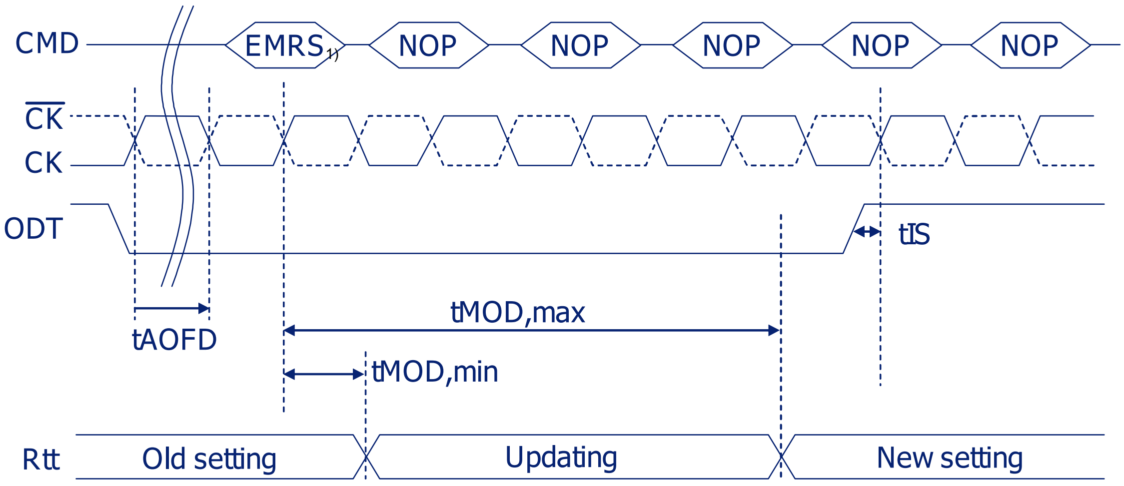
2.4.5 ODT related timings

2.4.5.1 MRS command to ODT update delay

During normal operation the value of the effective termination resistance can be changed with an EMRS command. The update of the Rtt setting is done between tMOD,min and tMOD,max, and CKE must remain HIGH for the entire duration of tMOD window for proper operation. The timings are shown in the following timing diagram.

2.4.5 ODT related timings (cont'd)

2.4.5.1 MRS command to ODT update delay (cont'd)



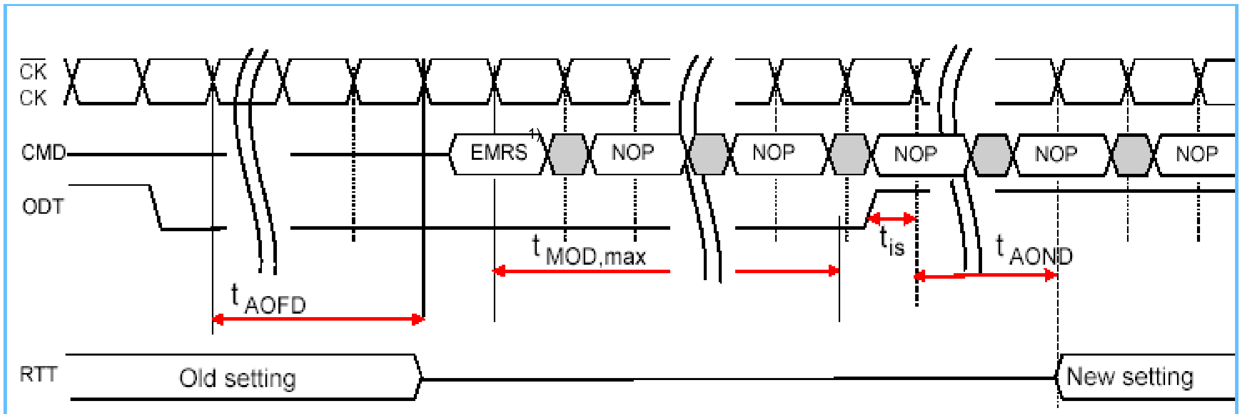
1) EMRS command directed to EMR(1), which updates the information in EMR(1)[A6,A2], i.e. Rtt (Nominal).
2) "setting' in this diagram is the Register and I/O setting, not what is measured from outside.

Figure 22 — ODT update delay timing - tMOD

However, to prevent any impedance glitch on the channel, the following conditions must be met.

- tAOFD must be met before issuing the EMRS command
- ODT must remain LOW for the entire duration of tMOD window, until tMOD,max is met

Now the ODT is ready for normal operation with the new setting, and the ODT signal may be raised again to turned on the ODT. Following timing diagram shows the proper Rtt update procedure.



1) EMRS command directed to EMR(1), which updates the information in EMR(1)[A6,A2], i.e. Rtt (Nominal).
2) "setting' in this diagram is what is measured from outside.

Figure 23 — ODT update delay timing - tMOD, as measured from outside

2.4.5 ODT related timings (cont'd)

2.4.5.2 ODT On/Off timings

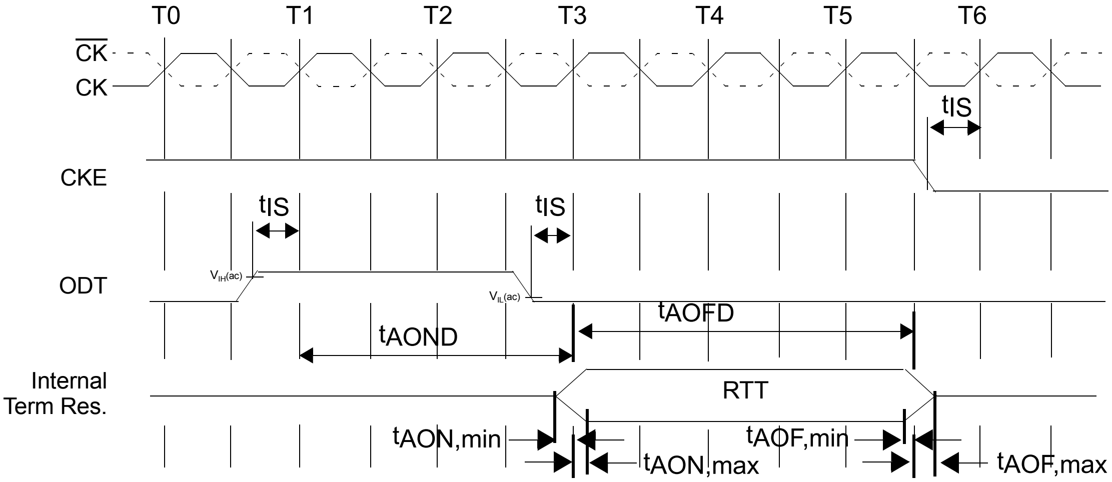


Figure 24 — ODT timing for active/standby mode

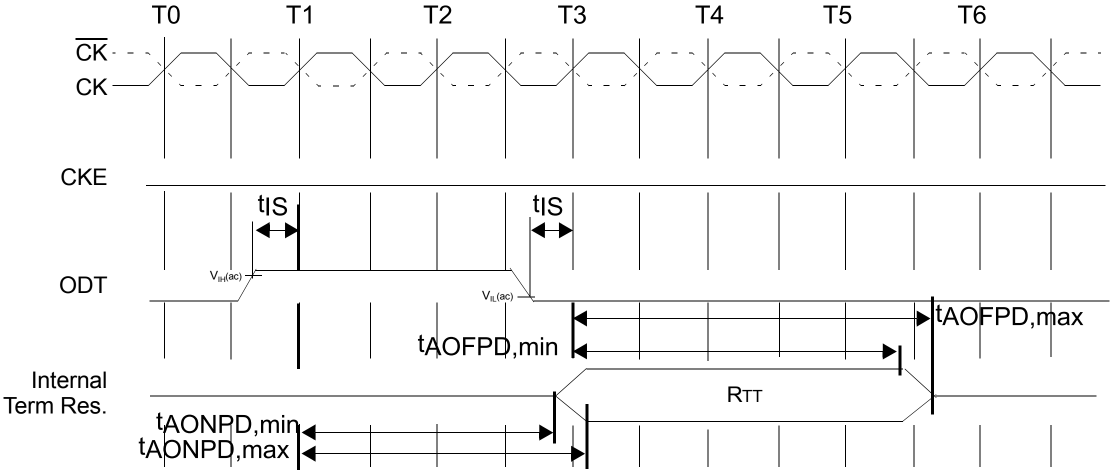


Figure 25 — ODT timing for power-down mode

2.4.5 ODT related timings (cont'd)

2.4.5.2 ODT On/Off timings (cont'd)

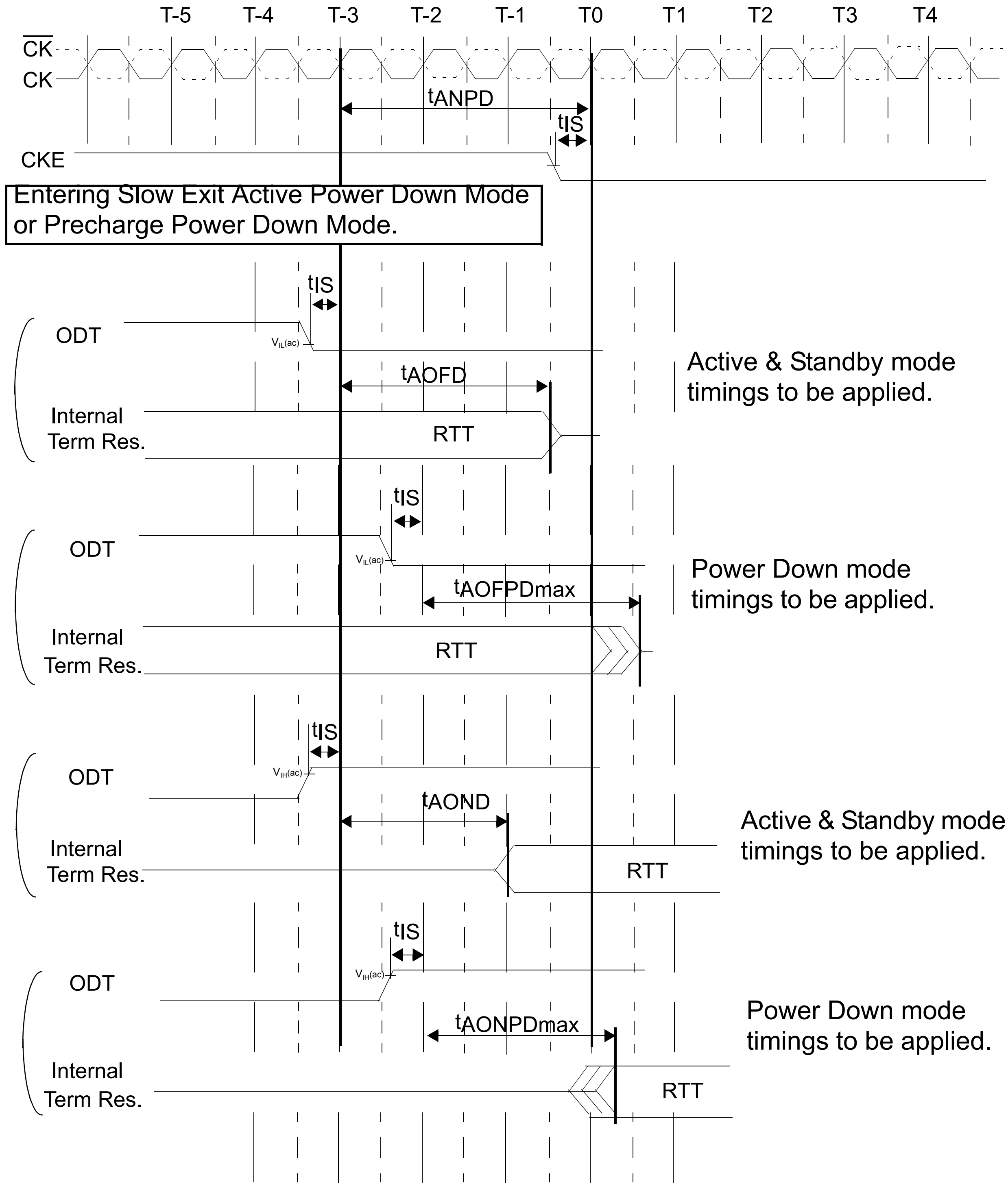


Figure 26 — ODT timing mode switch at entering power-down mode

2.4.5 ODT related timings (cont'd)

2.4.5.2 ODT On/Off timings (cont'd)

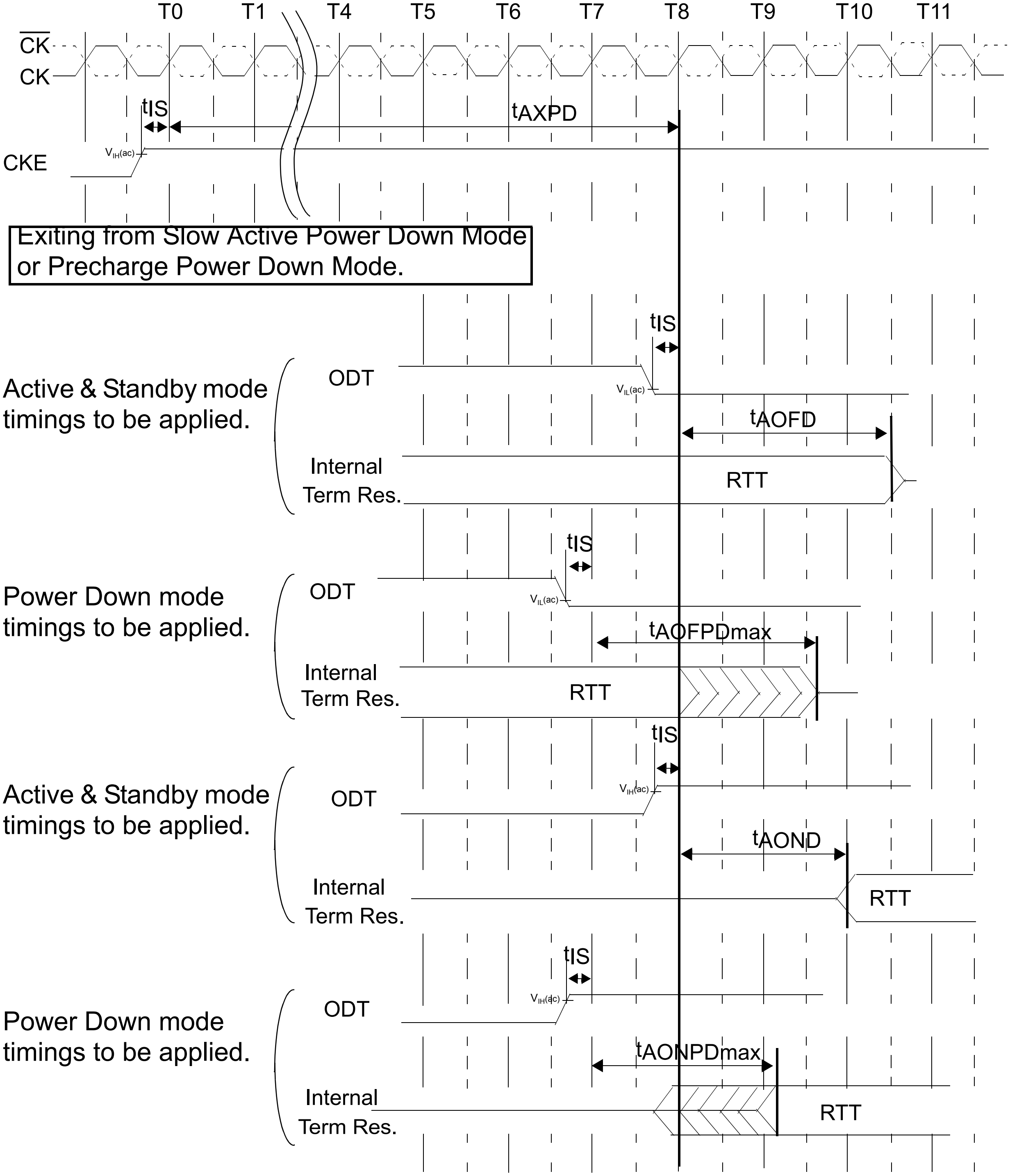


Figure 27 — ODT timing mode switch at exiting power-down mode

2.5 Bank activate command

The Bank Activate command is issued by holding $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ HIGH with $\overline{\text{CS}}$ and $\overline{\text{RAS}}$ LOW at the rising edge of the clock. The bank addresses BA0- BA2 are used to select the desired bank. The row address A0 through A15 is used to determine which row to activate in the selected bank. The Bank Activate command must be applied before any Read or Write operation can be executed. Immediately after the bank active command, the DDR2 SDRAM can accept a read or write command on the following clock cycle. If a Read/Write command is issued to a bank that has not satisfied the tRCDmin specification, then additive latency must be programmed into the device to delay when the Read/Write command is internally issued to the device. The additive latency value must be chosen to assure tRCDmin is satisfied. Additive latencies of 0, 1, 2, 3, 4 and optionally 5 are supported. Once a bank has been activated it must be precharged before another Bank Activate command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive Bank Activate commands to the same bank is determined by the RAS cycle time of the device (t_{RC}). The minimum time interval between Bank Activate commands is t_{RRD}.

In order to ensure that 8 bank devices do not exceed the instantaneous current supplying capability of 4 bank devices, certain restrictions on operation of the 8 bank devices must be observed. There are two rules. One for restricting the number of sequential ACT commands that can be issued and another for allowing more time for $\overline{\text{RAS}}$ precharge for a Precharge All command. The rules are as follows:

- 8 bank device Sequential Bank Activation Restriction : No more than 4 banks may be activated in a rolling tFAW window. Converting to clocks is done by dividing tFAW[ns] by tCK[ns] or tCK(avg)[ns], depending on the speed bin, and rounding up to next integer value. As an example of the rolling window, if RU{ (tFAW / tCK) } or RU{ (tFAW / tCK(avg) } is 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued at or between clock N+1 and N+9.
- 8 bank device Precharge All Allowance : tRP for a Precharge All command for an 8 Bank device will equal to tRP + 1 x tCK or tnRP + 1 x nCK, depending on the speed bin, where tnRP = RU{ tRP / tCK(avg) } and tRP is the value for a single bank precharge.

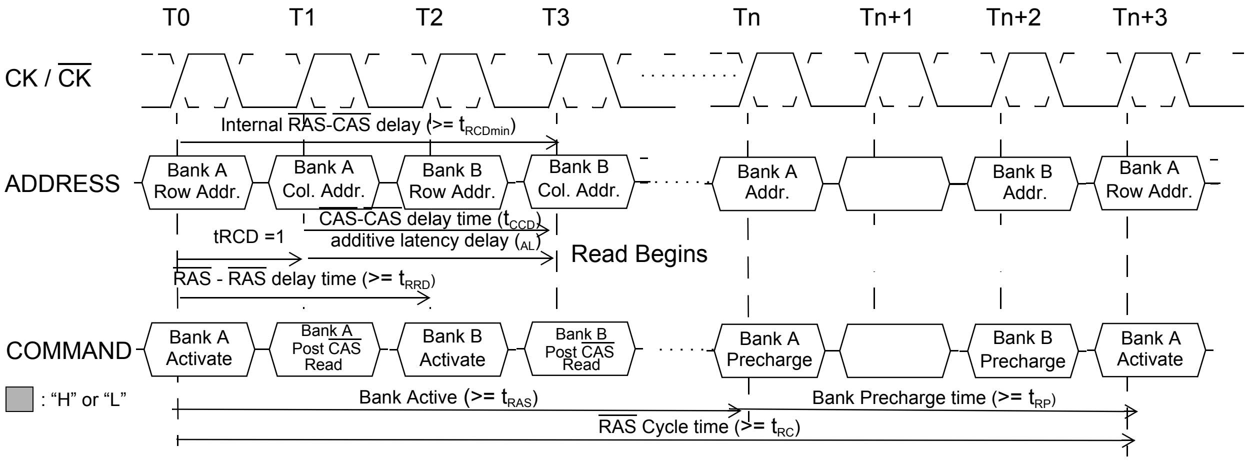


Figure 28 — Bank activate command cycle: tRCD = 3, AL = 2, tRP = 3, tRRD = 2, tCCD = 2

2.6 Read and write access modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting $\overline{\text{RAS}}$ HIGH, $\overline{\text{CS}}$ and $\overline{\text{CAS}}$ LOW at the clock's rising edge. $\overline{\text{WE}}$ must also be defined at this time to determine whether the access cycle is a read operation ($\overline{\text{WE}}$ HIGH) or a write operation ($\overline{\text{WE}}$ LOW).

The DDR2 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a serial read or write operation on successive clock cycles. The boundary of the burst cycle is strictly restricted to specific segments of the page length. For example, the 32 Mbit x 4 I/O x 4 Bank chip has a page length of 2048 bits (defined by CA0-CA9, CA11). The page length of 2048 is divided into 512 or 256 uniquely addressable boundary segments depending on burst length, 512 for 4 bit burst, 256 for 8 bit burst respectively. A 4-bit or 8-bit burst operation will

2 Functional description (cont'd)
2.6 Read and write access modes (cont'd)

occur entirely within one of the 512 or 256 groups beginning with the column address supplied to the device during the Read or Write Command (CA0-CA9, CA11). The second, third and fourth access will also occur within this group segment, however, the burst order is a function of the starting address, and the burst sequence.

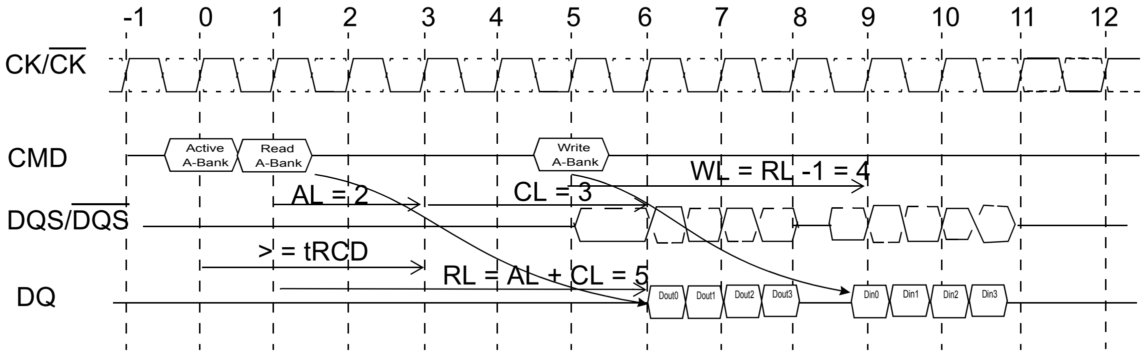
A new burst access must not interrupt the previous 4 bit burst operation in case of BL = 4 setting. However, in case of BL = 8 setting, two cases of interrupt by a new burst access are allowed, one reads interrupted by a read, the other writes interrupted by a write with 4 bit burst boundary respectively. The minimum $\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ delay is defined by tCCD, and is a minimum of 2 clocks for read or write cycles.

2.6.1 Posted $\overline{\text{CAS}}$

Posted $\overline{\text{CAS}}$ operation is supported to make command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. In this operation, the DDR2 SDRAM allows a $\overline{\text{CAS}}$ read or write command to be issued immediately after the $\overline{\text{RAS}}$ bank activate command (or any time during the $\overline{\text{RAS}}$-$\overline{\text{CAS}}$-delay time, tRCD, period). The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of AL and the $\overline{\text{CAS}}$ latency (CL). Therefore if a user chooses to issue a Read/Write command before the tRCDmin, then AL (greater than 0) must be written into the EMR(1). The Write Latency (WL) is always defined as RL - 1 (read latency -1) where read latency is defined as the sum of additive latency plus $\overline{\text{CAS}}$ latency (RL=AL+CL). Read or Write operations using AL allow seamless bursts (refer to seamless operation timing diagram examples in Read burst and Write burst section)

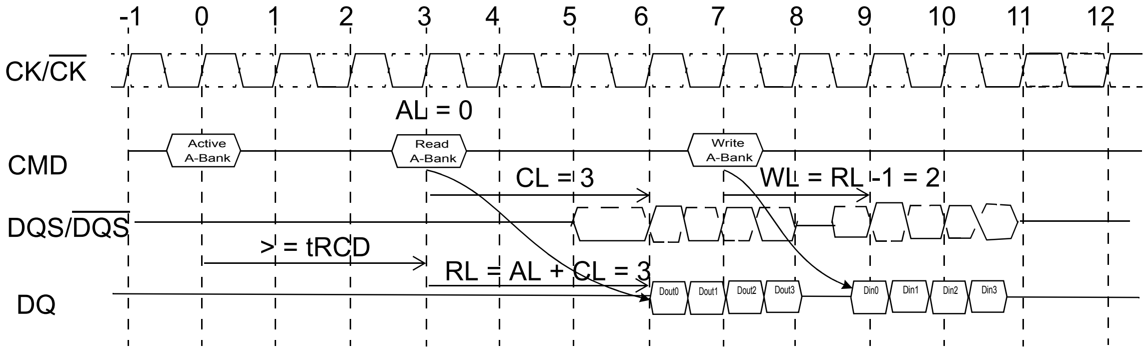
2.6.1.1 Examples of posted $\overline{\text{CAS}}$ operation

Examples of a read followed by a write to the same bank where AL = 2 and where AL = 0 are shown in Figures 29 and 30, respectively.



[AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL - 1) = 4, BL = 4]

Figure 29 — Example 1: Read followed by a write to the same bank, where AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL - 1) = 4, BL = 4



AL = 0 and CL = 3, RL = (AL + CL) = 3, WL = (RL - 1) = 2, BL = 4]

Figure 30 — Example 2: Read followed by a write to the same bank, where AL = 0 and CL = 3, RL = (AL + CL) = 3, WL = (RL - 1) = 2, BL = 4

2.6 Read and write access modes (cont'd)

2.6.2 Burst mode operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). The parameters that define how the burst mode will operate are burst sequence and burst length. DDR2 SDRAM supports 4 bit burst and 8 bit burst modes only. For 8 bit burst mode, full interleave address ordering is supported, however, sequential address ordering is nibble based for ease of implementation. The burst type, either sequential or interleaved, is programmable and defined by MR[A3], which is similar to the DDR SDRAM operation. Seamless burst read or write operations are supported. Unlike DDR devices, interruption of a burst read or write cycle during BL = 4 mode operation is prohibited. However in case of BL = 8 mode, interruption of a burst read or write operation is limited to two cases, reads interrupted by a read, or writes interrupted by a write. Therefore the Burst Stop command is not supported on DDR2 SDRAM devices.

Table 9 — Burst length and sequence

BL = 4

Burst Length	Starting Address (A1 A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
4	0 0	0, 1, 2, 3	0, 1, 2, 3
	0 1	1, 2, 3, 0	1, 0, 3, 2
	1 0	2, 3, 0, 1	2, 3, 0, 1
	1 1	3, 0, 1, 2	3, 2, 1, 0

BL = 8

Burst Length	Starting Address (A2 A1 A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
8	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

NOTE Page size is a function of I/O organization and column addressing.

2.6.3 Burst read command

The Burst Read command is initiated by having $\overline{\text{CS}}$ and $\overline{\text{CAS}}$ LOW while holding $\overline{\text{RAS}}$ and $\overline{\text{WE}}$ HIGH at the rising edge of the clock. The address inputs determine the starting column address for the burst. The delay from the start of the command to when the data from the first cell appears on the outputs is equal to the value of the read latency (RL). The data strobe output (DQS) is driven LOW one clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is equal to an additive latency (AL) plus $\overline{\text{CAS}}$ latency (CL). The CL is defined by the Mode Register (MR), similar to the existing SDR and DDR SDRAMs. The AL is defined by the Extended Mode Register(1)(EMR(1)).

DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMR "Enable DQS" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at VREF. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{\text{DQS}}$. This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMR, the complementary pin, $\overline{\text{DQS}}$, must be tied externally to VSS through a 20 Ω to 10 kΩ resistor to insure proper operation.

2.6 Read and write access modes (cont'd)

2.6.3 Burst read command (cont'd)

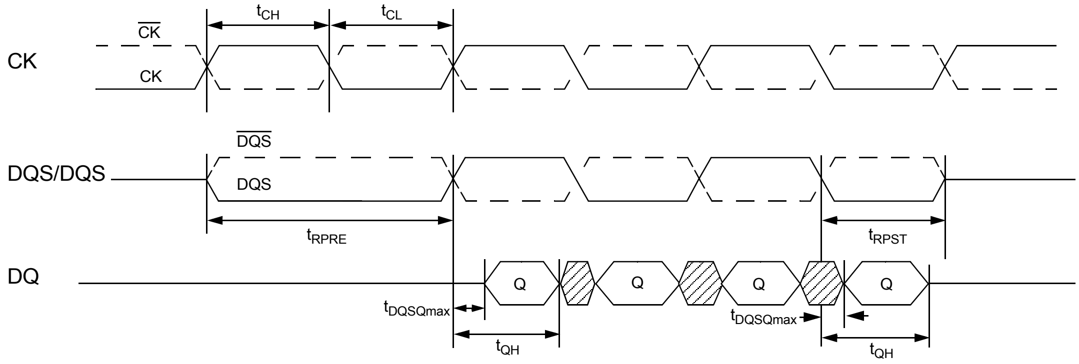


Figure 31 — Data output (read) timing

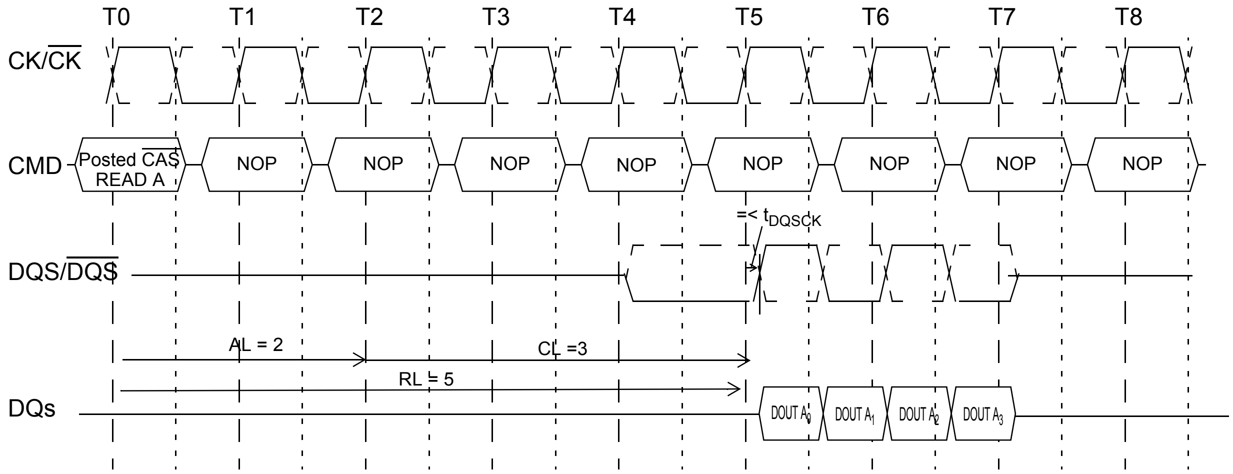


Figure 32 — Burst read operation: RL = 5 (AL = 2, CL = 3, BL = 4)

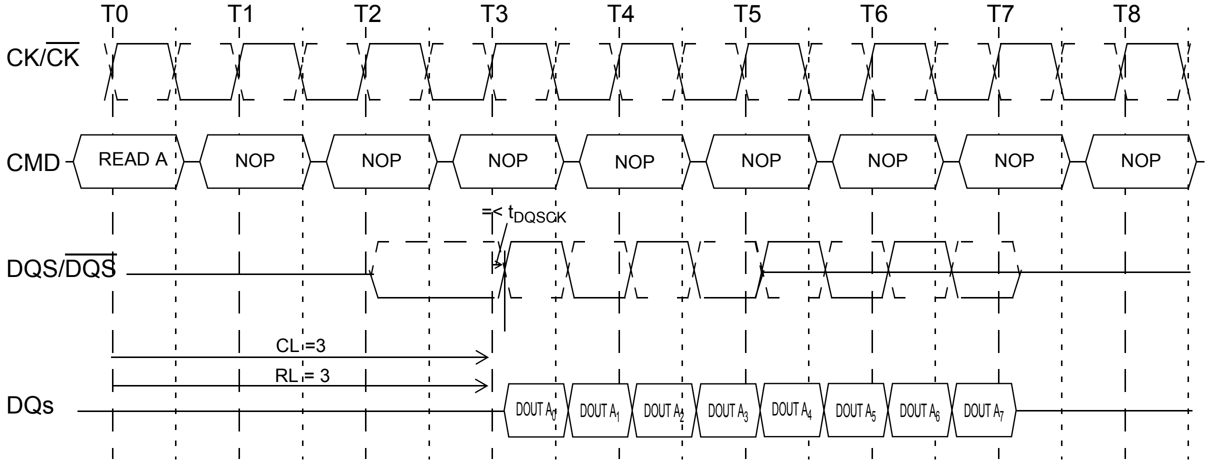


Figure 33 — Burst read operation: RL = 3 (AL = 0 and CL = 3, BL = 8)

2.6 Read and write access modes (cont'd)

2.6.3 Burst read command (cont'd)

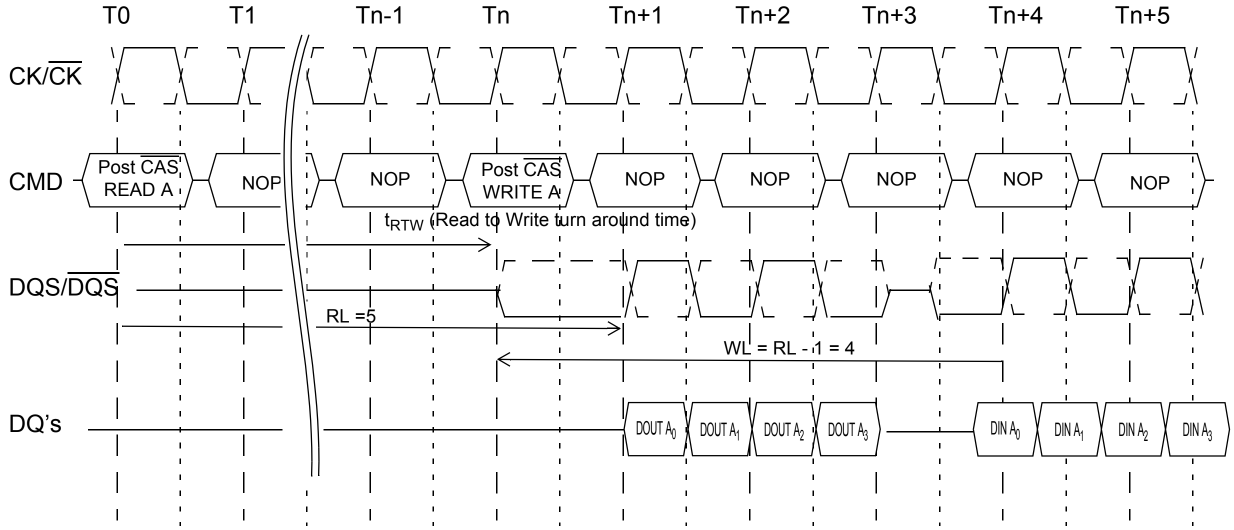


Figure 34 — Burst read followed by burst write: RL = 5, WL = (RL-1) = 4, BL = 4

The minimum time from the burst read command to the burst write command is defined by a read-to-write-turn-around-time, which is 4 clocks in case of BL = 4 operation, 6 clocks in case of BL = 8 operation.

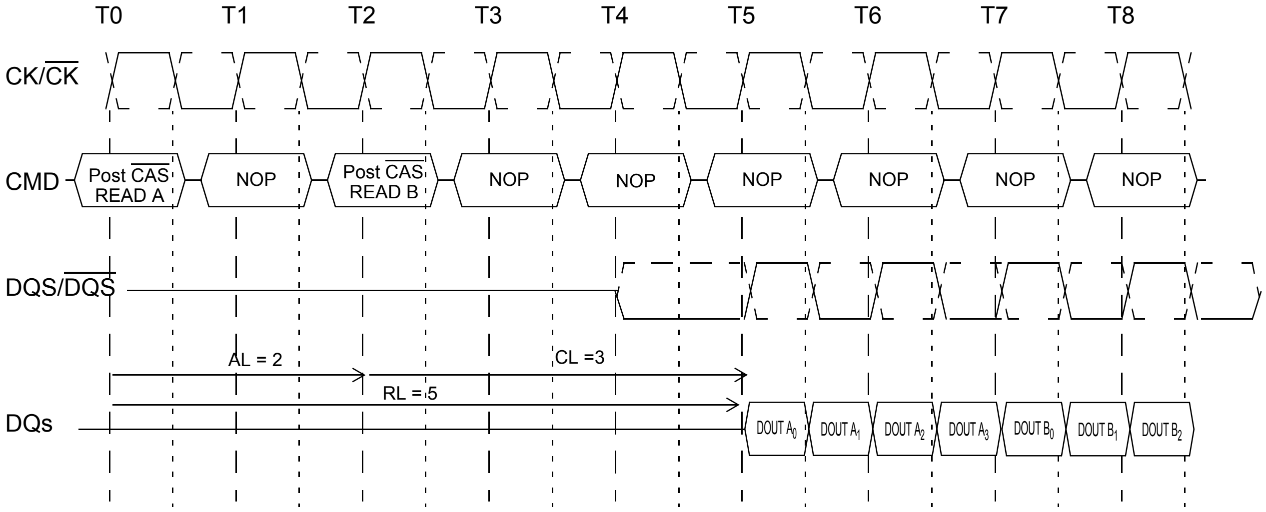


Figure 35 — Seamless burst read operation: RL = 5, AL = 2, and CL = 3, BL = 4

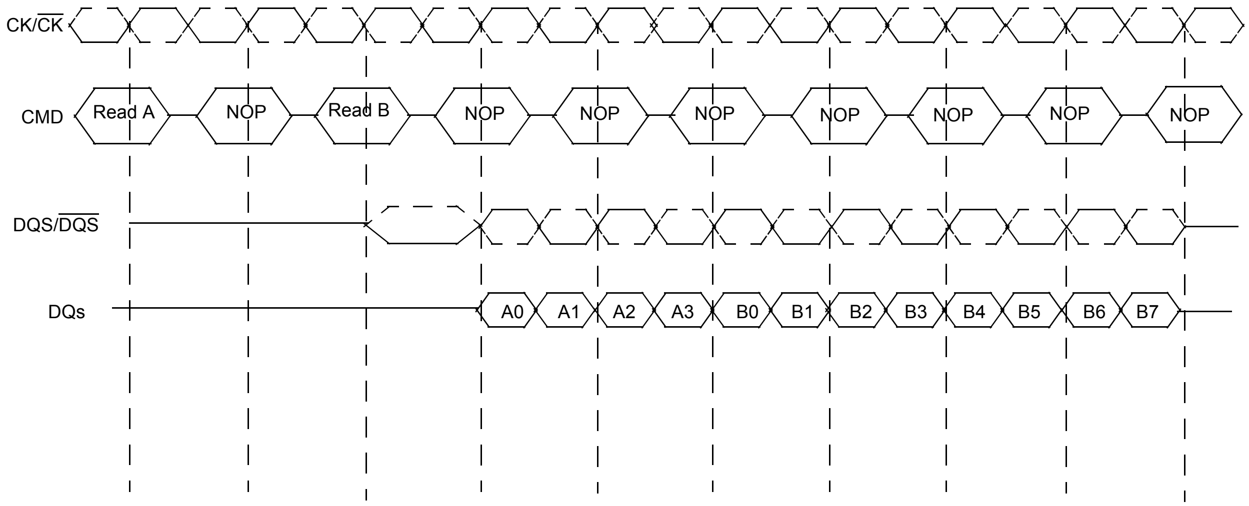
The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, and every 4 clock for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

2.6.3.1 Reads interrupted by a read

Burst read can only be interrupted by another read with 4 bit burst boundary. Any other case of read interrupt is not allowed.

2.6.3 Burst read command (cont'd)

2.6.3.1 Reads interrupted by a read (cont'd)



NOTE 1 Read burst interrupt function is only allowed on burst of 8. Burst interrupt of 4 is prohibited.

NOTE 2 Read burst of 8 can only be interrupted by another Read command. Read burst interruption by Write command or Precharge command is prohibited.

NOTE 3 Read burst interrupt must occur exactly two clocks after previous Read command. Any other Read burst interrupt timings are prohibited.

NOTE 4 Read burst interruption is allowed to any bank inside DRAM.

NOTE 5 Read burst with Auto Precharge enabled is not allowed to interrupt.

NOTE 6 Read burst interruption is allowed by another Read with Auto Precharge command.

NOTE 7 All command timings are referenced to burst length set in the mode register. They are not referenced to actual burst. For example, Minimum Read to Precharge timing is AL + BL/2 where BL is the burst length set in the mode register and not the actual burst (which is shorter because of interrupt).

Figure 36 — Read burst interrupt timing example: (CL=3, AL=0, RL=3, BL=8)

2.6.4 Burst write operation

The Burst Write command is initiated by having $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ LOW while holding $\overline{RAS}$ HIGH at the rising edge of the clock. The address inputs determine the starting column address. Write latency (WL) is defined by a read latency (RL) minus one and is equal to (AL + CL -1); and is the number of clocks of delay that are required from the time the write command is registered to the clock edge associated to the first DQS strobe. A data strobe signal (DQS) should be driven LOW (preamble) nominally half clock prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The tDQSS specification must be satisfied for each positive DQS transition to its associated clock edge during write cycles. The subsequent burst bit data are issued on successive edges of the DQS until the burst length is completed, which is 4 or 8 bit burst. When the burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ Signal is ignored after the burst write operation is complete. The time from the completion of the burst write to bank precharge is the write recovery time (WR).

DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMR "Enable DQS" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at the specified AC/DC levels (see Figure 85 on page 82, Figure 87 on page 84, Figure 89 on page 86 and Figure 91 on page 88.) In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$ (see Figure 86 on page 83, Figure 88 on page 85, Figure 90 on page 87 and Figure 92 on page 91.) This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMR, the complementary pin, $\overline{DQS}$, must be tied externally to VSS through a 20 Ω to 10 kΩ resistor to insure proper operation.

2.6 Read and write access modes (cont'd)

2.6.4 Burst write operation (cont'd)

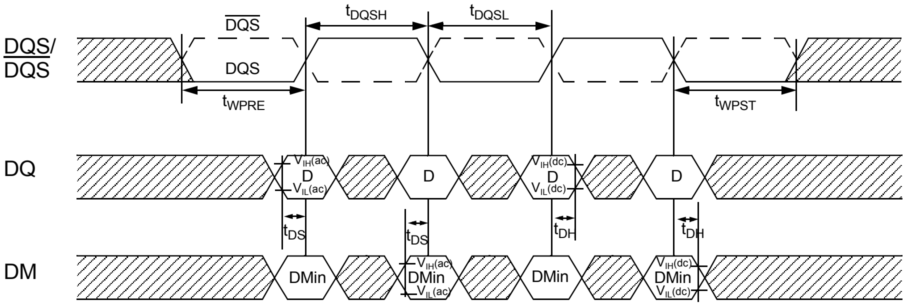


Figure 37 — Data input (write) timing

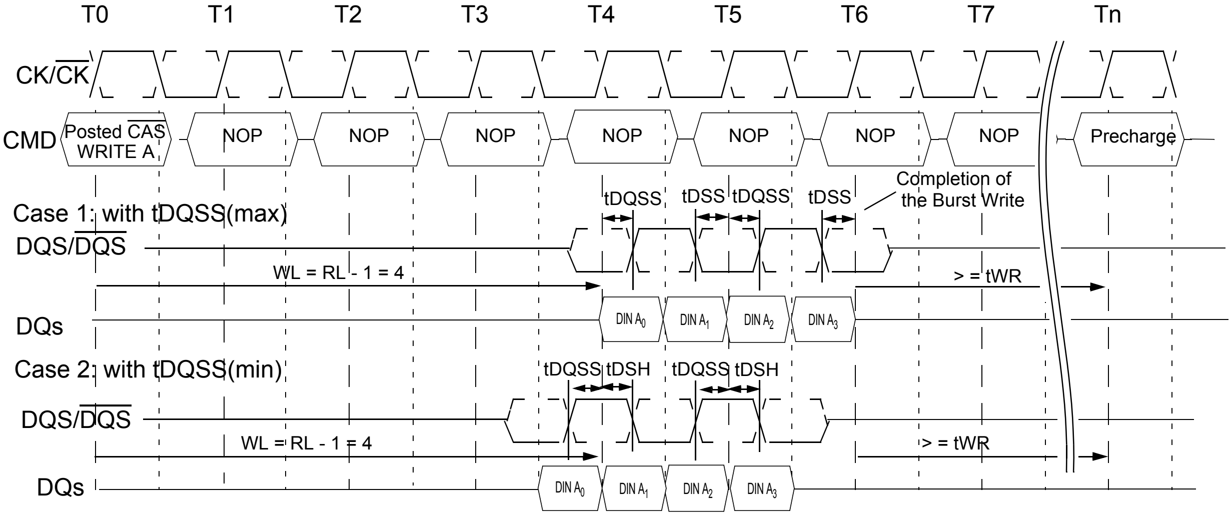


Figure 38 — Burst write operation: RL = 5 (AL=2, CL=3), WL = 4, BL = 4

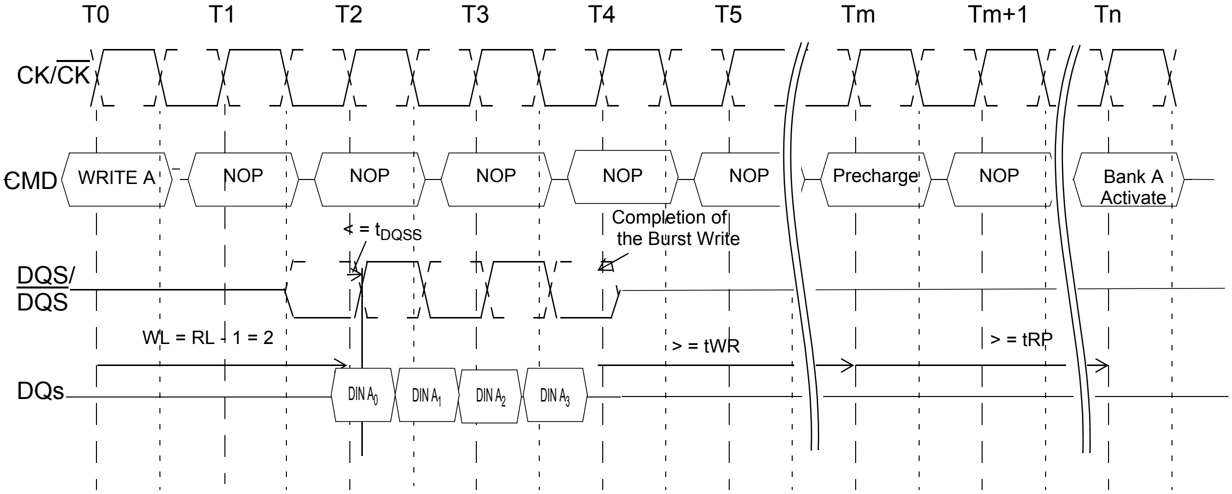
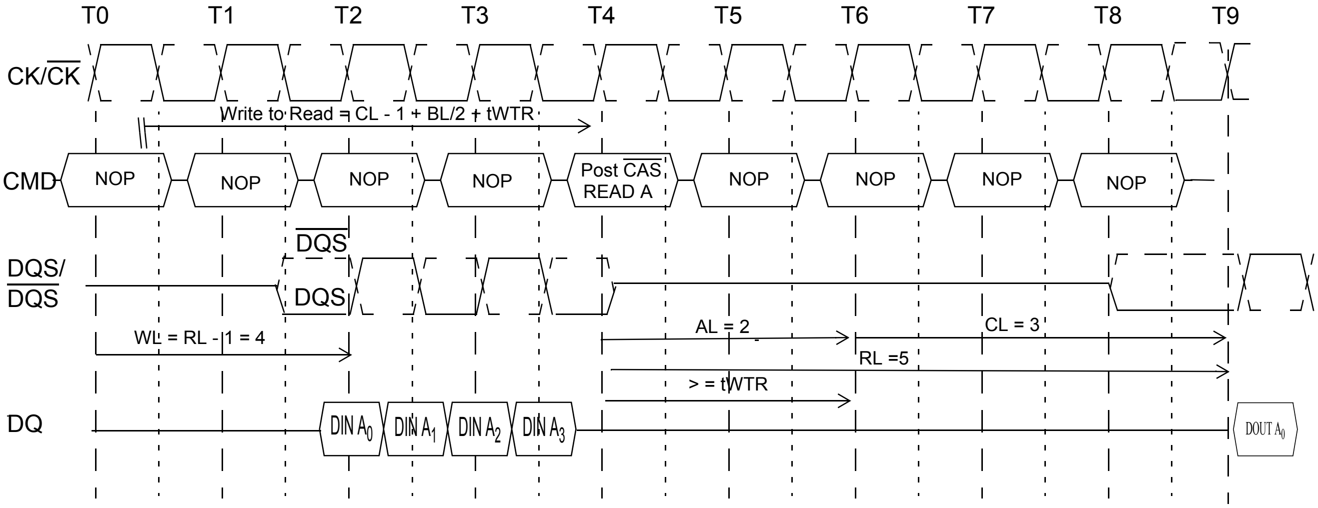


Figure 39 — Burst write operation: RL = 3 (AL=0, CL=3), WL = 2, BL = 4

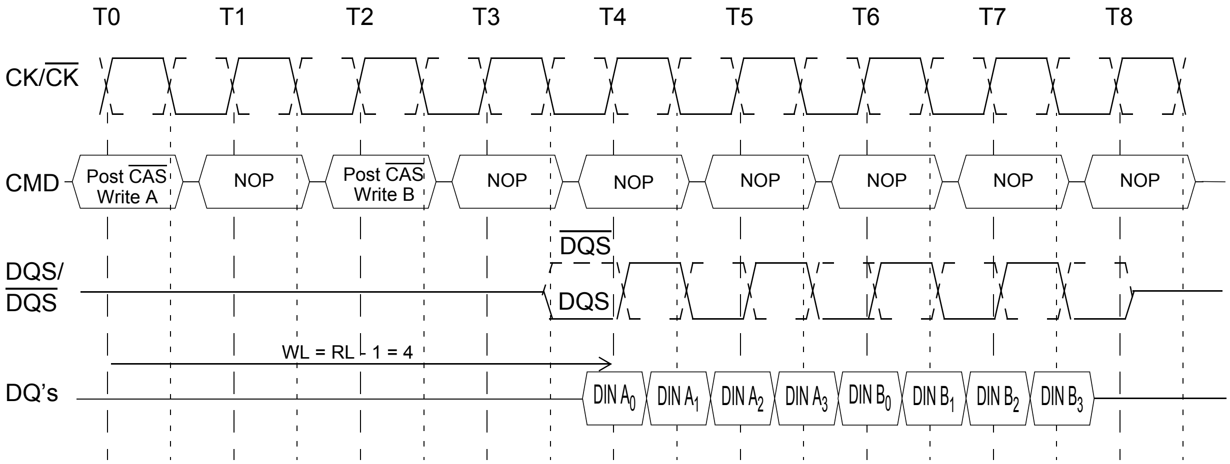
2.6 Read and write access modes (cont'd)

2.6.4 Burst write operation (cont'd)



NOTE The minimum number of clock from the burst write command to the burst read command is [CL - 1 + BL/2 + tWTR]. This tWTR is not a write recovery time (tWR) but the time required to transfer the 4bit write data from the input buffer into sense amplifiers in the array. tWTR is defined in the timing parameter table of this standard.

Figure 40 — Burst write followed by burst read: RL = 5 (AL=2, CL=3), WL = 4, tWTR = 2, BL = 4



NOTE The seamless burst write operation is supported by enabling a write command every other clock for BL = 4 operation, every four clocks for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

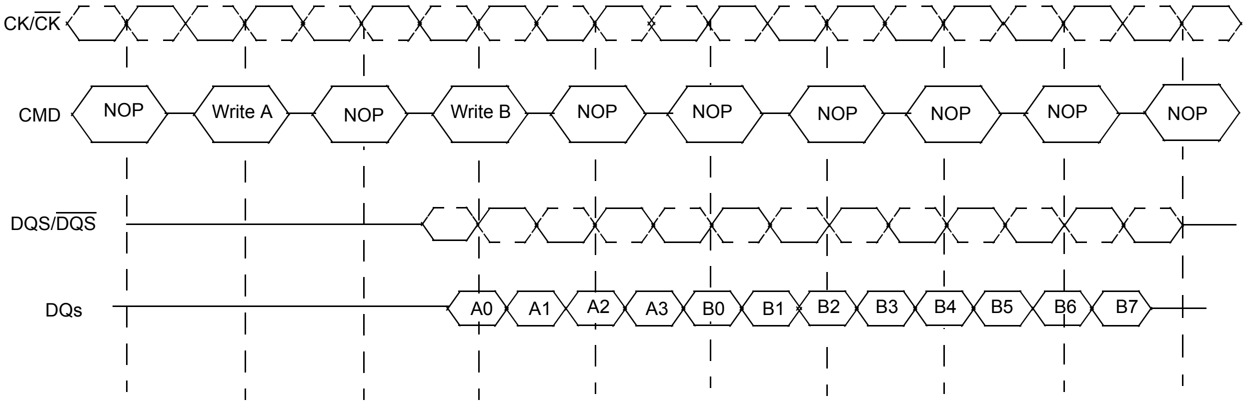
Figure 41 — Seamless burst write operation: RL = 5, WL = 4, BL = 4

2.6.4.1 Writes interrupted by a write

Burst write can only be interrupted by another write with 4 bit burst boundary. Any other case of write interrupt is not allowed.

2.6.4 Burst write operation (cont'd)

2.6.4.1 Writes interrupted by a write (cont'd)



NOTE 1 Write burst interrupt function is only allowed on burst of 8. Burst interrupt of 4 is prohibited.

NOTE 2 Write burst of 8 can only be interrupted by another Write command. Write burst interruption by Read command or Precharge command is prohibited.

NOTE 3 Write burst interrupt must occur exactly two clocks after previous Write command. Any other Write burst interrupt timings are prohibited.

NOTE 4 Write burst interruption is allowed to any bank inside DRAM.

NOTE 5 Write burst with Auto Precharge enabled is not allowed to interrupt.

NOTE 6 Write burst interruption is allowed by another Write with Auto Precharge command.

NOTE 7 All command timings are referenced to burst length set in the mode register. They are not referenced to actual burst. For example, minimum Write to Precharge timing is WL+BL/2+tWR where tWR starts with the rising clock after the uninterrupted burst end and not from the end of actual burst end.

Figure 42 — Write burst interrupt timing example: (CL=3, AL=0, RL=3, WL=2, BL=8)

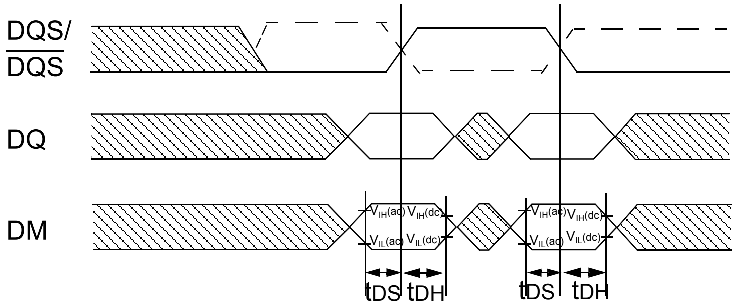
2.6.5 Write data mask

One write data mask (DM) pin for each 8 data bits (DQ) will be supported on DDR2 SDRAMs, consistent with the implementation on DDR SDRAMs. It has identical timings on write operations as the data bits, and though used in a unidirectional manner, is internally loaded identically to data bits to insure matched system timing. DM of x4 and x16 bit organization is not used during read cycles. However DM of x8 bit organization can be used as RDQS during read cycles by EMR(1) setting.

2.6 Read and write access modes (cont'd)

2.6.5 Write data mask (cont'd)

Data Mask Timing



Data Mask Function, WL=3, AL=0, BL = 4 shown

Case 1 : min tDQSS

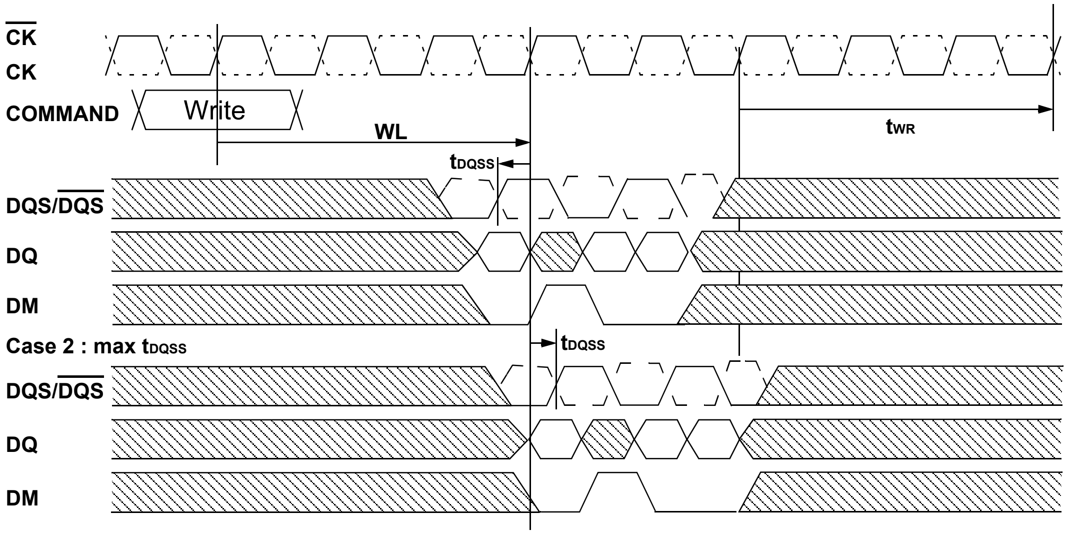


Figure 43 — Write data mask

2.7 Precharge operation

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is triggered when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are LOW and $\overline{CAS}$ is HIGH at the rising edge of the clock. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. Three address bits A10, BA0 and BA1 for 256 Mb and 512 Mb and four address bits A10, BA0 - BA2 for 1Gb and higher densities are used to define which bank to precharge when the command is issued. For 8 bank devices, refer to 2.5 Bank activate command section of this data sheet.

Table 10 — Bank selection for precharge by address bits

A10	BA2	BA1	BA0	Precharged Bank(s)	Remarks
LOW	LOW	LOW	LOW	Bank 0 only	
LOW	LOW	LOW	HIGH	Bank 1 only	
LOW	LOW	HIGH	LOW	Bank 2 only	
LOW	LOW	HIGH	HIGH	Bank 3 only	
LOW	HIGH	LOW	LOW	Bank 4 only	1 Gb and higher
LOW	HIGH	LOW	HIGH	Bank 5 only	1 Gb and higher

2 Functional description (cont'd)

2.7 Precharge operation (cont'd)

Table 10 — Bank selection for precharge by address bits (cont'd)

A10	BA2	BA1	BA0	Precharged Bank(s)	Remarks
LOW	HIGH	HIGH	LOW	Bank 6 only	1 Gb and higher
LOW	HIGH	HIGH	HIGH	Bank 7 only	1 Gb and higher
HIGH	DON'T CARE	DON'T CARE	DON'T CARE	All Banks	

2.7.1 Burst read operation followed by precharge

Minimum Read to precharge command spacing to the same bank = AL + BL/2 + max(RTP, 2) - 2 clocks

For the earliest possible precharge, the precharge command may be issued on the rising edge which is "Additive latency (AL) + BL/2 + max(RTP, 2) - 2 clocks" after a Read command. A new bank active (command) may be issued to the same bank after the RAS precharge time (t_{RP}). A precharge command cannot be issued until t_{RAS} is satisfied.

The minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a Read to Precharge command. This time is called tRTP (Read to Precharge). For BL = 4 this is the time from the actual read (AL after the Read command) to Precharge command. For BL = 8 this is the time from AL + 2 clocks after the Read to the Precharge command.

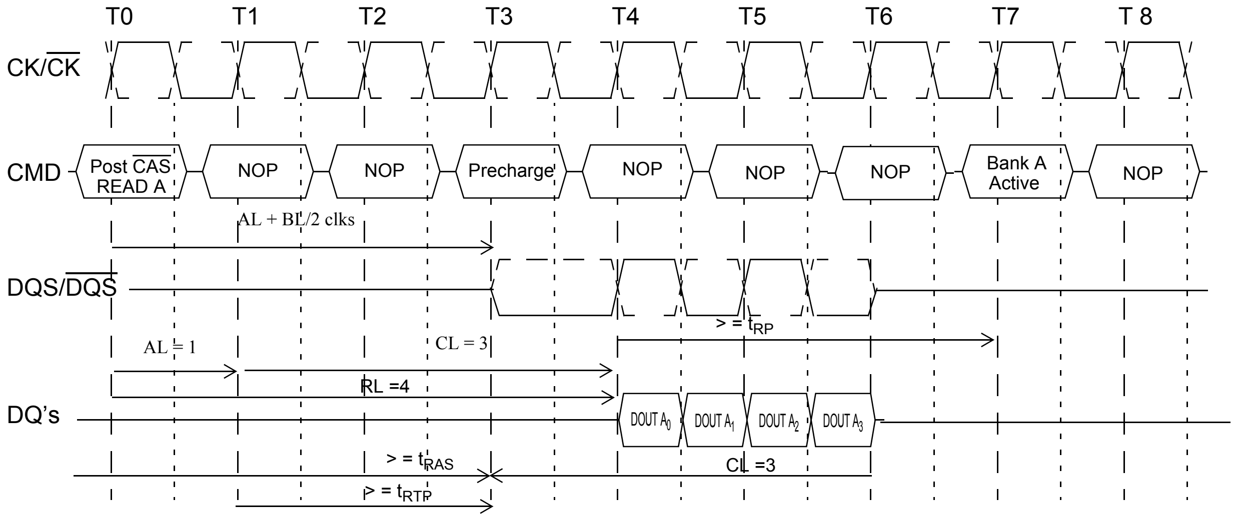


Figure 44 — Example 1: Burst read operation followed by precharge: RL = 4, AL = 1, CL = 3, BL = 4, t_{RTP} <= 2 clocks

2.7 Precharge operation (cont'd)

2.7.1 Burst read operation followed by precharge (cont'd)

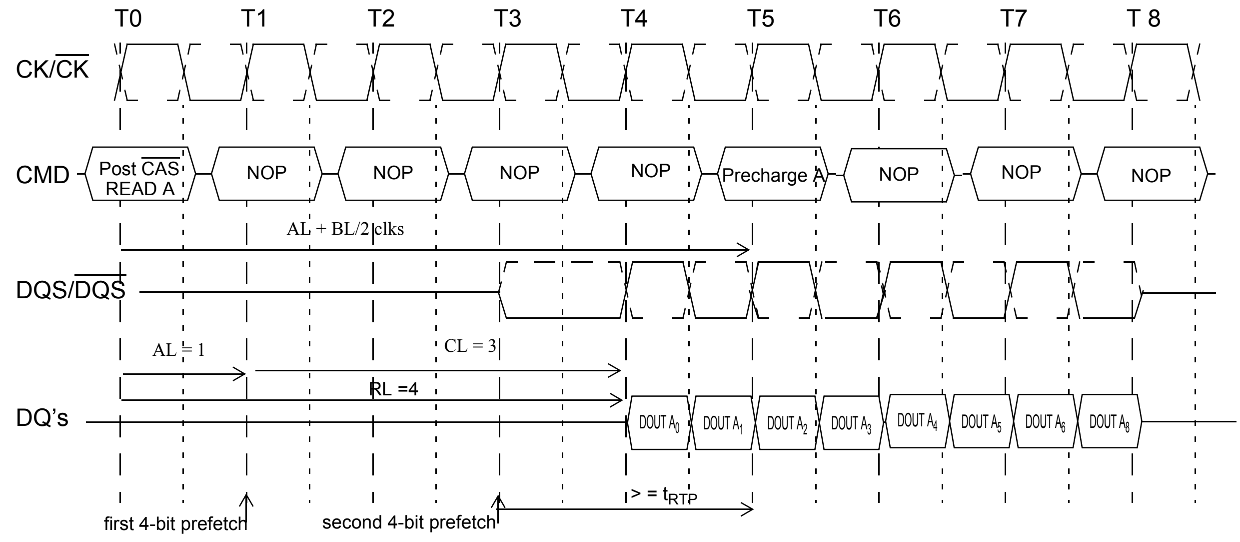


Figure 45 — Example 2: Burst read operation followed by precharge: RL = 4, AL = 1, CL = 3, BL = 8, t_{RTP} <= 2 clocks

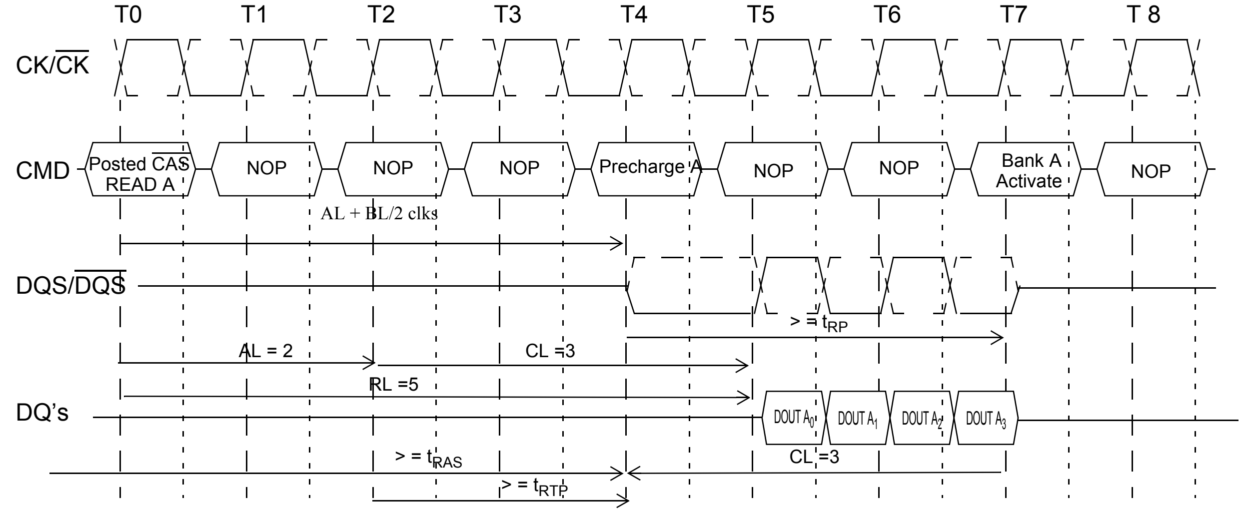


Figure 46 — Example 3: Burst read operation followed by precharge: RL = 5, AL = 2, CL = 3, BL = 4, t_{RTP} <= 2 clocks

2.7 Precharge operation (cont'd)

2.7.1 Burst read operation followed by precharge (cont'd)

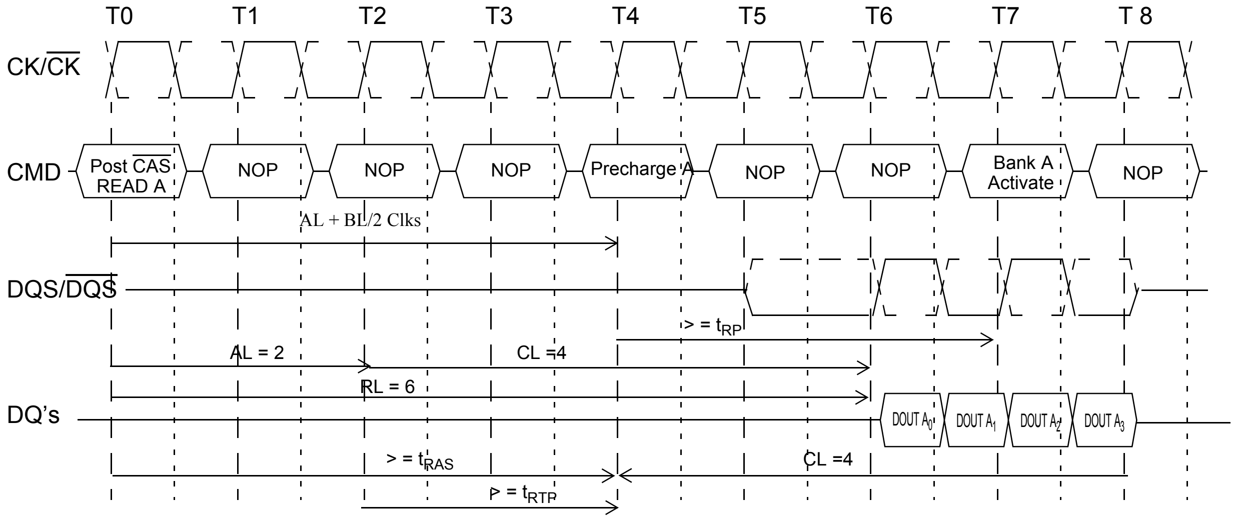
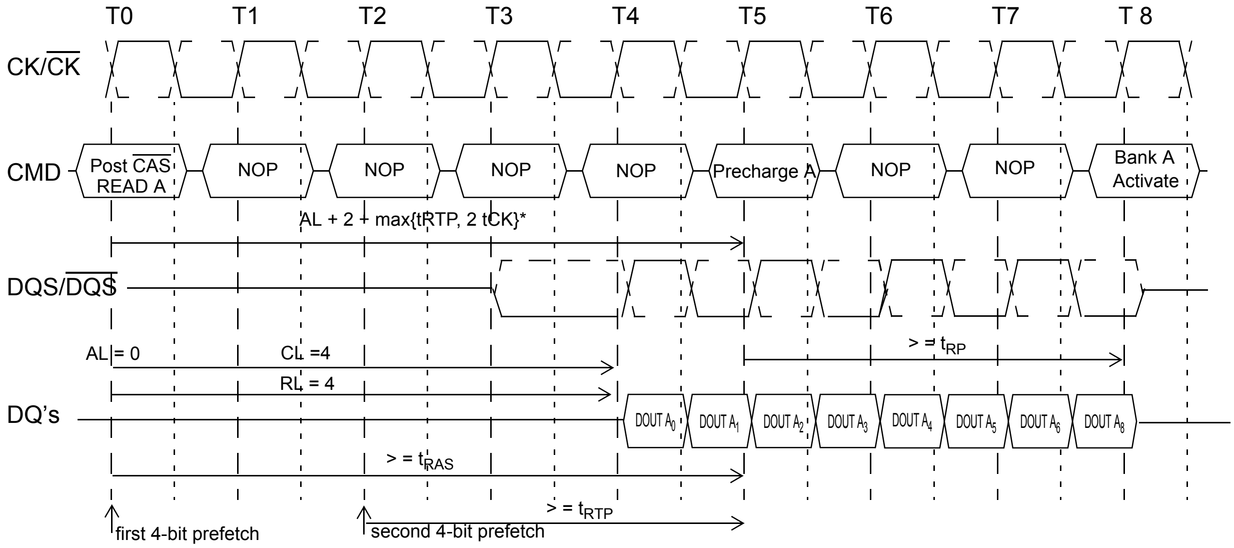


Figure 47 — Example 4: Burst read operation followed by precharge: RL = 6, AL = 2, CL = 4, BL = 4, t_{RTP} <= 2 clocks



* : rounded to next integer.

Figure 48 — Example 5: Burst read operation followed by precharge: RL = 4, AL = 0, CL = 4, BL = 8, t_{RTP} > 2 clocks

2.7.2 Burst write followed by precharge

Minimum Write to Precharge Command spacing to the same bank = WL + BL/2 clks + tWR

For write cycles, a delay must be satisfied from the completion of the last burst write cycle until the Precharge Command can be issued. This delay is known as a write recovery time (tWR) referenced from the completion of the burst write to the precharge command. No Precharge command should be issued prior to the tWR delay.

2.7 Precharge operation (cont'd)

2.7.2 Burst write followed by precharge (cont'd)

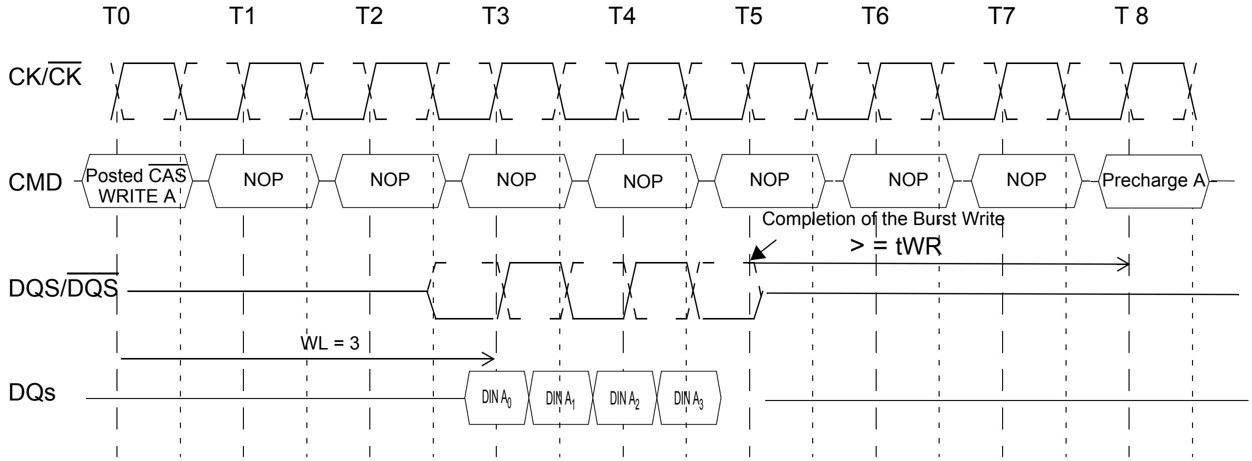


Figure 49 — Example 1: Burst write followed by precharge: WL = (RL-1) =3

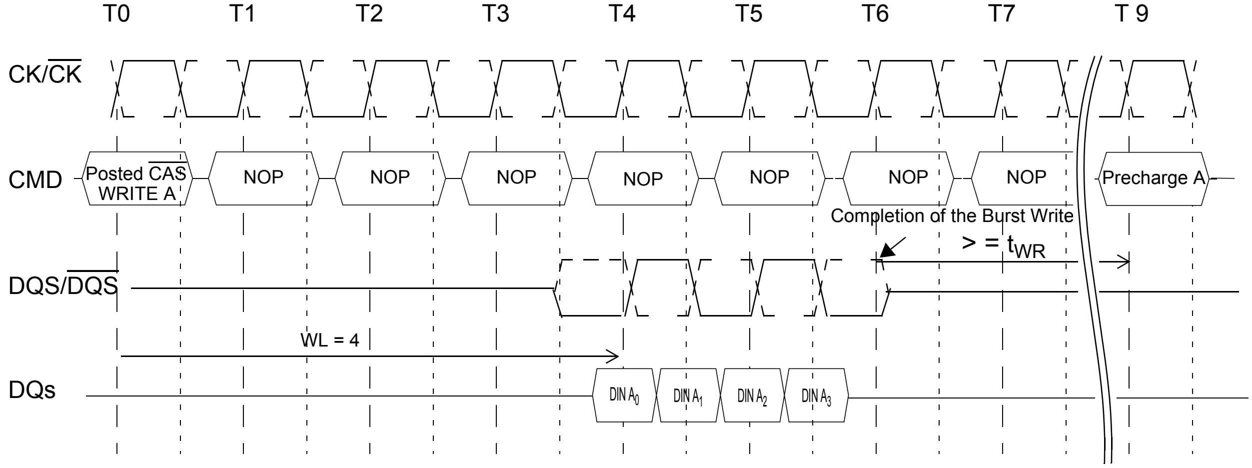


Figure 50 — Example 2: Burst write followed by precharge: WL = (RL-1) = 4

2.8 Auto precharge operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge command or the auto-precharge function. When a Read or a Write command is given to the DDR2 SDRAM, the $\overline{\text{CAS}}$ timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is LOW when the READ or WRITE command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is HIGH when the Read or Write command is issued, then the auto-precharge function is engaged. During auto-precharge, a Read command will execute as normal with the exception that the active bank will begin to precharge on the rising edge which is $\overline{\text{CAS}}$ latency (CL) clock cycles before the end of the read burst.

Auto-precharge is also implemented during Write commands. The precharge operation engaged by the Auto precharge command will not begin until the last data of the burst write sequence is properly stored in the memory array.

This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon $\overline{\text{CAS}}$ latency) thus improving system performance for random data access. The $\overline{\text{RAS}}$ lockout circuit internally delays the Precharge operation until the array restore operation has been completed (tRAS satisfied) so that the auto precharge command may be issued with any read or write command.

2.8 Auto precharge operation (cont’d)

2.8.1 Burst read with auto precharge

If A10 is HIGH when a Read Command is issued, the Read with Auto-Precharge function is engaged. The DDR2 SDRAM starts an Auto Precharge operation on the rising edge which is (AL + BL/2) cycles later than the read with AP command if tRAS(min) and tRTP(min) are satisfied.

If tRAS(min) is not satisfied at the edge, the start point of auto-precharge operation will be delayed until tRAS(min) is satisfied.

If tRTP(min) is not satisfied at the edge, the start point of auto-precharge operation will be delayed until tRTP(min) is satisfied.

In case the internal precharge is pushed out by tRTP, tRP starts at the point where tRTP ends (not at the next rising clock edge after this event). So for BL = 4 the minimum time from Read_AP to the next Activate command becomes AL + RU{ (tRTP + tRP) / tCK } (see Figure 52), for BL = 8 the time from Read_AP to the next Activate is AL + 2 + RU{ (tRTP + tRP) / tCK }, where RU stands for “rounded up to the next integer”. These equations change to AL + RU{ (tRTP + tRP) / tCK(avg) } and AL + 2 + RU{ (tRTP + tRP) / tCK(avg) }, respectively, for DDR2-667/800. In any event internal precharge does not start earlier than two clocks after the last 4-bit prefetch.

A new bank activate (command) may be issued to the same bank if the following two conditions are satisfied simultaneously.

a) The $\overline{\text{RAS}}$ precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.

b) The $\overline{\text{RAS}}$ cycle time (tRC) from the previous bank activation has been satisfied.

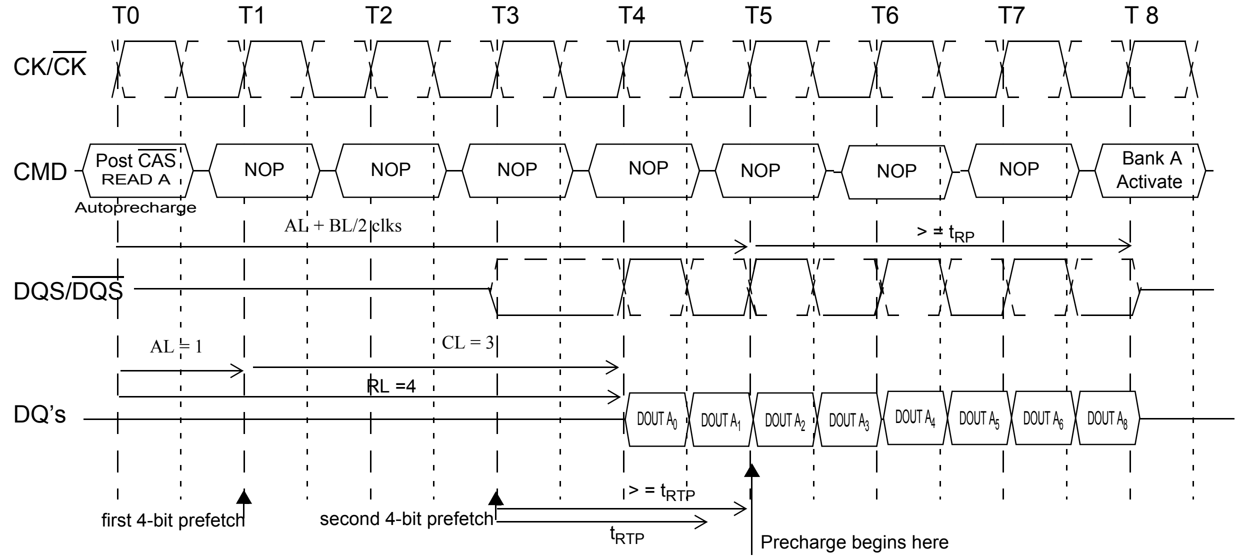


Figure 51 — Example 1: Burst read operation with auto precharge: RL = 4, AL = 1, CL = 3, BL = 8, t_{RTP} <= 2 clocks

2.8 Auto precharge operation (cont'd)

2.8.1 Burst read with auto precharge (cont'd)

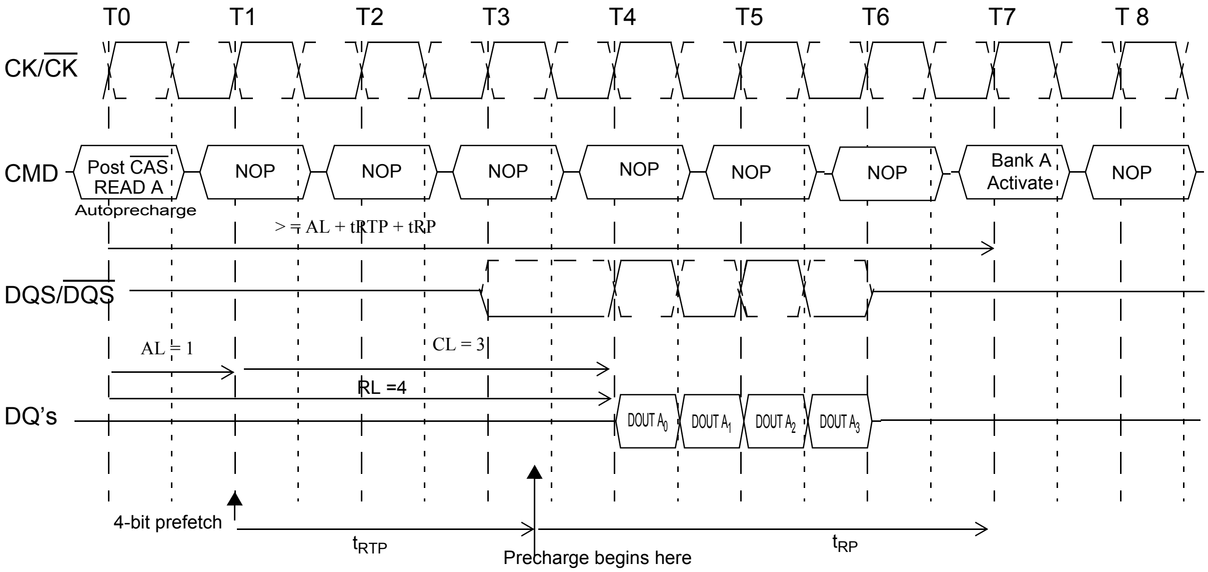


Figure 52 — Example 2: Burst read operation with auto precharge: RL = 4, AL = 1, CL = 3, BL = 4, t_{RTP} > 2 clocks

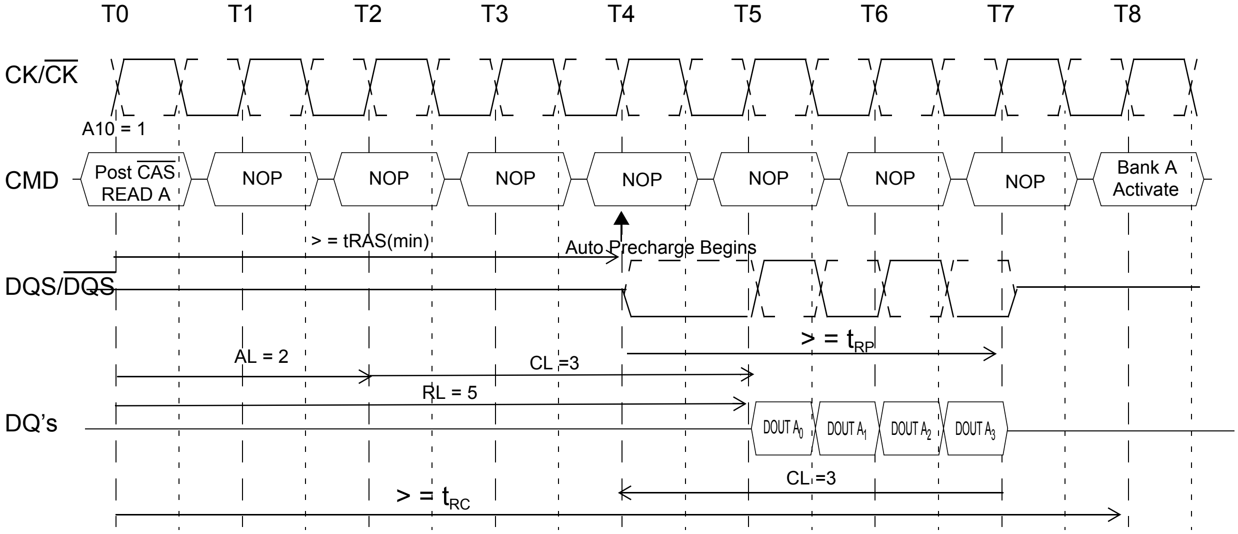


Figure 53 — Example 3: Burst read with auto precharge followed by an activation to the same bank (tRC Limit): RL = 5 (AL = 2, CL = 3, internal tRCD = 3, BL = 4, t_{RTP} <= 2 clocks)

2.8 Auto precharge operation (cont'd)

2.8.1 Burst read with auto precharge (cont'd)

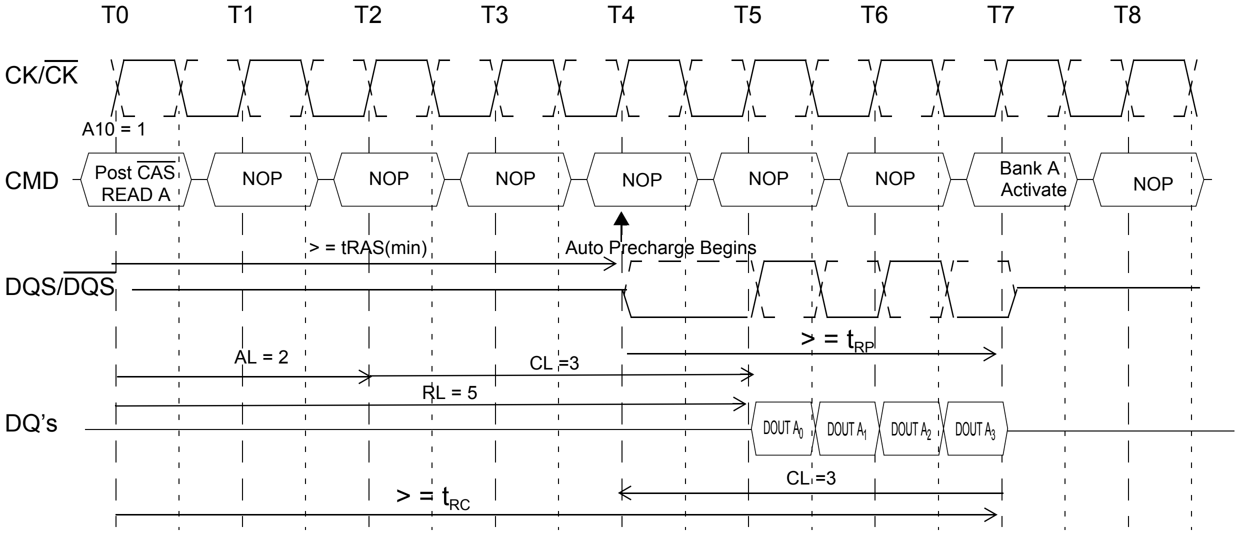


Figure 54 — Example 4: Burst read with auto precharge followed by an activation to the same bank (tRP Limit): RL = 5 (AL = 2, CL = 3, internal tRCD = 3, BL = 4, t_{RTP} <= 2 clocks)

2.8.2 Burst write with auto precharge

If A10 is HIGH when a Write Command is issued, the Write with Auto-Precharge function is engaged. The DDR2 SDRAM automatically begins precharge operation after the completion of the burst write plus write recovery time (WR) programmed in the mode register. The bank undergoing auto-precharge from the completion of the write burst may be reactivated if the following two conditions are satisfied.

a) The data-in to bank activate delay time (WR + tRP) has been satisfied.

b) The $\overline{RAS}$ cycle time (tRC) from the previous bank activation has been satisfied.

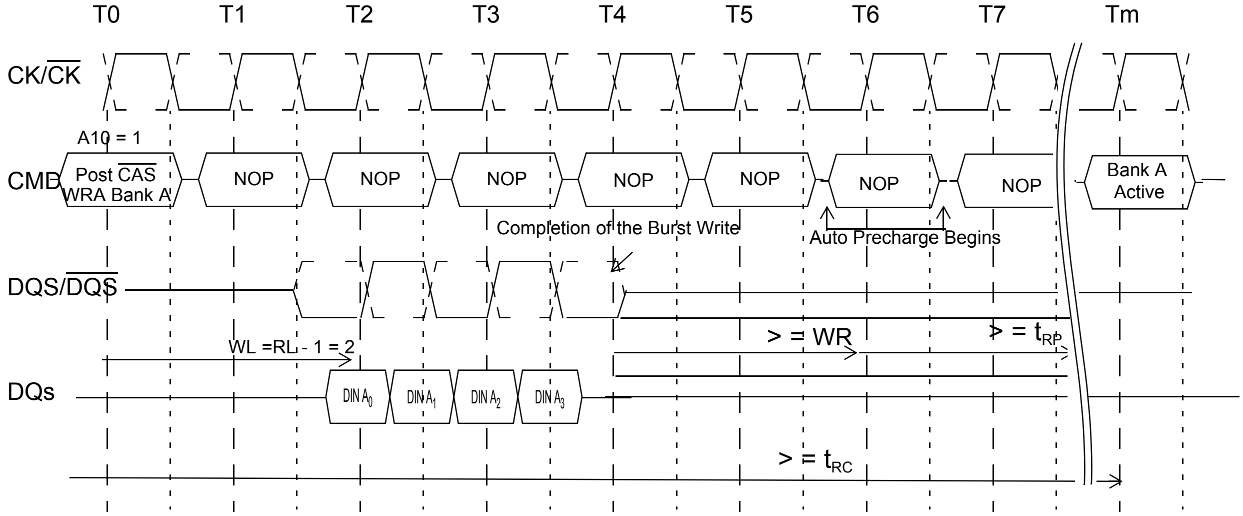


Figure 55 — Burst write with auto-precharge (tRC Limit): WL = 2, WR = 2, BL = 4, tRP = 3

2.8 Auto precharge operation (cont’d)

2.8.2 Burst write with auto precharge (cont’d)

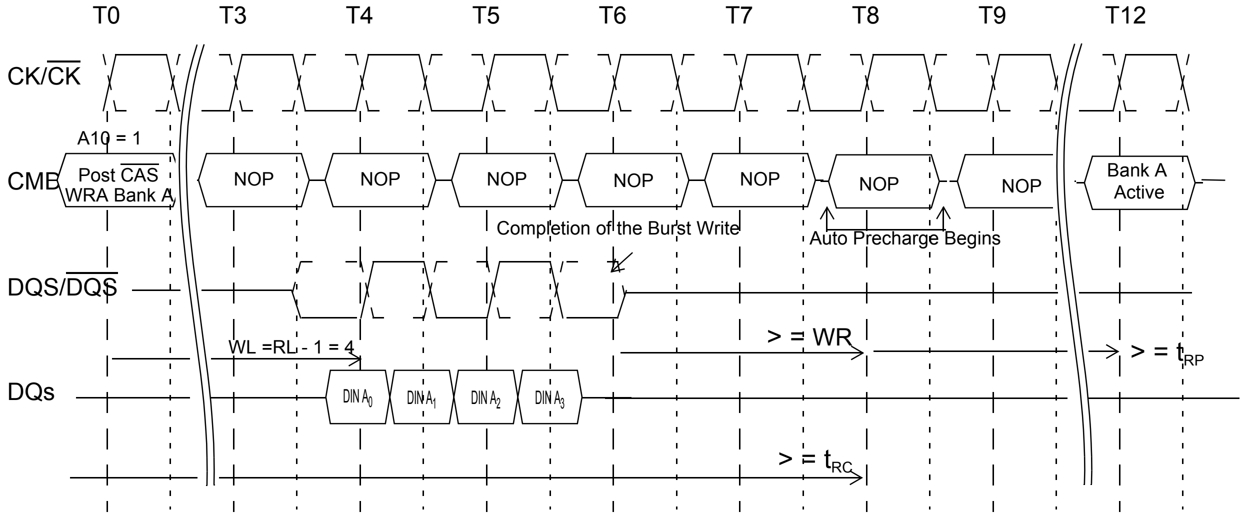


Figure 56 — Burst write with auto-precharge (WR + tRP): WL = 4, WR = 2, BL = 4, tRP = 3

Table 11 — Precharge & auto precharge clarification

From Command	To Command	Minimum Delay between “From Command” to “To Command”	Unit	Notes
Read	Precharge (to same Bank as Read)	AL + BL/2 + max(RTP, 2) - 2	clks	1, 2
	Precharge All	AL + BL/2 + max(RTP, 2) - 2	clks	1, 2
Read w/AP	Precharge (to same Bank as Read w/AP)	AL + BL/2 + max(RTP, 2) - 2	clks	1, 2
	Precharge All	AL + BL/2 + max(RTP, 2) - 2	clks	1, 2
Write	Precharge (to same Bank as Write)	WL + BL/2 + tWR	clks	2
	Precharge All	WL + BL/2 + tWR	clks	2
Write w/AP	Precharge (to same Bank as Write w/AP)	WL + BL/2 + WR	clks	2
	Precharge All	WL + BL/2 + WR	clks	2
Precharge	Precharge (to same Bank as Precharge)	1	clks	2
	Precharge All	1	clks	2
Precharge All	Precharge	1	clks	2
	Precharge All	1	clks	2

NOTE 1 RTP[cycles] = RU{ tRTP[ns] / tCK[ns] }, where RU stands for round up. tCK(avg) should be used in place of tCK for DDR2-667/800.

NOTE 2 For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after tRP or tRPall (= tRP for 4 bank device, = tRP + 1 x tCK for 8 bank device) depending on the latest precharge command issued to that bank.

2.9 Refresh command

When $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ are held LOW and $\overline{WE}$ HIGH at the rising edge of the clock, the chip enters the Refresh mode (REF). All banks of the DDR2 SDRAM must be precharged and idle for a minimum of the Precharge time (tRP) before the Refresh command (REF) can be applied. An address counter, internal to the device, supplies the bank address during the refresh cycle. No control of the external address bus is required once this cycle has started.

When the refresh cycle has completed, all banks of the DDR2 SDRAM will be in the precharged (idle) state. A delay between the Refresh command (REF) and the next Activate command or subsequent Refresh command must be greater than or equal to the Refresh cycle time (tRFC).

2 Functional description (cont'd)

2.9 Refresh command (cont'd)

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight Refresh commands can be posted to any given DDR2 SDRAM, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 9 x tREFI.

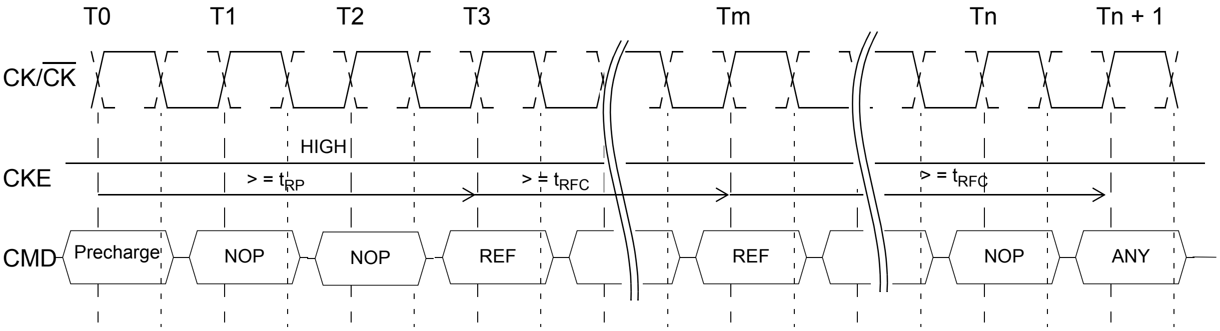


Figure 57 — Refresh command

2.10 Self refresh operation

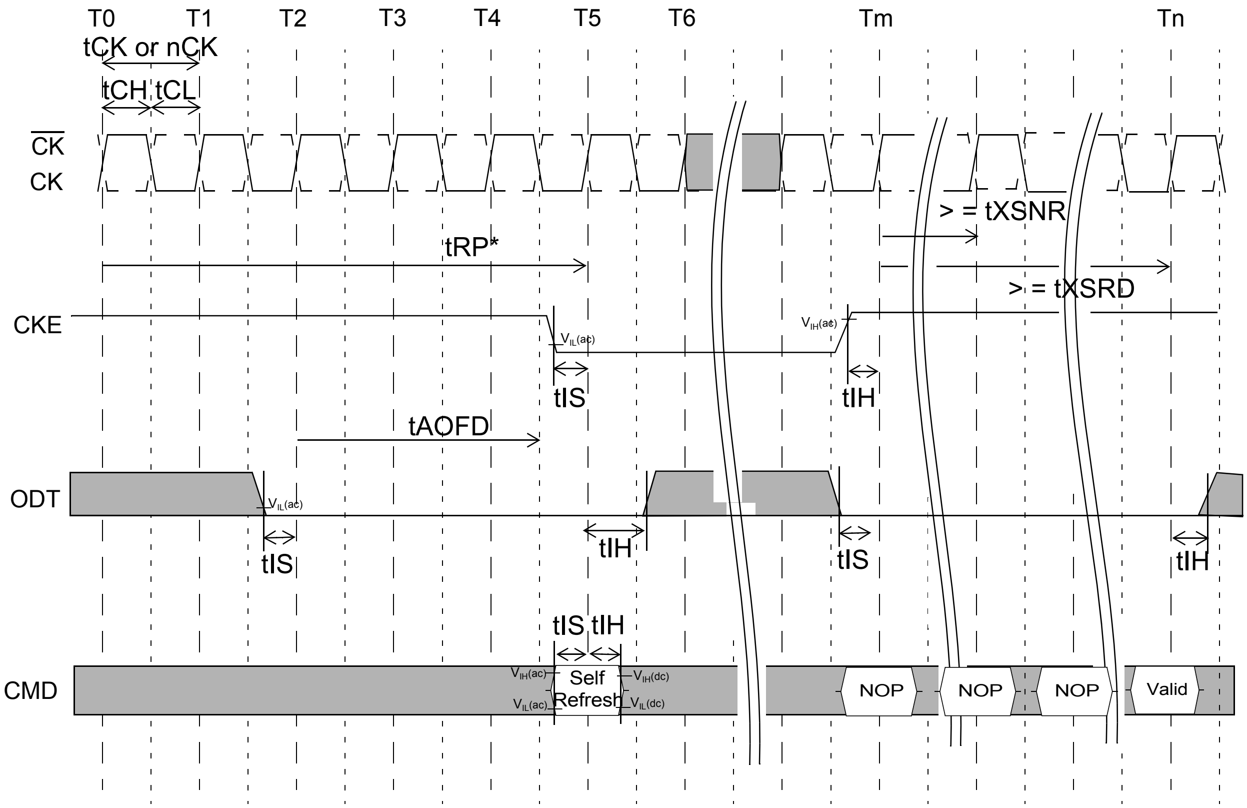
The Self Refresh command can be used to retain data in the DDR2 SDRAM, even if the rest of the system is powered down. When in the Self Refresh mode, the DDR2 SDRAM retains data without external clocking. The DDR2 SDRAM device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held LOW with $\overline{WE}$ HIGH at the rising edge of the clock. ODT must be turned off before issuing Self Refresh command, by either driving ODT pin LOW or using an EMRS command. Once the command is registered, CKE must be held LOW to keep the device in Self Refresh mode. The DLL is automatically disabled upon entering Self Refresh and is automatically enabled upon exiting Self Refresh. When the DDR2 SDRAM has entered Self Refresh mode, all of the external signals except CKE, are “don’t care”. For proper self refresh operation, all power supply pins (VDD, VDDQ, VDDL and Vref) must be at valid levels. The DRAM initiates a minimum of one refresh command internally within tCKE period once it enters Self Refresh mode. The clock is internally disabled during Self Refresh Operation to save power. The minimum time that the DDR2 SDRAM must remain in Self Refresh mode is tCKE. The user may change the external clock frequency or halt the external clock one clock after Self Refresh entry is registered; however, the clock must be restarted and stable before the device can exit Self Refresh operation.

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock must be stable prior to CKE going back HIGH. Once Self Refresh Exit is registered, a delay of at least tXSNR must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain HIGH for the entire Self Refresh exit period tXSRD for proper operation except for self refresh re-entry. Upon exit from Self Refresh, the DDR2 SDRAM can be put back into Self Refresh mode after waiting at least tXSNR period and issuing one refresh command (refresh period of tRFC). NOP or deselect commands must be registered on each positive clock edge during the Self Refresh exit interval tXSNR. ODT should be turned off during tXSRD.

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, the DDR2 SDRAM requires a minimum of one extra auto refresh command before it is put back into Self Refresh mode.

2 Functional description (cont'd)

2.10 Self refresh operation (cont'd)



NOTE 1 Device must be in the "All banks idle" state prior to entering Self Refresh mode.

NOTE 2 ODT must be turned off tAOFD before entering Self Refresh mode, and can be turned on again when tXSRD timing is satisfied.

NOTE 3 tXSRD is applied for a Read or a Read with autoprecharge command.

tXSNR is applied for any command except a Read or a Read with autoprecharge command.

Figure 58 — Self refresh operation

2.11 Power-down

Power-down is synchronously entered when CKE is registered LOW (along with Nop or Deselect command). CKE is not allowed to go LOW while mode register or extended mode register command time, or read or write operation is in progress. CKE is allowed to go LOW while any of other operations such as row activation, precharge or autoprecharge, or auto-refresh is in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in the following pages with details for entry into power down.

The DLL should be in a locked state when power-down is entered. Otherwise DLL should be reset after exiting power-down mode for proper read operation. DRAM design guarantees all AC and DC timing & voltage specifications as well as proper DLL operation with any CKE intensive operations as long as DRAM controller complies with DRAM specifications. Figures 60 and 61 show two examples of CKE intensive applications.

If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$, ODT and CKE. Also the DLL is disabled upon entering precharge power-down or slow exit active power-down, but the DLL is kept enabled during fast exit active power-down. In power-down mode, CKE LOW and a stable clock signal must be maintained at the inputs of the DDR2 SDRAM, and ODT should be in a valid state but all other input signals are "Don't Care". CKE LOW must be maintained until tCKE has been satisfied. Maximum power-down duration is limited by the refresh requirements of the device, which allows a maximum of 9 x tREFI if maximum posting of REF is utilized immediately before entering power down.

2 Functional description (cont'd)

2.11 Power-down (cont'd)

The power-down state is synchronously exited when CKE is registered HIGH (along with a Nop or Deselect command). CKE HIGH must be maintained until tCKE has been satisfied. A valid, executable command can be applied with power-down exit latency, tXP, tXARD, or tXARDS, after CKE goes HIGH. Power-down exit latency is defined in the timing parameter table of this standard.

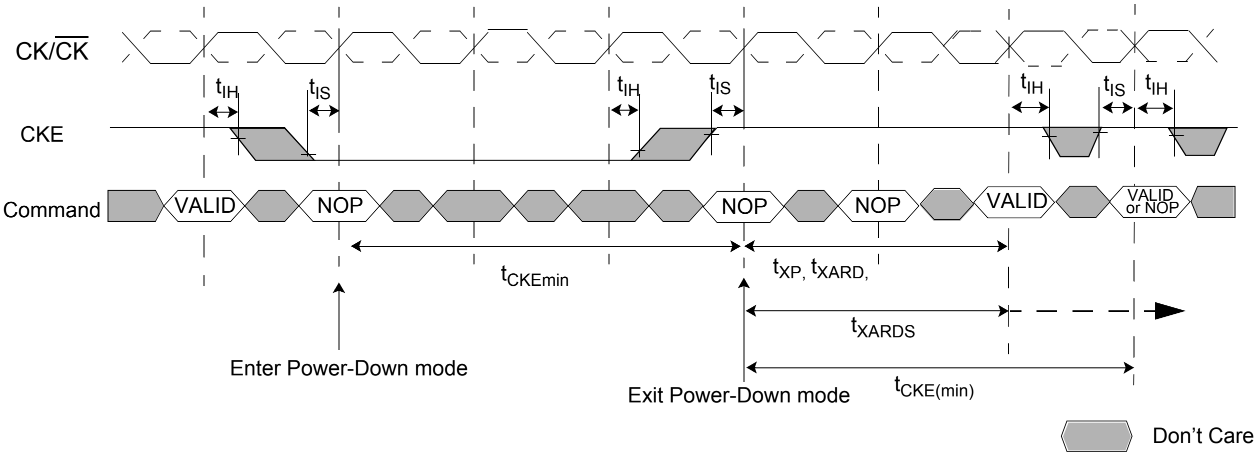
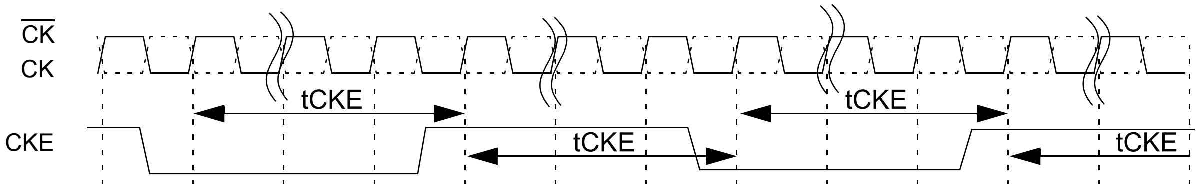
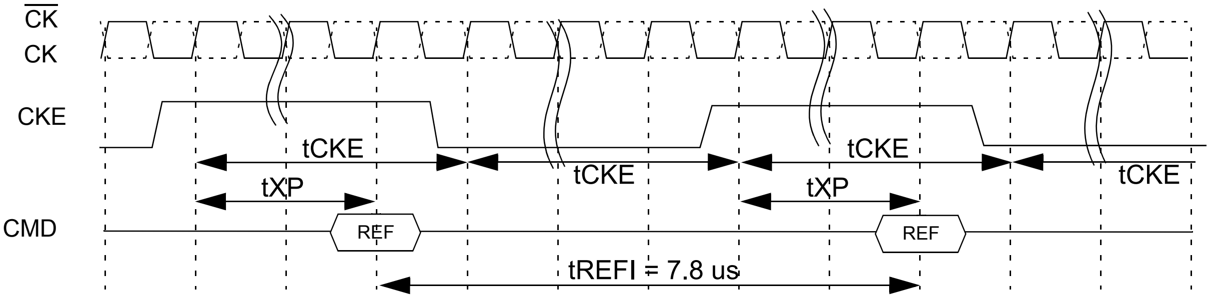


Figure 59 — Basic power down entry and exit timing diagram



NOTE DRAM guarantees all AC and DC timing & voltage specifications and proper DLL operation with intensive CKE operation

Figure 60 — Example 1 of CKE intensive environment



NOTE The pattern shown above can repeat over a long period of time. With this pattern, DRAM guarantees all AC and DC timing & voltage specifications and DLL operation with temperature and voltage drift

Figure 61 — Example 2 of CKE intensive environment

2 Functional description (cont’d)

2.11 Power-down (cont’d)

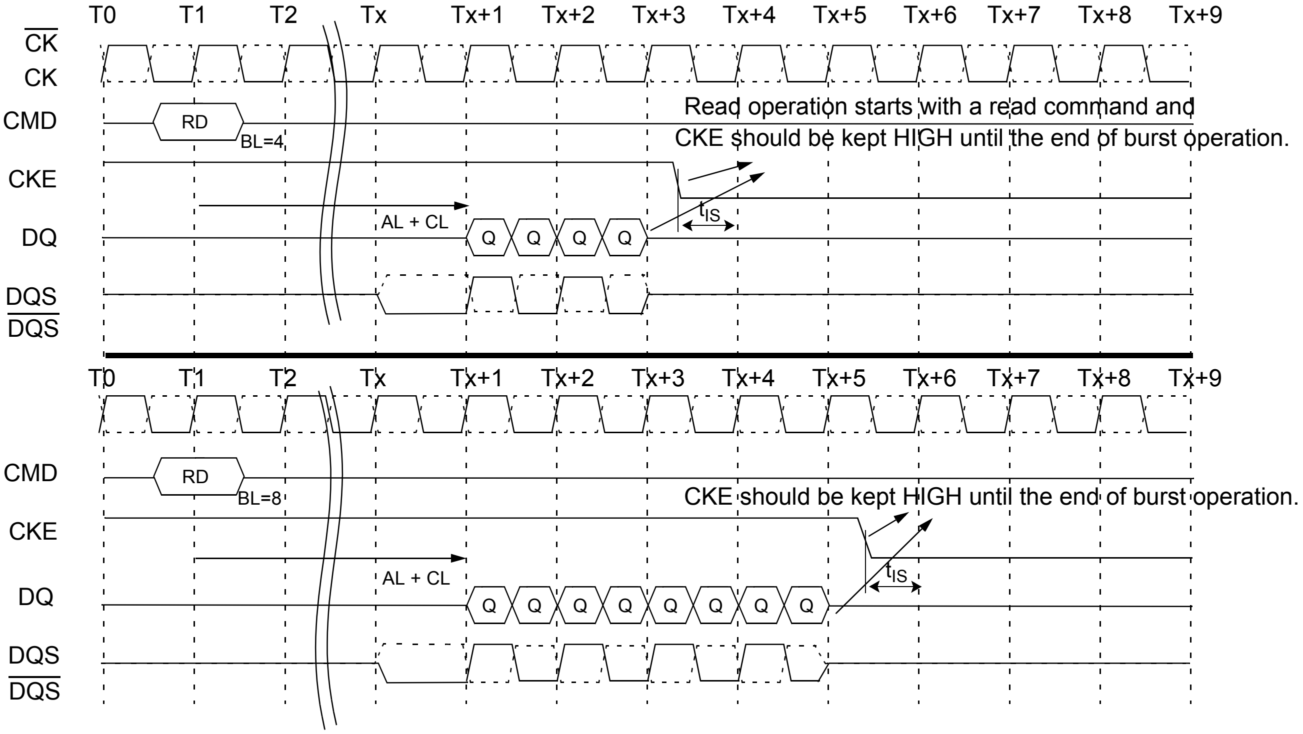


Figure 62 — Read to power-down entry

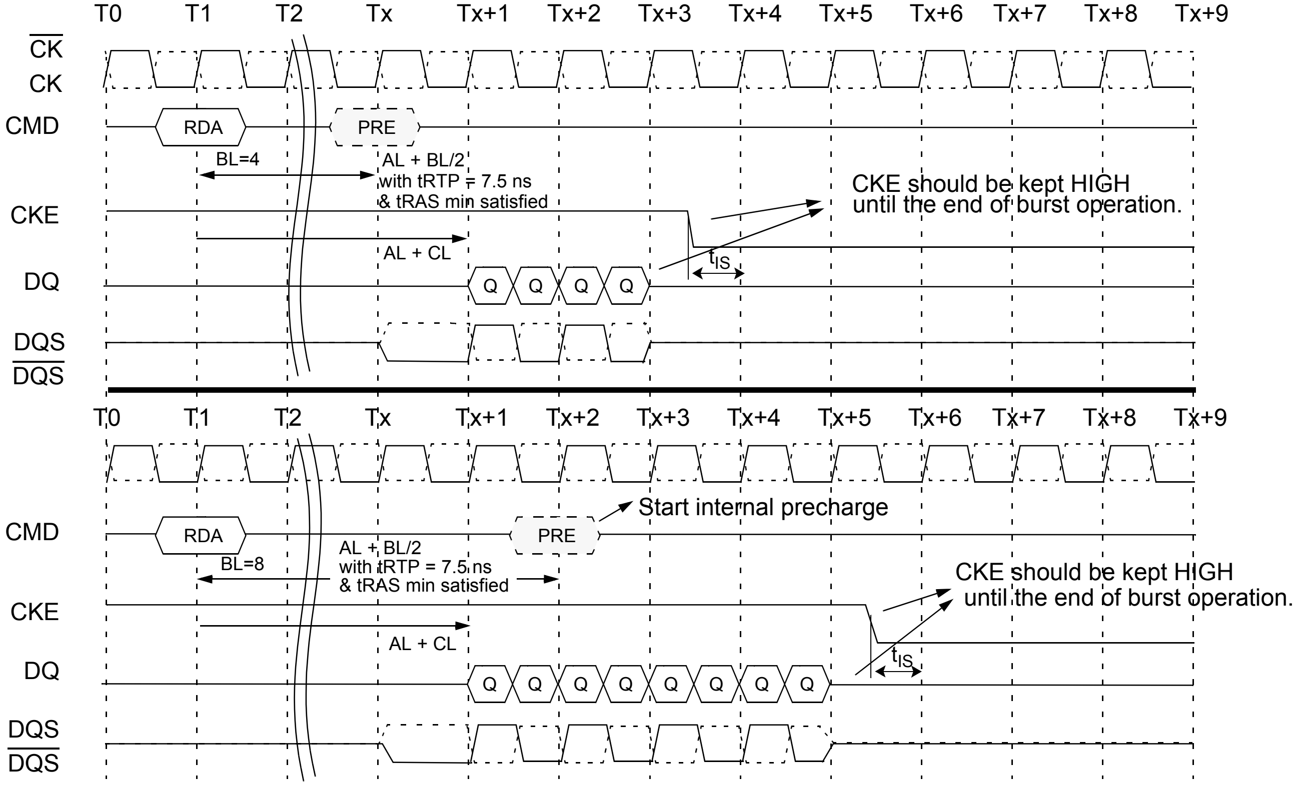


Figure 63 — Read with autoprecharge to power-down entry

2 Functional description (cont'd)

2.11 Power-down (cont'd)

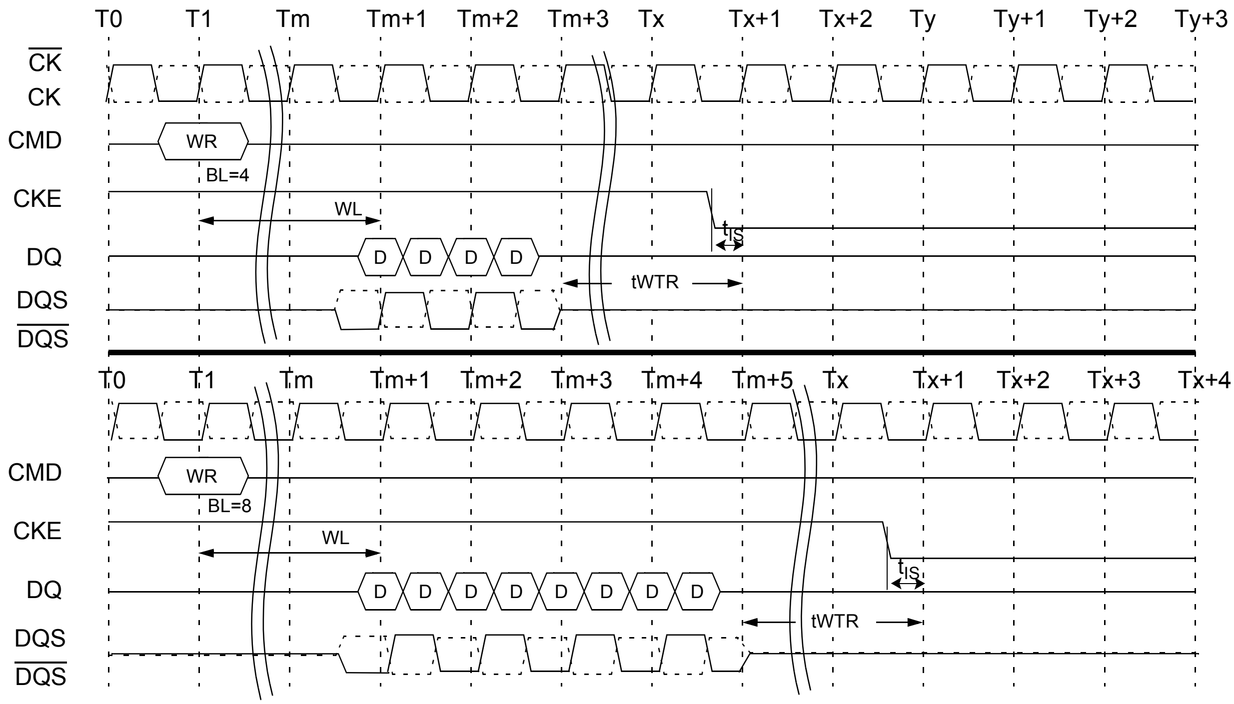
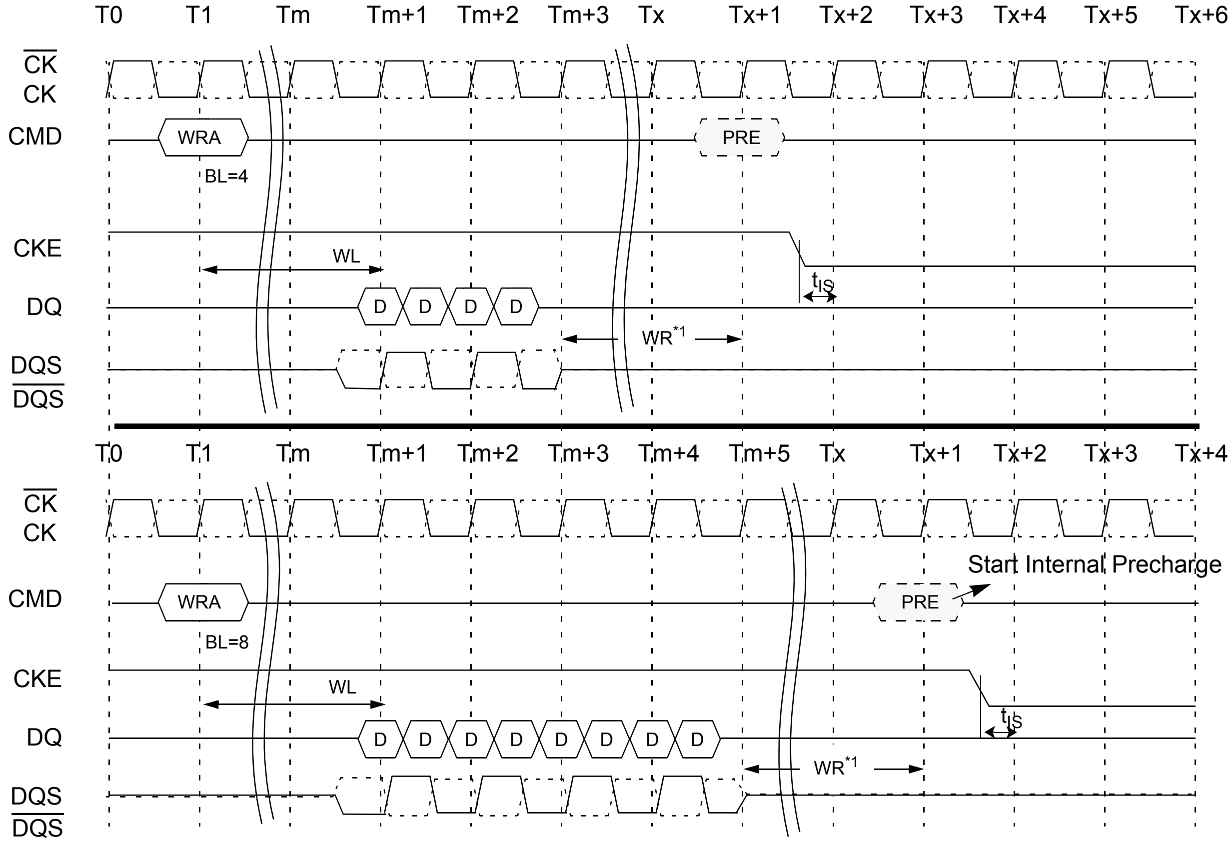


Figure 64 — Write to power-down entry



*1: WR is programmed through MRS

Figure 65 — Write with autoprecharge to power-down entry

2 Functional description (cont'd)

2.11 Power-down (cont'd)

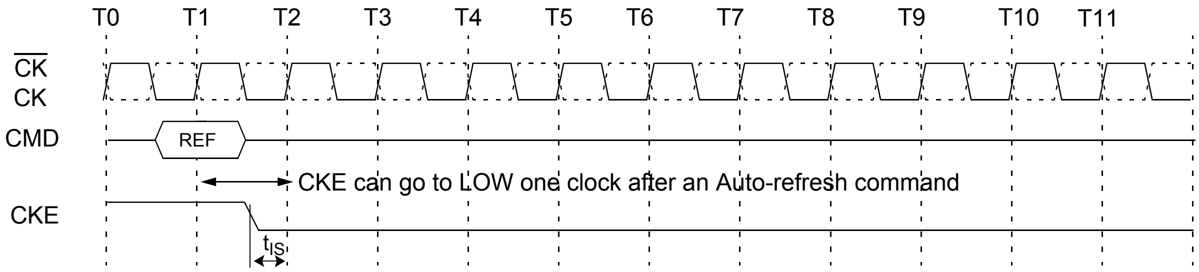


Figure 66 — Refresh command to power-down entry

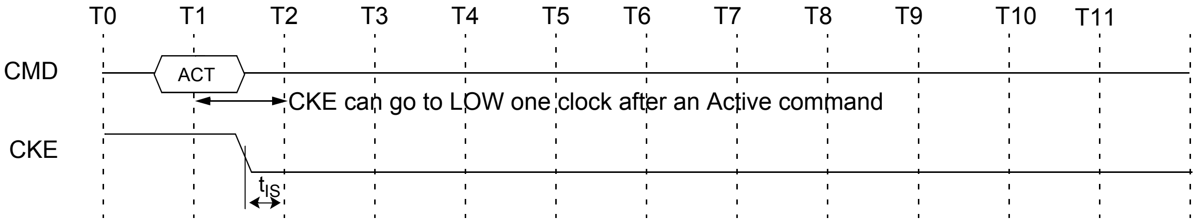


Figure 67 — Active command to power-down entry

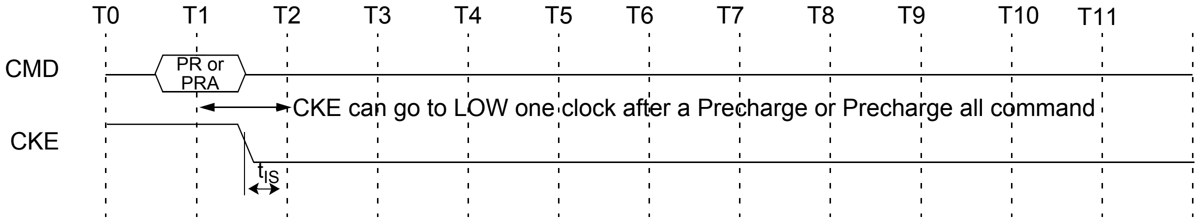


Figure 68 — Precharge/precharge-all command to power-down entry

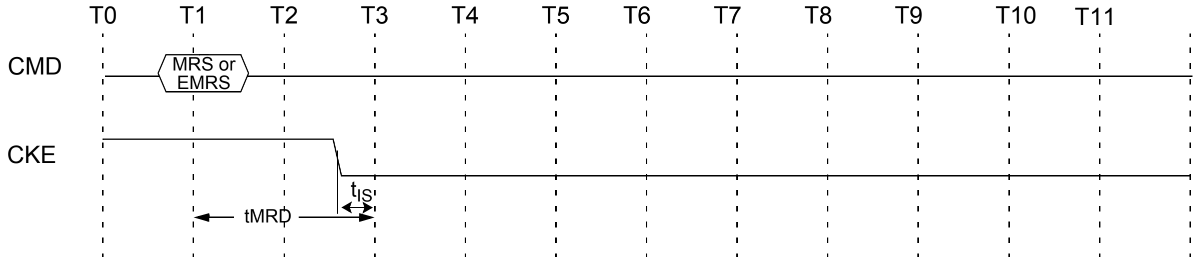


Figure 69 — MRS/EMRS command to power-down entry

2.12 Asynchronous CKE LOW event

DRAM requires CKE to be maintained "HIGH" for all valid operations as defined in this data sheet. If CKE asynchronously drops "LOW" during any valid operation DRAM is not guaranteed to preserve the contents of array. If this event occurs, memory controller must satisfy DRAM timing specification tDelay before turning off the clocks. Stable clocks must exist at the input of DRAM before CKE is raised "HIGH" again. DRAM must be fully re-initialized (steps d thru m) as described in the Power-up and initialization sequence. DRAM is ready for normal operation after the initialization sequence. See AC timing parametric tables 41 and 42 for tDelay specification.

2 Functional description (cont'd)

2.12 Asynchronous CKE LOW event (cont'd)

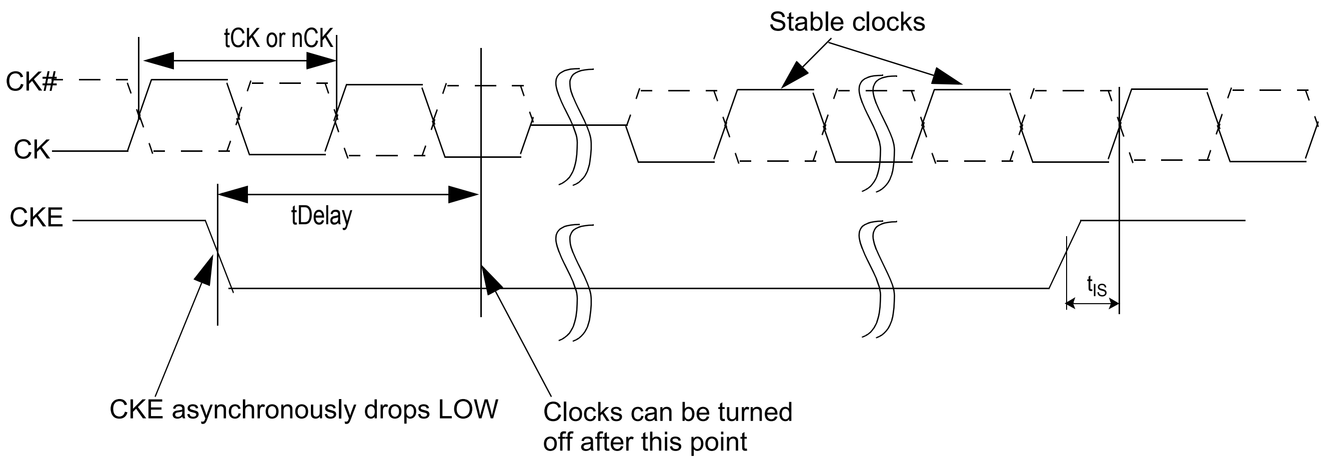


Figure 70 — Asynchronous CKE LOW event

2.13 Input clock frequency change during precharge power down

DDR2 SDRAM input clock frequency can be changed under following condition:

DDR2 SDRAM is in precharged power down mode. ODT must be turned off and CKE must be at logic LOW level. A minimum of 2 clocks must be waited after CKE goes LOW before clock frequency may change. SDRAM input clock frequency is allowed to change only within minimum and maximum operating frequency specified for the particular speed grade. During input clock frequency change, ODT and CKE must be held at stable LOW levels. Once input clock frequency is changed, stable new clocks must be provided to DRAM before precharge power down may be exited and DLL must be RESET via MRS command after precharge power down exit. Depending on new clock frequency an additional MRS or EMRS command may need to be issued to appropriately set the WR, CL etc.. During DLL re-lock period, ODT must remain off. After the DLL lock time, the DRAM is ready to operate with new clock frequency.

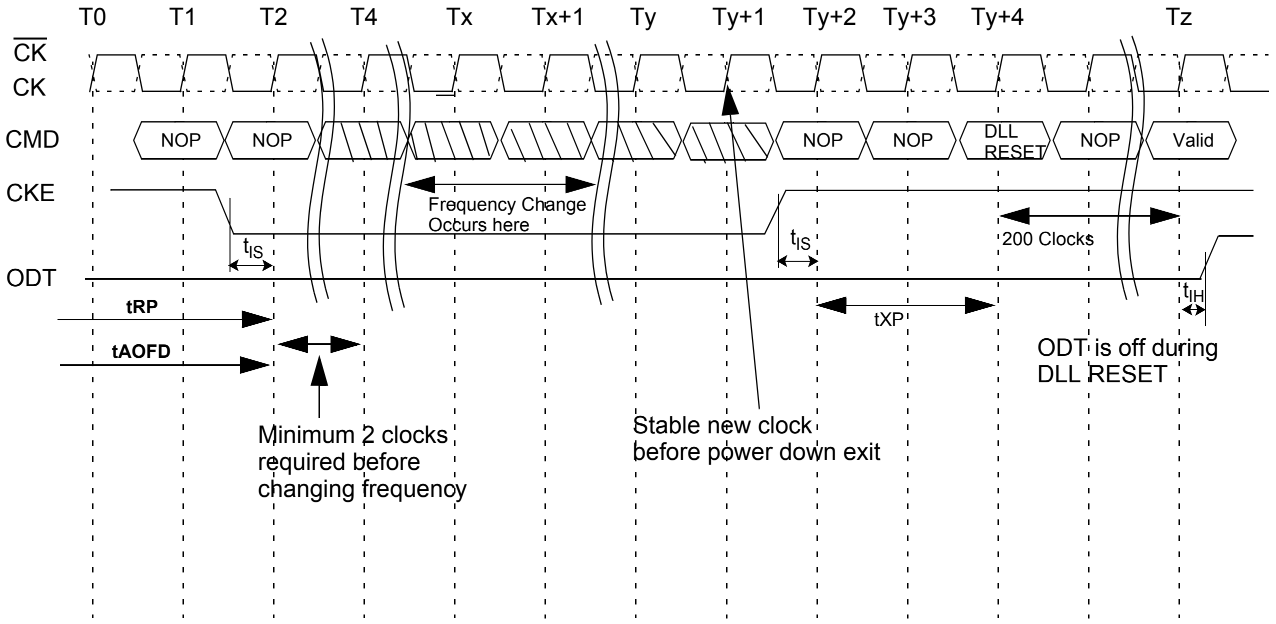


Figure 71 — Clock frequency change in precharge power-down mode

2 Functional description (cont'd)

2.14 SSC (Spread Spectrum Clocking)

2.14.1 Terms and definitions

$f_{CK,min}$: Minimum frequency supported by the DRAM (for all DDR2 speed bins, $1/t_{CK(avg),max} = 125$ MHz)

$f_{CK,max}$: Maximum frequency supported by the DRAM (for DDR2-667, $1/t_{CK(avg),min} = 333$ MHz)

SSC band: If the system modulates the input clock frequency between $f_{SSC,min}$ and $f_{SSC,max}$, this frequency band is referred to as SSC band

$f_{SSC,nom}$: Mean frequency of $f_{SSC,min}$ and $f_{SSC,max}$

Modulation frequency: Rate at which the frequency is modulated for SSC

ex) 20 kHz modulation: Input clock frequency shifts gradually from $f_{SSC,min}$ to $f_{SSC,max}$ over 25 us (=50 us/2)

2.14.2 SSC (Spread Spectrum Clocking) Criteria

SSC is allowed only if $f_{SSC,min}$ is greater than or equal to $f_{CK,min}$ and $f_{SSC,max}$ is less than or equal to $f_{CK,max}$. All input clock specs including, but not limited to, terr(nper) must be met at all times. Allowed modulation frequency is 20 kHz to 60 kHz.

2.14.3 Allowed SSC band

If the DRAM DLL is locked at $f_{SSC,nom}$ (by issuing a DLL reset and waiting 200 clock cycles) and then the SSC is turned on later, the system is allowed an SSC band of $f_{SSC,nom}$ +/-1 %.

In all other cases, the system is allowed an SSC band of $f_{SSC,nom}$ +/-0.5 %.

If the input clock frequency drifts out of this band, the output timings can no longer be guaranteed and DLL reset must be issued to regain the output timings assuming a different SSC band.

2.15 No operation command

The No Operation command should be used in cases when the DDR2 SDRAM is in an idle or a wait state. The purpose of the No Operation command (NOP) is to prevent the DDR2 SDRAM from registering any unwanted commands between operations. A No Operation command is registered when $\overline{CS}$ is LOW with $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ held HIGH at the rising edge of the clock. A No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

2.16 Deselect command

The Deselect command performs the same function as a No Operation command. Deselect command occurs when $\overline{CS}$ is brought HIGH at the rising edge of the clock, the $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ signals become don't cares.

---

3 Truth tables

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the speechified initialization sequence before normal operation can continue.

3.1 Command truth table

Table 12 provides the command truth table.

Table 12 — Command truth table

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 - BAx[9]	Axx[9]-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			1,2
Refresh (REF)	H	H	L	L	L	H	X	X	X	X	1
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	1,8

3 Truth tables (cont’d)

3.1 Command truth table (cont’d)

Table 12 — Command truth table (cont’d)

Function	CKE		$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	BA0 - BAx^9	Axx^9-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	1,7,8
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1,2
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3,
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3,
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1,2,3
No Operation	H	X	L	H	H	H	X	X	X	X	1
Device Deselect	H	X	H	X	X	X	X	X	X	X	1
Power Down Entry	H	L	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					

NOTE 1 All DDR2 SDRAM commands are defined by states of $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and CKE at the rising edge of the clock.
NOTE 2 Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.
NOTE 3 Burst reads or writes at BL=4 cannot be terminated or interrupted. See sections "Reads interrupted by a Read" and "Writes interrupted by a Write" in section 2.6 for details.
NOTE 4 The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements outlined in section 2.9.
NOTE 5 The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh. See section 2.4.4.
NOTE 6 “X” means “H or L (but a defined logic level)”
NOTE 7 Self refresh exit is asynchronous.
NOTE 8 VREF must be maintained during Self Refresh operation.
NOTE 9 BAx and Axx refers to the MSBs of bank addresses and addresses, respectively, per device density.

3.2 Clock enable truth table.

Table 13 provides the clock enable truth table.

Table 13 — Clock enable (CKE) truth table for synchronous transitions

Current State ^{2}	CKE		Command (N) ^{3} $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{CS}}$	Action (N) ^{3}	Notes
	Previous Cycle ^{1} (N-1)	Current Cycle ^{1} (N)			
Power Down	L	L	X	Maintain Power-Down	11, 13, 15
	L	H	DESELECT or NOP	Power Down Exit	4, 8, 11,13

3 Truth tables (cont'd)

3.2 Clock enable truth table (cont'd)

Table 13 — Clock enable (CKE) truth table for synchronous transitions

Current State [2]	CKE		Command (N) [3]	Action (N) [3]	Notes
	Previous Cycle [1] (N-1)	Current Cycle [1] (N)	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$		
Self Refresh	L	L	X	Maintain Self Refresh	11, 15,16
	L	H	DESELECT or NOP	Self Refresh Exit	4, 5, 9, 16
Bank(s) Active	H	L	DESELECT or NOP	Active Power Down Entry	4, 8, 10, 11, 13
All Banks Idle	H	L	DESELECT or NOP	Precharge Power Down Entry	4, 8, 10, 11,13
	H	L	REFRESH	Self Refresh Entry	6, 9, 11,13
	H	H	Refer to the Command Truth Table		7

NOTE 1 CKE (N) is the logic state of CKE at clock edge N; CKE (N–1) was the state of CKE at the previous clock edge.
NOTE 2 Current state is the state of the DDR2 SDRAM immediately prior to clock edge N.
NOTE 3 COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N).
NOTE 4 All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
NOTE 5 On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the t_{XSNR} period. Read commands may be issued only after t_{XSRD} (200 clocks) is satisfied.
NOTE 6 Self Refresh mode can only be entered from the All Banks Idle state.
NOTE 7 Must be a legal command as defined in the Command Truth Table.
NOTE 8 Valid commands for Power Down Entry and Exit are NOP and DESELECT only.
NOTE 9 Valid commands for Self Refresh Exit are NOP and DESELECT only.
NOTE 10 Power Down and Self Refresh can not be entered while Read or Write operations, (Extended) Mode Register Set operations or Precharge operations are in progress. See section 2.11 Power-down and 2.10 Self refresh operation for a detailed list of restrictions.
NOTE 11 tCKEmin of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + 2 x tCK + tIH.
NOTE 12 The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh. See section 2.4.4.
NOTE 13 The Power Down does not perform any refresh operations. The duration of Power Down Mode is therefore limited by the refresh requirements outlined in section 2.9.
NOTE 14 CKE must be maintained HIGH while the SDRAM is in OCD calibration mode .
NOTE 15 "X" means "don't care (including floating around VREF)" in Self Refresh and Power Down. However ODT must be driven HIGH or LOW in Power Down if the ODT function is enabled (Bit A2 or A6 set to "1" in EMR(1)).
NOTE 16 VREF must be maintained during Self Refresh operation.

3.3 Data mask truth table.

Table 14 provides the data mask truth table.

Table 14 — DM truth table

Name (Functional)	DM	DQs	Note
Write enable	L	Valid	1
Write inhibit	H	X	1

NOTE 1 Used to mask write data, provided coincident with the corresponding data

4 Absolute maximum DC ratings

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the speechified initialization sequence before normal operation can continue.

Table 15 provides the absolute maximum DC ratings.

Table 15 — Absolute maximum DC ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	- 1.0 V ~ 2.3 V	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.5 V ~ 2.3 V	V	1,3
VDDL	Voltage on VDDL pin relative to Vss	- 0.5 V ~ 2.3 V	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	- 0.5 V ~ 2.3 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1, 2

NOTE 1 Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

NOTE 2 Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

NOTE 3 When VDD and VDDQ and VDDL are less than 500 mV, Vref may be equal to or less than 300 mV.

5 AC & DC operating conditions

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the speechified initialization sequence before normal operation can continue.

Table 16 — Recommended DC operating conditions (SSTL_1.8)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.7	1.8	1.9	V	1
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V	5
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V	1, 5
VREF	Input Reference Voltage	0.49 x VDDQ	0.50 x VDDQ	0.51 x VDDQ	mV	2. 3
VTT	Termination Voltage	VREF - 0.04	VREF	VREF + 0.04	V	4

NOTE 1 There is no specific device VDD supply voltage requirement for SSTL_18 compliance. However under all conditions VDDQ must be less than or equal to VDD.

NOTE 2 The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.

NOTE 3 Peak to peak ac noise on VREF may not exceed +/-2 % VREF(dc).

NOTE 4 VTT of transmitting device must track VREF of receiving device.

NOTE 5 VDDQ tracks with VDD, VDDL tracks with VDD. AC parameters are measured with VDD, VDDQ and VDDDL tied together

5 AC & DC operating conditions (cont'd)

Table 17 — Operating temperature condition

SYMBOL	PARAMETER	RATING	UNITS	NOTES
TOPER	Operating Temperature	0 to 85	°C	1, 2

NOTE 1 Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51.2 standard.

NOTE 2 The operation temperature range are the temperature where all DRAM specification will be supported. Outside of this temperature range, even if it is still within the limit of stress condition, some deviation on portion of operation specification may be required. During operation, the DRAM case temperature must be maintained between 0 - 85 °C under all other specification parameter. However, in some applications, it is desirable to operate the DRAM up to 95 °C case temperature. Therefore, two spec options may exist.

a) Supporting 0 - 85 °C with full JEDEC AC & DC specifications. This is the minimum requirements for all operating temperature options.

b) This is an optional feature and not required. Supporting 0 - 85 °C and being able to extend to 95 °C with doubling auto-refresh commands in frequency to a 32 ms period (tREFI = 3.9 us).

Currently the periodic Self-Refresh interval is hard coded within the DRAM to a vendor specific value. There is a migration plan to support higher temperature Self-Refresh entry via the control of EMSR(2) bit A7. However, since Self-Refresh control function is a migrated process to be phased-in by individual manufacturer, checking on the DRAM parts for this function availability is necessary. For JEDEC standard DIMM module user, it is imperative to check SPD Byte 49 Bit 0 to ensure the DRAM parts support higher than 85 °C case temperature Self-Refresh entry.

a) if SPD Byte 49 Bit 0 is a "0" means DRAM does not support Self-Refresh at higher than 85 °C, then system have to ensure the DRAM is at or below 85 °C case temperature before initiating Self-Refresh operation.

b) if SPD Byte 49 Bit 0 is a "1" means DRAM supports Self-Refresh at higher than 85 °C case temperature, then system can use register bit A7 at EMSR(2) to control DRAM to operate at proper Self-Refresh rate for higher temperate. Please also refer to EMR(2) register definition section and DDR2 DIMM SPD definition for details.

For more detail, please refer to JEP-179 DDR2 SDRAM Operating Temperature Application Note.

For the system users who use non-standard DIMM module or discrete parts, please refer to DRAM manufacture specifications to verify the DRAM capability supporting Self-Refresh at higher temperature.

Table 18 — ODT DC electrical characteristics

PARAMETER/CONDITION	SYMBOL	MIN	NOM	MAX	UNITS	NOTES
Rtt effective impedance value for EMRS(A6,A2)=0,1; 75 Ω	Rtt1(eff)	60	75	90	Ω	1
Rtt effective impedance value for EMRS(A6,A2)=1,0; 150 Ω	Rtt2(eff)	120	150	180	Ω	1
Rtt effective impedance value for EMRS(A6,A2)=1,1; 50 Ω	Rtt3(eff)	40	50	60	Ω	1, 2
Deviation of VM with respect to VDDQ/2	ΔVM	- 6		+ 6	%	1

NOTE 1 Test condition for Rtt measurements

NOTE 2 Optional for DDR2-400/533/667, mandatory for DDR2-800.

Measurement Definition for Rtt(eff): Apply $V_{IH}(ac)$ and $V_{IL}(ac)$ to test pin separately, then measure current $I(V_{IH}(ac))$ and $I(V_{IL}(ac))$ respectively. $V_{IH}(ac)$, $V_{IL}(ac)$, and VDDQ values defined in SSTL_18

$$\mathrm{Rtt(eff)} \quad \frac{V_{IH}(ac) - V_{IL}(ac)}{I(V_{IH}(ac)) - I(V_{IL}(ac))}$$

5 AC & DC operating conditions (cont'd)

Measurement Definition for VM: Measure voltage (VM) at test pin (midpoint) with no load.

$$\Delta VM = \left(\frac{2 \times Vm}{VDDQ} - 1\right) \times 100\%$$

Table 19 — Input DC logic level

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IH}(dc)	dc input logic HIGH	VREF + 0.125	VDDQ + 0.3	V	
V_{IL}(dc)	dc input logic LOW	- 0.3	VREF - 0.125	V	

Table 20 — Input AC logic level

Symbol	Parameter	DDR2-400, DDR2-533		DDR2-667, DDR2-800		Units
		Min.	Max.	Min.	Max.	
V_{IH} (ac)	ac input logic HIGH	VREF + 0.250	-	VREF + 0.200	-	V
V_{IL} (ac)	ac input logic LOW	-	VREF - 0.250		VREF - 0.200	V

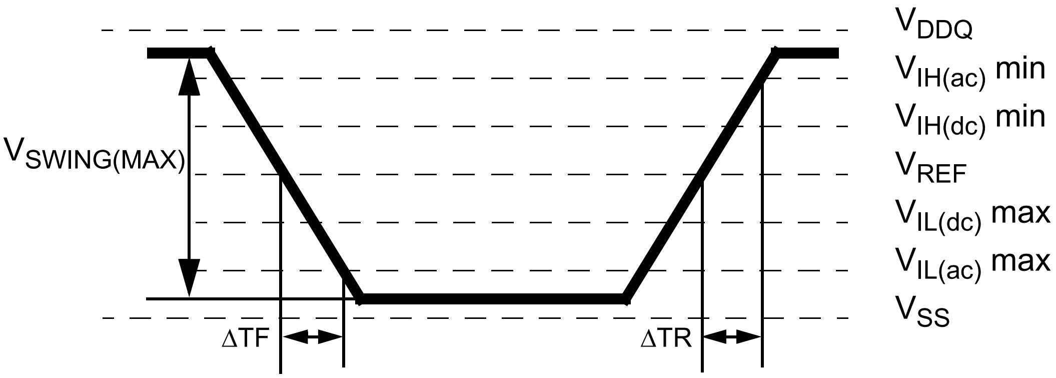
Table 21 — AC input test conditions

Symbol	Condition	Value	Units	Notes
V_{REF}	Input reference voltage	0.5 x V_{DDQ}	V	1
$V_{SWING(MAX)}$	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

NOTE 1 Input waveform timing is referenced to the input signal crossing through the $V_{IH/IL(AC)}$ level applied to the device under test.

NOTE 2 The input signal minimum slew rate is to be maintained over the range from V_{REF} to $V_{IH(ac)}$ min for rising edges and the range from V_{REF} to $V_{IL(ac)}$ max for falling edges as shown in the below figure.

NOTE 3 AC timings are referenced with input waveforms switching from VIL(ac) to VIH(ac) on the positive transitions and VIH(ac) to VIL(ac) on the negative transitions.



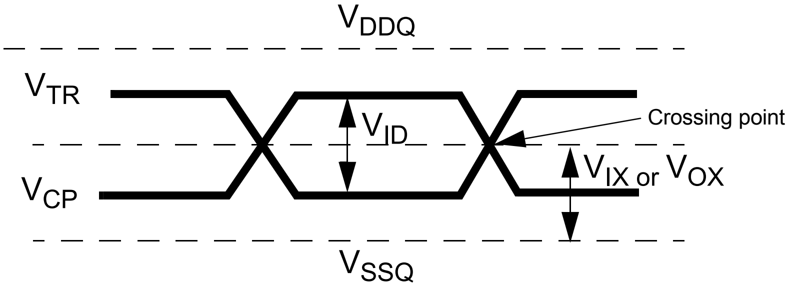
$$\text{Falling Slew} = \frac{V_{REF} - V_{IL(ac)}\ \text{max}}{\Delta TF} \qquad \text{Rising Slew} = \frac{V_{IH(ac)}\ \text{min} - V_{REF}}{\Delta TR}$$

Figure 72 — AC input test signal waveform

5 AC & DC operating conditions (cont'd)

Table 22 — Differential input AC logic level

Symbol	Parameter	Min.	Max.	Units	Notes
V_{ID} (ac)	ac differential input voltage	0.5	VDDQ + 0.6	V	1
V_{IX} (ac)	ac differential crosspoint voltage	0.5 x VDDQ - 0.175	0.5 x VDDQ + 0.175	V	2



NOTE 1 $V_{ID(AC)}$ specifies the input differential voltage $|V_{TR} - V_{CP}|$ required for switching, where V_{TR} is the true input signal (such as CK, DQS, LDQS or UDQS) and V_{CP} is the complementary input signal (such as $\overline{\text{CK}}$, $\overline{\text{DQS}}$, $\overline{\text{LDQS}}$ or $\overline{\text{UDQS}}$). The minimum value is equal to $V_{IH(AC)} - V_{IL(AC)}$.

NOTE 2 The typical value of $V_{IX(AC)}$ is expected to be about 0.5 x VDDQ of the transmitting device and $V_{IX(AC)}$ is expected to track variations in VDDQ. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.

Figure 73 — Differential signal levels

Table 23 — Differential AC output parameters

Symbol	Parameter	Min.	Max.	Units	Notes
V_{OX} (ac)	ac differential crosspoint voltage	0.5 x VDDQ - 0.125	0.5 x VDDQ + 0.125	V	1

NOTE 1 The typical value of $V_{OX(AC)}$ is expected to be about 0.5 x VDDQ of the transmitting device and $V_{OX(AC)}$) is expected to track variations in VDDQ . $V_{OX(AC)}$ indicates the voltage at which differential output signals must cross.

Overshoot/undershoot specification

Table 24 — AC overshoot/undershoot specification for address and control pins:
A0-A15, BA0-BA2, $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, CKE, ODT

Parameter	Specification			
	DDR2-400	DDR2-533	DDR2-667	DDR2-800
Maximum peak amplitude allowed for overshoot area (See Figure 74):	0.5(0.9)[1] V	0.5(0.9)[1] V	0.5(0.9)[1] V	0.5(0.9)[1] V
Maximum peak amplitude allowed for undershoot area (See Figure 74):	0.5(0.9)[1] V	0.5(0.9)[1] V	0.5(0.9)[1] V	0.5(0.9)[1] V
Maximum overshoot area above VDD (See Figure 74).	1.33 V-ns	1.0 V-ns	0.8 V-ns	0.66 V-ns
Maximum undershoot area below VSS (See Figure 74).	1.33 V-ns	1.0 V-ns	0.8 V-ns	0.66 V-ns
NOTE 1 The maximum requirements for peak amplitude were reduced from 0.9V to 0.5V. Register vendor data sheets will specify the maximum over/undershoot induced in specific RDIMM applications. DRAM vendor data sheets will also specify the maximum overshoot/undershoot that their DRAM can tolerate. This will allow the RDIMM supplier to understand whether the DRAM can tolerate the overshoot that the register will induce in the specific RDIMM application.				

5 AC & DC operating conditions (cont'd)

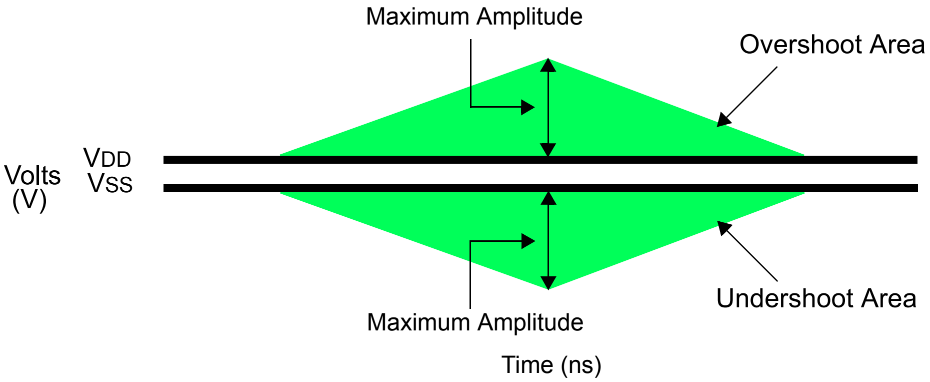


Figure 74 — AC overshoot and undershoot definition for address and control pins

Table 25 — AC overshoot/undershoot specification for clock, data, strobe, and mask pins: DQ, (U/L/R)DQS, $\overline{\text{(U/L/R)DQS}}$, DM, CK, $\overline{\text{CK}}$

Parameter	Specification			
	DDR2-400	**DDR2-533**	**DDR2-667**	**DDR2-800**
Maximum peak amplitude allowed for overshoot area (See Figure 75):	0.5 V	0.5 V	0.5 V	0.5 V
Maximum peak amplitude allowed for undershoot area (See Figure 75):	0.5 V	0.5 V	0.5 V	0.5 V
Maximum overshoot area above VDDQ (See Figure 75).	0.38 V-ns	0.28 V-ns	0.23 V-ns	0.23 V-ns
Maximum undershoot area below VSSQ (See Figure 75).	0.38 V-ns	0.28 V-ns	0.23 V-ns	0.23 V-ns

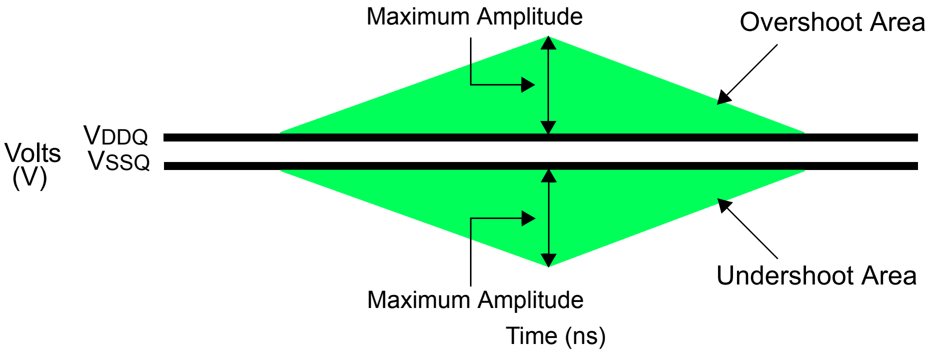


Figure 75 — AC overshoot and undershoot definition for clock, data, strobe, and mask pins

Power and ground clamps are required on the following input only pins:

a) BA0-BAx

b) A0-Axx

c) $\overline{\text{RAS}}$

d) $\overline{\text{CAS}}$

e) $\overline{\text{WE}}$

f) $\overline{\text{CS}}$

g) ODT

h) CKE

5 AC & DC operating conditions (cont'd)

Table 26 — V-I characteristics for input-only pins with clamps

Voltage across Clamp (V)	Minimum Power Clamp Current (mA)	Minimum Ground Clamp Current (mA)
0.0	0	0
0.1	0	0
0.2	0	0
0.3	0	0
0.4	0	0
0.5	0	0
0.6	0	0
0.7	0	0
0.8	0.1	0.1
0.9	1.0	1.0
1.0	2.5	2.5
1.1	4.7	4.7
1.2	6.8	6.8
1.3	9.1	9.1
1.4	11.0	11.0
1.5	13.5	13.5
1.6	16.0	16.0
1.7	18.2	18.2
1.8	21.0	21.0

Output buffer characteristics

Table 27 — Output AC test conditions

Symbol	Parameter	SSTL_18	Units	Notes
V_{OTR}	Output Timing Measurement Reference Level	0.5 x V_{DDQ}	V	1

NOTE 1 The VDDQ of the device under test is referenced.

Table 28 — Output DC current drive

Symbol	Parameter	SSTl_18	Units	Notes
$I_{OH(dc)}$	Output Minimum Source DC Current	- 13.4	mA	1, 3, 4
$I_{OL(dc)}$	Output Minimum Sink DC Current	13.4	mA	2, 3, 43

NOTE 1 V_{DDQ} = 1.7 V; V_{OUT} = 1420 mV. (V_{OUT} - V_{DDQ})/I_{OH} must be less than 21 Ω for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280 mV.

NOTE 2 V_{DDQ} = 1.7 V; V_{OUT} = 280 mV. V_{OUT}/I_{OL} must be less than 21 Ω for values of V_{OUT} between 0 V and 280 mV.

NOTE 3 The dc value of V_{REF} applied to the receiving device is set to V_{TT}

NOTE 4 The values of $I_{OH(dc)}$ and $I_{OL(dc)}$ are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure V_{IH} min plus a noise margin and V_{IL} max minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point (see Section 3.3 of JESD8-15A) along a 21 Ω load line to define a convenient driver current for measurement.

5 AC & DC operating conditions (cont’d)

Table 29 — OCD default characteristics

Description	Parameter	Min	Nom	Max	Unit	Notes
Output impedance		See full strength default driver characteristics			Ω	1
Output impedance step size for OCD calibration		0		1.5	Ω	6
Pull-up and pull-down mismatch		0		4	Ω	1,2,3
Output slew rate	Sout	1.5		5	V/ns	1,4,5,7,8,9

NOTE 1 Absolute Specifications (TOPER; VDD = +1.8V ±0.1V, VDDQ = +1.8V ±0.1V). DRAM I/O specifications for timing, voltage, and slew rate are no longer applicable if OCD is changed from default settings.

NOTE 2 Impedance measurement condition for output source dc current: VDDQ = 1.7 V; VOUT = 1420 mV; (VOUT-VDDQ)/Ioh must be less than 23.4 Ω for values of VOUT between VDDQ and VDDQ - 280 mV. Impedance measurement condition for output sink dc current: VDDQ = 1.7 V; VOUT = 280 mV; VOUT/Iol must be less than 23.4 Ω for values of VOUT between 0 V and 280 mV.

NOTE 3 Mismatch is absolute value between pull-up and pull-down, both are measured at same temperature and voltage.

NOTE 4 Slew rate measured from vil(ac) to vih(ac).

NOTE 5 The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterization.

NOTE 6 This represents the step size when the OCD is near 18 Ω at nominal conditions across all process corners/variations and represents only the DRAM uncertainty. A 0 Ω value (no calibration) can only be achieved if the OCD impedance is 18 Ω +/-0.75 Ω under nominal conditions.

NOTE 7 DRAM output slew rate specification applies to 400 MT/s, 533 MT/s & 667 MT/s speed bins.

NOTE 8 Timing skew due to DRAM output slew rate mis-match between DQS / $\overline{\text{DQS}}$ and associated DQ’s is included in tDQSQ and tQHS specification.

NOTE 9 DDR2 SDRAM output slew rate test load is defined in General Note 3 of the AC Timing specification Table.

DDR2 SDRAM default output driver V–I characteristics

DDR2 SDRAM output driver characteristics are defined for full strength default operation as selected by the EMR(1) bits A7-A9 = ‘111’. Figures 76, 77, 78 and 79 show the driver characteristics graphically, and Tables 30, 31, 32 and 33 show the same data in tabular format suitable for input into simulation tools. The driver characteristics evaluation conditions are:

a) Nominal Default 25 ^{o}C (T case), VDDQ = 1.8 V, typical process

b) Minimum TOPER(max), VDDQ = 1.7 V, slow–slow process

c) Maximum 0 ^{o}C (T case), VDDQ = 1.9 V, fast–fast process

Default output driver characteristic curves notes:

1) The full variation in driver current from minimum to maximum process, temperature, and voltage will lie within the outer bounding lines of the V–I curve of Figures 76, 77, 78 and 79.

2) It is recommended that the “typical” IBIS V–I curve lie within the inner bounding lines of the V–I curves of Figures 76, 77, 78 and 79.

5 AC & DC operating conditions (cont’d)

Table 30 — Full strength default pulldown driver characteristics

	Pulldown Current (mA)			
Voltage (V)	Minimum	Suggested IBIS Target Low	Suggested IBIS Target High	Maximum
0.0	0.00	0.00	0.00	0.00
0.1	4.30	5.65	5.90	7.95
0.2	8.60	11.30	11.80	15.90
0.3	12.90	16.50	16.80	23.85
0.4	16.90	21.20	22.10	31.80
0.5	20.05	25.00	27.60	39.75
0.6	22.10	28.30	32.40	47.70
0.7	23.27	30.90	36.90	55.55
0.8	24.10	33.00	40.90	62.95
0.9	24.73	34.50	44.60	69.55
1.0	25.23	35.50	47.70	75.35
1.1	25.65	36.10	50.40	80.35
1.2	26.02	36.60	52.60	84.55
1.3	26.35	36.90	54.20	87.95
1.4	26.65	37.10	55.90	90.70
1.5	26.93	37.40	57.10	93.00
1.6	27.20	37.60	58.40	95.05
1.7	27.46	37.70	59.60	97.05
1.8		37.90	60.90	99.05
1.9				101.05

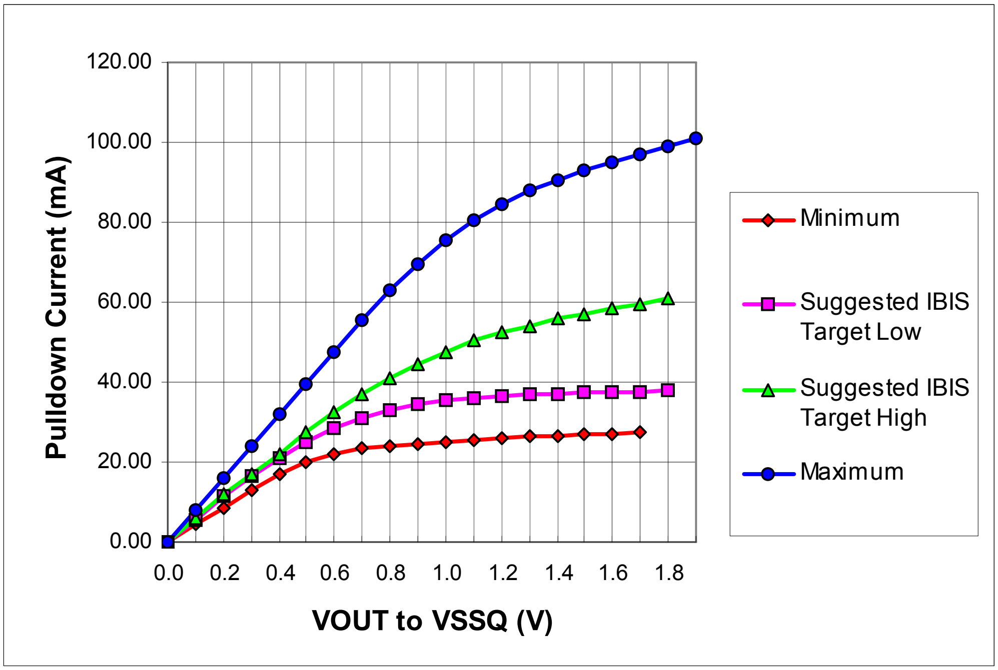


Figure 76 — DDR2 default pulldown characteristics for full strength driver

5 AC & DC operating conditions (cont'd)

Table 31 — Full strength default pullup driver characteristics

	Pulldown Current (mA)			
Voltage (V)	Minimum	Nominal Default Low	Nominal Default High	Maximum
0.0	0.00	0.00	0.00	0.00
0.1	4.30	5.65	5.90	7.95
0.2	8.60	11.30	11.80	15.90
0.3	12.90	16.50	16.80	23.85
0.4	16.90	21.20	22.10	31.80
0.5	20.05	25.00	27.60	39.75
0.6	22.10	28.30	32.40	47.70
0.7	23.27	30.90	36.90	55.55
0.8	24.10	33.00	40.90	62.95
0.9	24.73	34.50	44.60	69.55
1.0	25.23	35.50	47.70	75.35
1.1	25.65	36.10	50.40	80.35
1.2	26.02	36.60	52.60	84.55
1.3	26.35	36.90	54.20	87.95
1.4	26.65	37.10	55.90	90.70
1.5	26.93	37.40	57.10	93.00
1.6	27.20	37.60	58.40	95.05
1.7	27.46	37.70	59.60	97.05
1.8		37.90	60.90	99.05
1.9				101.05

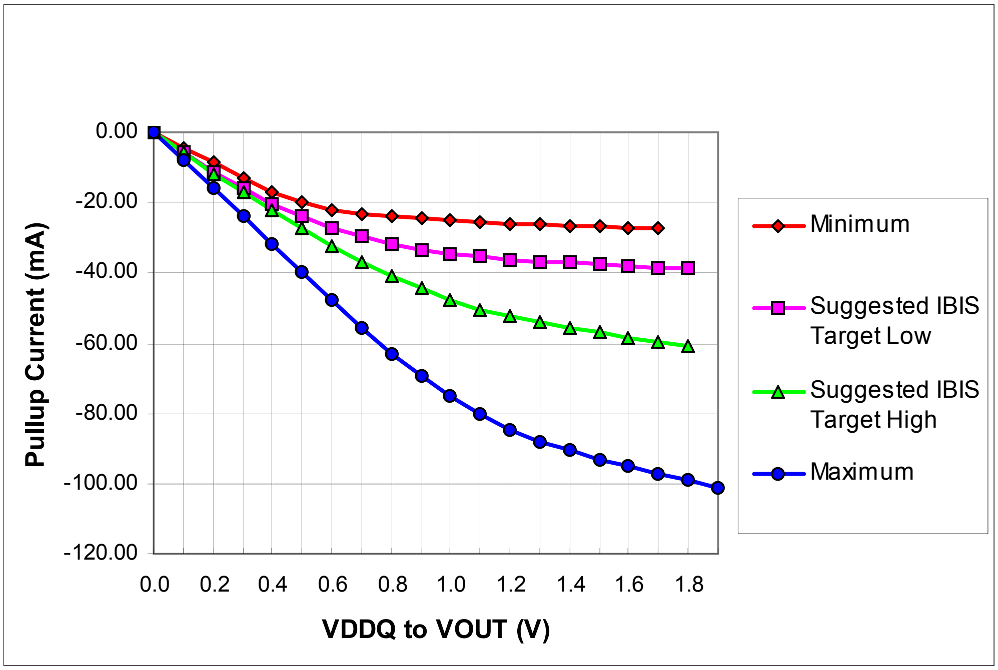


Figure 77 — DDR2 default pullup characteristics for full strength output driver

5 AC & DC operating conditions (cont'd)

Table 32 — Reduced strength default pulldown driver characteristics

	Pulldown Current (mA)			
Voltage (V)	Minimum	Suggested IBIS Target Low	Suggested IBIS Target High	Maximum
0.0	0.00	0.00	0.00	0.00
0.1	1.72	3.24	4.11	4.77
0.2	3.44	6.25	8.01	9.54
0.3	5.16	9.03	11.67	14.31
0.4	6.76	11.52	15.03	19.08
0.5	8.02	13.66	18.03	23.85
0.6	8.84	15.41	20.61	28.62
0.7	9.31	16.77	22.71	33.33
0.8	9.64	17.74	24.35	37.77
0.9	9.89	18.38	25.56	41.73
1.0	10.09	18.80	26.38	45.21
1.1	10.26	19.06	26.90	48.21
1.2	10.41	19.23	27.24	50.73
1.3	10.54	19.35	27.47	52.77
1.4	10.66	19.46	27.64	54.42
1.5	10.77	19.56	27.78	55.80
1.6	10.88	19.65	27.89	57.03
1.7	10.98	19.73	27.97	58.23
1.8		19.80	28.02	59.43
1.9				60.63

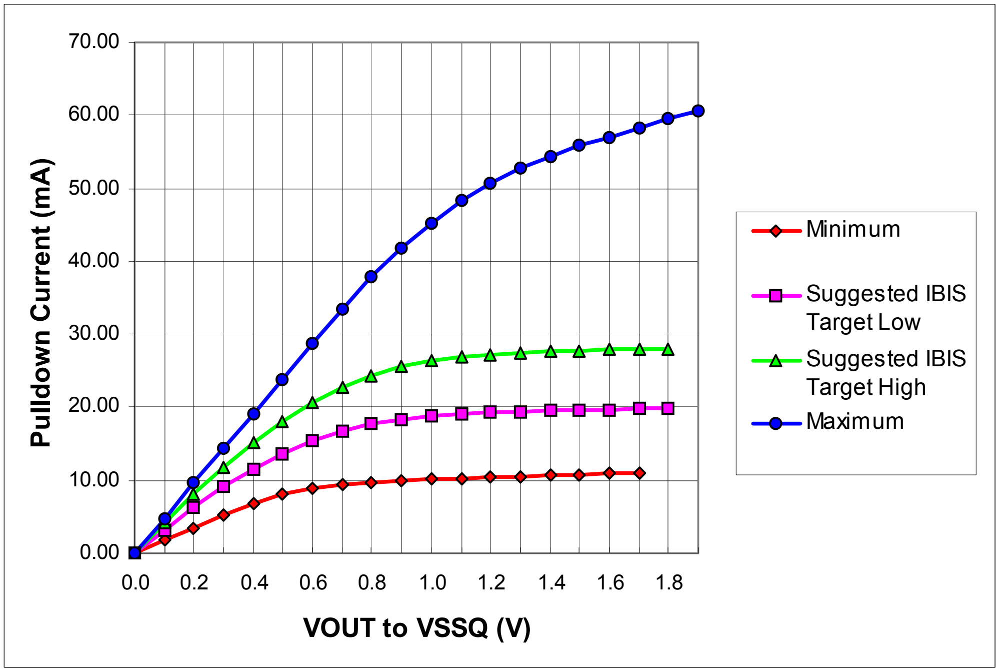


Figure 78 — DDR2 default pulldown characteristics for reduced strength drive

5 AC & DC operating conditions (cont'd)

Table 33 — Reduced strength default pullup driver characteristics

	Pullup Current (mA)			
Voltage (V)	Minimum	Suggested IBIS Target Low	Suggested IBIS Target High	Maximum
0.0	0.00	0.000	0.00	0.00
0.1	-1.72	-3.200	-3.70	-4.77
0.2	-3.44	-6.200	-7.22	-9.54
0.3	-5.16	-9.040	-10.56	-14.31
0.4	-6.76	-11.690	-13.75	-19.08
0.5	-8.02	-14.110	-16.78	-23.85
0.6	-8.84	-16.270	-19.61	-28.62
0.7	-9.31	-18.160	-22.20	-33.33
0.8	-9.64	-19.770	-24.50	-37.77
0.9	-9.89	-21.100	-26.46	-41.73
1.0	-10.09	-22.150	-28.07	-45.21
1.1	-10.26	-22.960	-29.36	-48.21
1.2	-10.41	-23.610	-30.40	-50.73
1.3	-10.54	-24.160	-31.24	-52.77
1.4	-10.66	-24.640	-31.93	-54.42
1.5	-10.77	-25.070	-32.51	-55.80
1.6	-10.88	-25.470	-33.01	-57.03
1.7	-10.98	-25.850	-33.46	-58.23
1.8		-26.210	-33.89	-59.43
1.9				-60.63

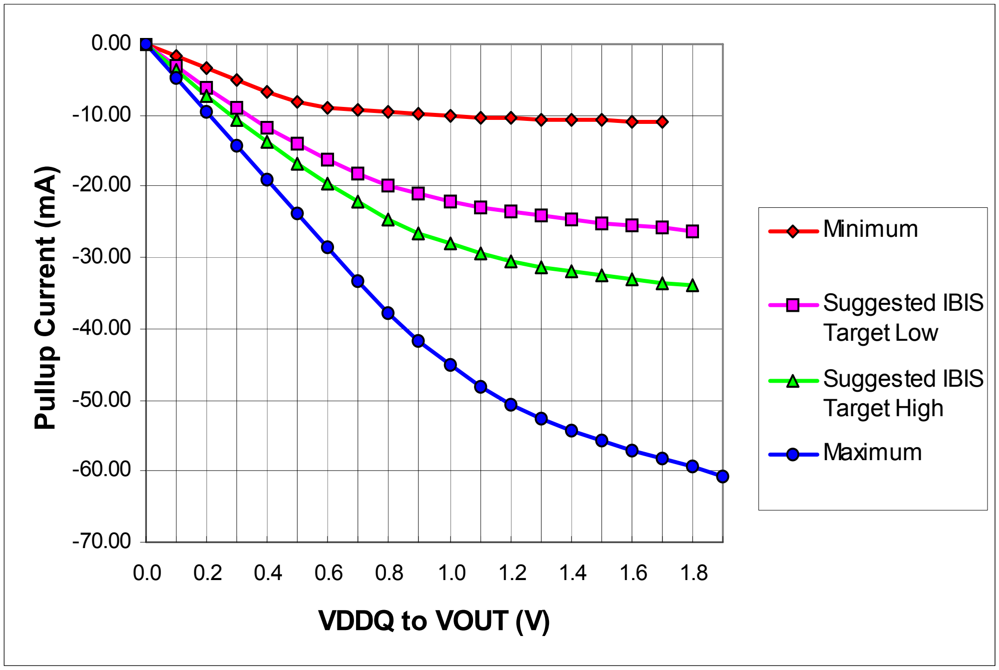


Figure 79 — DDR2 default pullup characteristics for reduced strength driver

5 AC & DC operating conditions (cont'd)

DDR2 SDRAM calibrated output driver V–I characteristics

DDR2 SDRAM output driver characteristics are defined for full strength calibrated operation as selected by the procedure outlined in section 2.4.3 Off-chip driver (OCD) impedance adjustment. Tables 34 and 35 show the data in tabular format suitable for input into simulation tools. The nominal points represent a device at exactly 18 Ω. The nominal low and nominal high values represent the range that can be achieved with a maximum 1.5 Ω step size with no calibration error at the exact nominal conditions only (i.e. perfect calibration procedure, 1.5 Ω maximum step size guaranteed by specification). Real system calibration error needs to be added to these values. It must be understood that these V-I curves as represented here or in supplier IBIS models need to be adjusted to a wider range as a result of any system calibration error. Since this is a system specific phenomena, it cannot be quantified here. The values in the calibrated tables represent just the DRAM portion of uncertainty while looking at one DQ only. If the calibration procedure is used, it is possible to cause the device to operate outside the bounds of the default device characteristics tables and figures. In such a situation, the timing parameters in the specification cannot be guaranteed. It is solely up to the system application to ensure that the device is calibrated between the minimum and maximum default values at all times. If this can't be guaranteed by the system calibration procedure, re-calibration policy, and uncertainty with DQ to DQ variation, then it is recommended that only the default values be used. The nominal maximum and minimum values represent the change in impedance from nominal low and high as a result of voltage and temperature change from the nominal condition to the maximum and minimum conditions. If calibrated at an extreme condition, the amount of variation could be as much as from the nominal minimum to the nominal maximum or vice versa. The driver characteristics evaluation conditions are:

a) Nominal 25 °C (T case), VDDQ = 1.8 V, typical process

b) Nominal Low and Nominal High 25 °C (T case), VDDQ = 1.8 V, any process

c) Nominal Minimum TOPER(max), VDDQ = 1.7 V, any process

d) Nominal Maximum 0 °C (T case), VDDQ = 1.9 V, any process

Table 34 — Full strength calibrated pulldown driver characteristics

	Calibrated Pulldown Current (mA)				
Voltage (V)	Nominal Minimum (21 Ω)	Nominal Low (18.75 Ω)	Nominal (18 Ω)	Nominal High (17.25 Ω)	Nominal Maximum (15 Ω)
0.2	9.5	10.7	11.5	11.8	13.3
0.3	14.3	16.0	16.6	17.4	20.0
0.4	18.7	21.0	21.6	23.0	27.0

Table 35 — Full strength calibrated pullup driver characteristics

	Calibrated Pullup Current (mA)				
Voltage (V)	Nominal Minimum (21 Ω)	Nominal Low (18.75 Ω)	Nominal (18 Ω)	Nominal High (17.25 Ω)	Nominal Maximum (15 Ω)
0.2	- 9.5	- 10.7	- 11.4	- 11.8	- 13.3
0.3	- 14.3	- 16.0	- 16.5	- 17.4	- 20.0
0.4	- 18.7	- 21.0	- 21.2	- 23.0	- 27.0

5 AC & DC operating conditions (cont’d)

Table 36 — IDD specification parameters and test conditions

(IDD values are for full operating range of Voltage and Temperature, Notes 1 - 6)

Symbol	Conditions		Max	Units	Notes
IDD0	**Operating one bank active-precharge current**; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RASmin(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING			mA	
IDD1	**Operating one bank active-read-precharge current**; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC\ (IDD)}$, $t_{RAS} = t_{RASmin(IDD)}$, $t_{RCD} = t_{RCD(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W			mA	
IDD2P	**Precharge power-down current**; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING			mA	
IDD2Q	**Precharge quiet standby current**; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING			mA	
IDD2N	**Precharge standby current**; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING			mA	
IDD3P	**Active power-down current**; All banks open; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0		mA	
		Slow PDN Exit MRS(12) = 1		mA	
IDD3N	**Active standby current**; All banks open; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING			mA	

5 AC & DC operating conditions (cont’d)

Table 36 — IDD specification parameters and test conditions

(IDD values are for full operating range of Voltage and Temperature, Notes 1 - 6)

Symbol	Conditions	Max	Units	Notes
IDD4W	**Operating burst write current**; All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD4R	**Operating burst read current**; All banks open, Continuous burst reads, IOUT = 0 mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		mA	
IDD5B	**Burst refresh current**; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD6	**Self refresh current**; CK and $\overline{CK}$ at 0 V; CKE $\leq$ 0.2 V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING		mA	
IDD7	**Operating bank interleave read current**; All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = tRCD(IDD) - 1 x tCK(IDD); tCK = tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tFAW = tFAW(IDD), tRCD = 1 x tCK(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; - Refer to the following pages for detailed timing conditions		mA	

5 AC & DC operating conditions (cont'd)

Table 36 — IDD specification parameters and test conditions

(IDD values are for full operating range of Voltage and Temperature, Notes 1 - 6)

Symbol	Conditions	Max	Units	Notes

NOTE 1 IDD specifications are tested after the device is properly initialized

NOTE 2 Input slew rate is specified by AC Parametric Test Condition

NOTE 3 IDD parameters are specified with ODT disabled.

NOTE 4 Data bus consists of DQ, DM, DQS, $\overline{\text{DQS}}$, RDQS, $\overline{\text{RDQS}}$, LDQS, $\overline{\text{LDQS}}$, UDQS, and $\overline{\text{UDQS}}$. IDD values must be met with all combinations of EMRS bits 10 and 11.

NOTE 5 For DDR2-667/800 testing, tCK in the Conditions should be interpreted as tCK(avg)

NOTE 6 Definitions for IDD
LOW = Vin ≤ VILAC(max)
HIGH = Vin ≥ VIHAC(min)
STABLE = inputs stable at a HIGH or LOW level
FLOATING = inputs at VREF = VDDQ/2
SWITCHING = inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks or strobes.

IDD testing parameters

For purposes of IDD testing, the parameters in Table 37 are to be utilized.

Table 37 — IDD testing parameters

Speed	DDR2-800			DDR2-667		DDR2-533		DDR2-400		Units
Bin(CL-tRCD-tRP)	4-4-4	5-5-5	6-6-6	4-4-4	5-5-5	3-3-3	4-4-4	3-3-3	4-4-4	
CL(IDD)	4	5	6	4	5	3	4	3	4	tCK
tRCD(IDD)	10	12.5	15	12	15	11.25	15	15	20	ns
tRC(IDD)	55	57.5	60	57	60	56.25	60	55	65	ns
tRRD(IDD)-1KB	7.5	7.5	7.5	7.5	7.5	7.5	7.5	7.5	7.5	ns
tRRD(IDD)-2KB	10	10	10	10	10	10	10	10	10	ns
tFAW(IDD)-1KB	35	35	35	37.5	37.5	37.5	37.5	37.5	37.5	ns
tFAW(IDD)-2KB	45	45	45	50	50	50	50	50	50	ns
tCK(IDD)	2.5	2.5	2.5	3	3	3.75	3.75	5	5	ns
tRASmin(IDD)	45	45	45	45	45	45	45	40	45	ns
tRASmax(IDD)	70000	70000	70000	70000	70000	70000	70000	70000	70000	ns
tRP(IDD)	10	12.5	15	12	15	11.25	15	15	20	ns
tRFC(IDD)-256Mb	75	75	75	75	75	75	75	75	75	ns
tRFC(IDD)-512Mb	105	105	105	105	105	105	105	105	105	ns
tRFC(IDD)-1Gb	127.5	127.5	127.5	127.5	127.5	127.5	127.5	127.5	127.5	ns
tRFC(IDD)-2Gb	197.5	197.5	197.5	197.5	197.5	197.5	197.5	197.5	197.5	ns
tRFC(IDD)-4Gb	327.5	327.5	327.5	327.5	327.5	327.5	327.5	327.5	327.5	ns

5 AC & DC operating conditions (cont'd)

Detailed IDD7

The detailed timings are shown below for IDD7. Changes will be required if timing parameter changes are made to the specification.

Legend: A = Active; RA = Read with Autoprecharge; D = Deselect

IDD7: Operating Current: All Bank Interleave Read operation

All banks are being interleaved at minimum ^{t}RC(IDD) without violating ^{t}RRD(IDD) and ^{t}FAW(IDD) using a burst length of 4. Control and address bus inputs are STABLE during DESELECTs. IOUT = 0 mA

Timing Patterns for 4 bank devices with 1 KB or 2 KB page size

-DDR2-400 4-4-4: A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D D D D

-DDR2-400 3-3-3: A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D D

-DDR2-533 4-4-4: A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D D

-DDR2-533 3-3-3: A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D

-DDR2-667 5-5-5: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D

-DDR2-667 4-4-4: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D

-DDR2-800 6-6-6: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D D D D D

-DDR2-800 5-5-5: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D D D D

-DDR2-800 4-4-4: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D D D

Timing Patterns for 8 bank devices with 1 KB page size

-DDR2-400 all bins: A0 RA0 A1 RA1 A2 RA2 A3 RA3 A4 RA4 A5 RA5 A6 RA6 A7 RA7

-DDR2-533 all bins: A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D A4 RA4 A5 RA5 A6 RA6 A7 RA7 D D

-DDR2-667 all bins: A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D A4 RA4 D A5 RA5 D A6 RA6 D A7 RA7 D D

-DDR2-800 all bins: A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D A4 RA4 D A5 RA5 D A6 RA6 D A7 RA7 D D D

Timing Patterns for 8 bank devices with 2 KB page size

-DDR2-400 all bins: A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D A4 RA4 A5 RA5 A6 RA6 A7 RA7 D D

-DDR2-533 all bins: A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D A4 RA4 D A5 RA5 D A6 RA6 D A7 RA7 D D D

-DDR2-667 all bins: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D

-DDR2-800 all bins: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D

Table 38 — Input/output capacitance

Parameter	Symbol	DDR2-400 DDR2-533		DDR2-667		DDR2-800		
		Min	Max	Min	Max	Min	Max	Units
Input capacitance, CK and $\overline{\text{CK}}$	CCK	1.0	2.0	1.0	2.0	1.0	2.0	pF
Input capacitance delta, CK and $\overline{\text{CK}}$	CDCK	x	0.25	x	0.25	x	0.25	pF
Input capacitance, all other input-only pins	CI	1.0	2.0	1.0	2.0	1.0	1.75	pF
Input capacitance delta, all other input-only pins	CDI	x	0.25	x	0.25	x	0.25	pF
Input/output capacitance, DQ, DM, DQS, $\overline{\text{DQS}}$	CIO	2.5	4.0	2.5	3.5	2.5	3.5	pF
Input/output capacitance delta, DQ, DM, DQS, $\overline{\text{DQS}}$	CDIO	x	0.5	x	0.5	x	0.5	pF

5 AC & DC operating conditions (cont'd)

Electrical characteristics & AC timing for DDR2-400/533/667/800 - absolute specification

(TOPER; V_{DDQ} = 1.8 V +/– 0.1 V; V_{DD} = 1.8 V +/– 0.1 V)

Table 39 — Refresh parameters by device density

Parameter	Symbol		256 Mb	512 Mb	1 Gb	2 Gb	4 Gb	Units	Note
Refresh to active/Refresh command time	tRFC		75	105	127.5	195	327.5	ns	1
Average periodic refresh interval	tREFI	0 °C ≤ T_{CASE} ≤ 85 °C	7.8	7.8	7.8	7.8	7.8	µs	1
		85 °C < T_{CASE} ≤ 95 °C	3.9	3.9	3.9	3.9	3.9	µs	1, 2

NOTE 1 If refresh timing is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.
NOTE 2 This is an optional feature. For detailed information, please refer to “operating temperature condition” chapter in this spec

Table 40 — DDR2 SDRAM standard speed bins and tCK/tCK(avg), tRCD, tRP, tRAS and tRC for corresponding bin

Speed bin	DDR2-800C		DDR2-800D		DDR2-800E		DDR2-667C		DDR2-667D		Units	Notes
CL - tRCD - tRP	4 - 4 - 4		5 - 5 - 5		6 - 6 - 6		4 - 4 - 4		5 - 5 - 5			
Parameter	min	max	min	max	min	max	min	max	min	max		
tRCD	10	-	12.5	-	15	-	12	-	15	-	ns	2
tRP[1]	10	-	12.5	-	15	-	12	-	15	-	ns	2
tRC	55	-	57.5	-	60	-	57	-	60	-	ns	2
tRAS	45	70000	45	70000	45	70000	45	70000	45	70000	ns	2,3
tCK(avg) @ CL=2	Optional		Optional		Optional		Optional		Optional		ns	4
tCK(avg) @ CL=3	Optional		Optional		Optional		Optional		Optional		ns	4
tCK(avg) @ CL=4	2.5	8	3.75	8	3.75	8	3	8	3.75	8	ns	4
tCK(avg) @ CL=5	2.5	8	2.5	8	3	8	3	8	3	8	ns	4
tCK(avg) @ CL=6	Optional		Optional		2.5	8	Optional		Optional		ns	4

Speed bin	DDR2-533B		DDR2-533C		DDR2-400B		DDR2-400C		Units
CL - tRCD - tRP	3 - 3 - 3		4 - 4 - 4		3 - 3 - 3		4 - 4 - 4		
Parameter	min	max	min	max	min	max	min	max	
tRCD: ACT to RD(A) or WT(A) Delay	11.25	-	15	-	15	-	20	-	ns
tRP[1]: PRE to ACT Delay	11.25	-	15	-	15	-	20	-	ns
tRC: ACT to ACT Delay	56.25	-	60	-	55	-	65	-	ns
tRAS: ACT to PRE Delay	45	70000	45	70000	40	70000	45	70000	ns
tCK @ CL=2	Optional		Optional		Optional		Optional		ns
tCK @ CL=3	3.75	8	5	8	5	8	Optional		ns
tCK @ CL=4	3.75	8	3.75	8	5	8	5	8	ns
tCK @ CL=5	Optional		Optional		Optional		Optional		ns
tCK @ CL=6	Optional		Optional		Optional		Optional		ns

NOTE 1 8 bank device Precharge All Allowance : tRPall for a Precharge All command for an 8 Bank device is equal to tRP + 1 x tCK, where tRP is the value for a single bank precharge, which are shown in this table.
NOTE 2 Refer to Specific Notes 32.
NOTE 3 Refer to Specific Notes 3.
NOTE 4 Refer to Specific Notes 35.

5 AC & DC operating conditions (cont'd)

Table 41 — Timing parameters by speed grade (DDR2-400 and DDR2-533)

(For information related to the entries in this table, refer to both the General Notes and the Specific Notes following Table 42.)

Parameter	**Symbol**	DDR2-400		DDR2-533		**Units**	**Specific Notes**
		min	**max**	**min**	**max**		
Clock cycle time, CL=x	tCK	5000	8000	3750	8000	ps	15
CK HIGH pulse width	tCH	0.45	0.55	0.45	0.55	tCK	
CK LOW pulse width	tCL	0.45	0.55	0.45	0.55	tCK	
Write command to DQS associated clock edge	WL	RL - 1		RL - 1		tCK	
DQS latching rising transitions to associated clock edges	tDQSS	- 0.25	0.25	- 0.25	0.25	tCK	
DQS falling edge to CK setup time	tDSS	0.2	x	0.2	x	tCK	
DQS falling edge hold time from CK	tDSH	0.2	x	0.2	x	tCK	
DQS input HIGH pulse width	tDQSH	0.35	x	0.35	x	tCK	
DQS input LOW pulse width	tDQSL	0.35	x	0.35	x	tCK	
Write preamble	tWPRE	0.35	x	0.35	x	tCK	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK	10
Address and control input setup time	tIS(base)	350	x	250	x	ps	5,7,9,22
Address and control input hold time	tIH(base)	475	x	375	x	ps	5,7,9,23
Control & Address input pulse width for each input	tIPW	0.6	x	0.6	x	tCK	
DQ and DM input setup time (differential strobe)	tDS(base)	150	x	100	x	ps	6,7,8,20, 28
DQ and DM input hold time (differential strobe)	tDH(base)	275	x	225	x	ps	6,7,8,21, 28
DQ and DM input setup time (single-ended strobe)	tDS1(base)	25	x	- 25	x	ps	6,7,8,25
DQ and DM input hold time (single-ended strobe)	tDH1(base)	25	x	- 25	x	ps	6,7,8,26
DQ and DM input pulse width for each input	tDIPW	0.35	x	0.35	x	tCK	
DQ output access time from CK/$\overline{\text{CK}}$	tAC	- 600	+ 600	- 500	+ 500	ps	
DQS output access time from CK/$\overline{\text{CK}}$	tDQSCK	- 500	+ 500	- 450	+ 450	ps	
Data-out high-impedance time from CK/$\overline{\text{CK}}$	tHZ	x	tAC max	x	tAC max	ps	18
DQS(/$\overline{\text{DQS}}$) low-impedance time from CK/$\overline{\text{CK}}$	tLZ(DQS)	tAC min	tAC max	tAC min	tAC max	ps	18
DQ low-impedance time from CK/$\overline{\text{CK}}$	tLZ(DQ)	2 x tAC min	tAC max	2 x tAC min	tAC max	ps	18
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	350	x	300	ps	13
CK half pulse width	tHP	min(tCL, tCH)	x	min(tCL, tCH)	x	ps	11,12
DQ hold skew factor	tQHS	x	450	x	400	ps	12
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	x	tHP - tQHS	x	ps	
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	19
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK	19

5 AC & DC operating conditions (cont'd)

Table 41 — Timing parameters by speed grade (DDR2-400 and DDR2-533)

(For information related to the entries in this table, refer to both the General Notes and the Specific Notes following Table 42.)

Parameter	**Symbol**	DDR2-400		DDR2-533		**Units**	**Specific Notes**
		min	**max**	**min**	**max**		
Active to active command period for 1KB page size products	tRRD	7.5	x	7.5	x	ns	4
Active to active command period for 2KB page size products	tRRD	10	x	10	x	ns	4
Four Activate Window for 1KB page size products	tFAW	37.5		37.5		ns	
Four Activate Window for 2KB page size products	tFAW	50		50		ns	
$\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ command delay	tCCD	2		2		tCK	
Write recovery time	tWR	15	x	15	x	ns	
Auto precharge write recovery + precharge time	tDAL	WR + tRP	x	WR + tRP	x	tCK	14
Internal write to read command delay	tWTR	10	x	7.5	x	ns	24
Internal read to precharge command delay	tRTP	7.5		7.5		ns	3
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE	3		3		tCK	27
Exit self refresh to a non-read command	tXSNR	tRFC + 10		tRFC + 10		ns	
Exit self refresh to a read command	tXSRD	200		200		tCK	
Exit precharge power down to any non-read command	tXP	2	x	2	x	tCK	
Exit active power down to read command	tXARD	2	x	2	x	tCK	1
Exit active power down to read command (slow exit, lower power)	tXARDS	6 - AL		6 - AL		tCK	1,2
ODT turn-on delay	tAOND	2	2	2	2	tCK	16
ODT turn-on	tAON	tAC(min)	tAC(max)+1	tAC(min)	tAC(max)+1	ns	16
ODT turn-on (Power-Down mode)	tAONPD	tAC(min)+2	2 x tCK + tAC(max)+1	tAC(min) + 2	2 x tCK + tAC(max)+1	ns	
ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	tCK	17,44
ODT turn-off	tAOF	tAC(min)	tAC(max) + 0.6	tAC(min)	tAC(max) + 0.6	ns	17,44
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min)+2	2.5 x tCK + tAC(max)+1	tAC(min)+2	2.5 x tCK+ tAC(max)+1	ns	
ODT to power down entry latency	tANPD	3		3		tCK	
ODT power down exit latency	tAXPD	8		8		tCK	
Mode register set command cycle time	tMRD	2	x	2	x	tCK	
MRS command to ODT update delay	tMOD	0	12	0	12	ns	
OCD drive mode output delay	tOIT	0	12	0	12	ns	
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH		tIS+tCK+tIH		ns	15

5 AC & DC operating conditions (cont'd)

Table 42 — Timing parameters by speed grade (DDR2-667 and DDR2-800)

(For information related to the entries in this table, refer to both the General Notes and the Specific Notes following this Table.)

Parameter	Symbol	DDR2-667		DDR2-800		Units^{34}	Specific Notes
		min	max	min	max		
Average clock period	tCK(avg)	3000	8000	2500	8000	ps	35,36
Average clock HIGH pulse width	tCH(avg)	0.48	0.52	0.48	0.52	tCK(avg)	35,36
Average clock LOW pulse width	tCL(avg)	0.48	0.52	0.48	0.52	tCK(avg)	35,36
Write command to DQS associated clock edge	WL	RL - 1		RL - 1		nCK	
DQS latching rising transitions to associated clock edges	tDQSS	- 0.25	0.25	- 0.25	0.25	tCK(avg)	30
DQS falling edge to CK setup time	tDSS	0.2	x	0.2	x	tCK(avg)	30
DQS falling edge hold time from CK	tDSH	0.2	x	0.2	x	tCK(avg)	30
DQS input HIGH pulse width	tDQSH	0.35	x	0.35	x	tCK(avg)	
DQS input LOW pulse width	tDQSL	0.35	x	0.35	x	tCK(avg)	
Write preamble	tWPRE	0.35	x	0.35	x	tCK(avg)	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK(avg)	10
Address and control input setup time	tIS(base)	200	x	175	x	ps	5,7,9,22, 29
Address and control input hold time	tIH(base)	275	x	250	x	ps	5,7,9,23, 29
Control & Address input pulse width for each input	tIPW	0.6	x	0.6	x	tCK(avg)	
DQ and DM input setup time	tDS(base)	100	x	50	x	ps	6,7,8,20, 28,31
DQ and DM input hold time	tDH(base)	175	x	125	x	ps	6,7,8,21, 28,31
DQ and DM input pulse width for each input	tDIPW	0.35	x	0.35	x	tCK(avg)	
DQ output access time from CK/$\overline{\text{CK}}$	tAC	- 450	450	- 400	400	ps	40
DQS output access time from CK/$\overline{\text{CK}}$	tDQSCK	- 400	400	- 350	350	ps	40
Data-out high-impedance time from CK/$\overline{\text{CK}}$	tHZ	x	tAC,max	x	tAC,max	ps	18,40
DQS/$\overline{\text{DQS}}$ low-impedance time from CK/$\overline{\text{CK}}$	tLZ(DQS)	tAC,min	tAC,max	tAC,min	tAC,max	ps	18,40
DQ low-impedance time from CK/$\overline{\text{CK}}$	tLZ(DQ)	2 x tAC,min	tAC,max	2 x tAC,min	tAC,max	ps	18,40
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	240	x	200	ps	13
CK half pulse width	tHP	Min(tCH(abs), tCL(abs))	x	Min(tCH(abs), tCL(abs))	x	ps	37
DQ hold skew factor	tQHS	x	340	x	300	ps	38
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	x	tHP - tQHS	x	ps	39
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK(avg)	19,41
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK(avg)	19,42

5 AC & DC operating conditions (cont'd)

Table 42 — Timing parameters by speed grade (DDR2-667 and DDR2-800) (cont'd)

(For information related to the entries in this table, refer to both the General Notes and the Specific Notes following this Table.)

Parameter	Symbol	DDR2-667		DDR2-800		Units[34]	Specific Notes
		min	max	min	max		
Activate to activate command period for 1KB page size products	tRRD	7.5	x	7.5	x	ns	4,32
Activate to activate command period for 2KB page size products	tRRD	10	x	10	x	ns	4,32
Four Activate Window for 1KB page size products	tFAW	37.5	x	35	x	ns	32
Four Activate Window for 2KB page size products	tFAW	50	x	45	x	ns	32
$\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ command delay	tCCD	2	x	2	x	nCK	
Write recovery time	tWR	15	x	15	x	ns	32
Auto precharge write recovery + precharge time	tDAL	WR + tnRP	x	WR + tnRP	x	nCK	33
Internal write to read command delay	tWTR	7.5	x	7.5	x	ns	24,32
Internal read to precharge command delay	tRTP	7.5	x	7.5	x	ns	3,32
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE	3	x	3	x	nCK	27
Exit self refresh to a non-read command	tXSNR	tRFC + 10	x	tRFC + 10	x	ns	32
Exit self refresh to a read command	tXSRD	200	x	200	x	nCK	
Exit precharge power down to any command	tXP	2	x	2	x	nCK	
Exit active power down to read command	tXARD	2	x	2	x	nCK	1
Exit active power down to read command (slow exit, lower power)	tXARDS	7 - AL	x	8 - AL	x	nCK	1,2
ODT turn-on delay	tAOND	2	2	2	2	nCK	16
ODT turn-on	tAON	tAC,min	tAC,max + 0.7	tAC,min	tAC,max + 0.7	ns	6,16,40
ODT turn-on (Power-Down mode)	tAONPD	tAC,min + 2	2 x tCK(avg) + tAC,max + 1	tAC,min + 2	2 x tCK(avg) + tAC,max + 1	ns	
ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	nCK	17,45
ODT turn-off	tAOF	tAC,min	tAC,max + 0.6	tAC,min	tAC,max + 0.6	ns	17,43,45
ODT turn-off (Power-Down mode)	tAOFPD	tAC,min + 2	2.5 x tCK(avg) + tAC,max + 1	tAC,min + 2	2.5 x tCK(avg) + tAC,max + 1	ns	
ODT to power down entry latency	tANPD	3	x	3	x	nCK	
ODT Power Down Exit Latency	tAXPD	8		8		nCK	
Mode register set command cycle time	tMRD	2	x	2	x	nCK	
MRS command to ODT update delay	tMOD	0	12	0	12	ns	32
OCD drive mode output delay	tOIT	0	12	0	12	ns	32
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS + tCK(avg) + tIH	x	tIS + tCK(avg) + tIH	x	ns	15

General notes, which may apply for all AC parameters

General Note 1 DDR2 SDRAM AC timing reference load

Figure 80 represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment or a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).

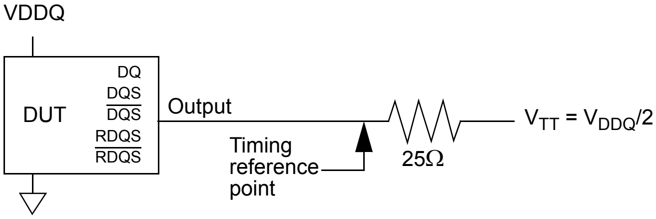


Figure 80 — AC timing reference load

The output timing reference voltage level for single ended signals is the crosspoint with VTT. The output timing reference voltage level for differential signals is the crosspoint of the true (e.g. DQS) and the complement (e.g. $\overline{\text{DQS}}$) signal.

General Note 2 Slew Rate Measurement Levels

a) Output slew rate for falling and rising edges is measured between VTT - 250 mV and VTT + 250 mV for single ended signals. For differential signals (e.g. DQS - $\overline{\text{DQS}}$) output slew rate is measured between DQS - $\overline{\text{DQS}}$ = - 500 mV and DQS - $\overline{\text{DQS}}$ = + 500 mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.

b) Input slew rate for single ended signals is measured from Vref(dc) to VIH(ac),min for rising edges and from Vref(dc) to VIL(ac),max for falling edges.
For differential signals (e.g. CK - $\overline{\text{CK}}$) slew rate for rising edges is measured from CK - $\overline{\text{CK}}$ = - 250 mV to CK - $\overline{\text{CK}}$ = + 500 mV (+ 250 mV to - 500 mV for falling edges).

c) VID is the magnitude of the difference between the input voltage on CK and the input voltage on $\overline{\text{CK}}$, or between DQS and $\overline{\text{DQS}}$ for differential strobe.

General Note 3 DDR2 SDRAM output slew rate test load

Output slew rate is characterized under the test conditions as shown in Figure 81.

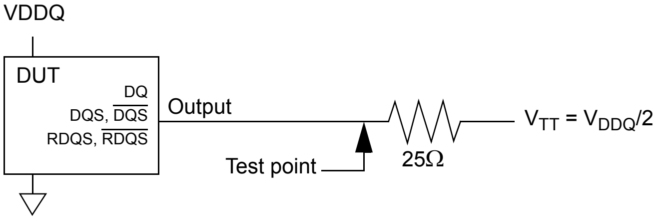


Figure 81 — Slew rate test load

General Note 4 Differential data strobe

DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS “Enable DQS” mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at VREF. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{\text{DQS}}$. This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled

5 AC & DC operating conditions (cont'd)

via the EMRS, the complementary pin, $\overline{\text{DQS}}$, must be tied externally to VSS through a 20 Ω to 10 kΩ resistor to insure proper operation.

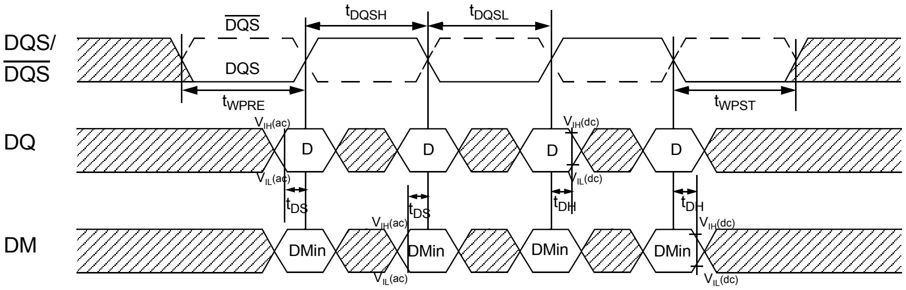


Figure 82 — Data Input (Write) Timing

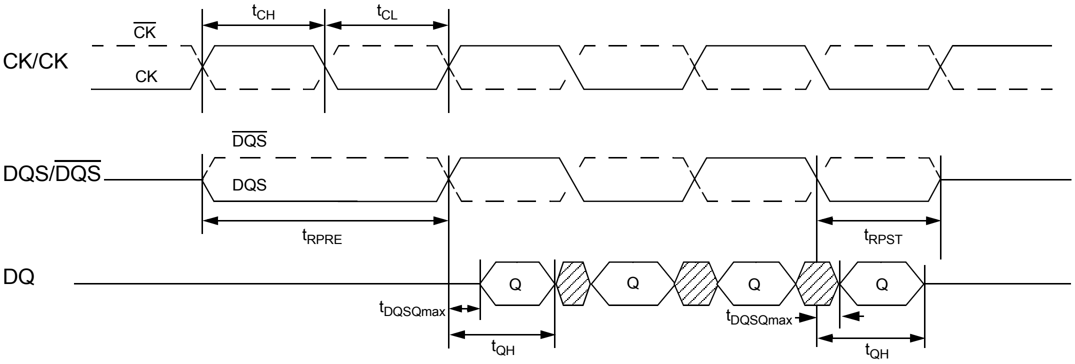


Figure 83 — Data output (read) timing

General Note 5 AC timings are for linear signal transitions. See Specific Notes on derating for other signal transitions.

General Note 6 All voltages are referenced to VSS.

General Note 7 These parameters guarantee device behavior, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.

General Note 8 Tests for AC timing, IDD, and electrical (AC and DC) characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.

Specific notes for dedicated AC parameters

Specific Note 1 User can choose which active power down exit timing to use via MRS (bit 12). tXARD is expected to be used for fast active power down exit timing. tXARDS is expected to be used for slow active power down exit timing where a lower power value is defined by each vendor data sheet.

Specific Note 2 AL = Additive Latency.

Specific Note 3 This is a minimum requirement. Minimum read to precharge timing is AL + BL / 2 provided that the tRTP and tRAS(min) have been satisfied.

Specific Note 4 A minimum of two clocks (2 x tCK or 2 x nCK) is required irrespective of operating frequency.

Specific Note 5 Timings are specified with command/address input slew rate of 1.0 V/ns. See Specific Notes on derating for other slew rate values.

Specific Note 6 Timings are specified with DQs, DM, and DQS's (DQS/RDQS in single ended mode) input slew rate of 1.0V/ns. See Specific Notes on derating for other slew rate values.

5 AC & DC operating conditions (cont'd)

Specific Note 7 Timings are specified with CK/$\overline{\text{CK}}$ differential slew rate of 2.0 V/ns. Timings are guaranteed for DQS signals with a differential slew rate of 2.0 V/ns in differential strobe mode and a slew rate of 1 V/ns in single ended mode. See Specific Notes on derating for other slew rate values.

Specific Note 8 Data setup and hold time derating.

Table 43 — DDR2-400/533 tDS/tDH derating with differential data strobe

ΔtDS, ΔtDH derating values for DDR2-400, DDR2-533 (All units in 'ps'; the note applies to the entire table)																			
		DQS,$\overline{\text{DQS}}$ Differential Slew Rate																	
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	2.0	125	45	125	45	125	45	-	-	-	-	-	-	-	-	-	-	-	-
	1.5	83	21	83	21	83	21	95	33	-	-	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	12	12	24	24	-	-	-	-	-	-	-	-
	0.9	-	-	-11	-14	-11	-14	1	-2	13	10	25	22	-	-	-	-	-	-
	0.8	-	-	-	-	-25	-31	-13	-19	-1	-7	11	5	23	17	-	-	-	-
	0.7	-	-	-	-	-	-	-31	-42	-19	-30	-7	-18	5	-6	17	6	-	-
	0.6	-	-	-	-	-	-	-	-	-43	-59	-31	-47	-19	-35	-7	-23	5	-11
	0.5	-	-	-	-	-	-	-	-	-	-	-74	-89	-62	-77	-50	-65	-38	-53
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-127	-140	-115	-128	-103	-116

Table 44 — DDR2-667/800 tDS/tDH derating with differential data strobe

ΔtDS, ΔtDH derating values for DDR2-667, DDR2-800 (All units in 'ps'; the note applies to the entire table)																			
		DQS,$\overline{\text{DQS}}$ Differential Slew Rate																	
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	2.0	100	45	100	45	100	45	-	-	-	-	-	-	-	-	-	-	-	-
	1.5	67	21	67	21	67	21	79	33	-	-	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	12	12	24	24	-	-	-	-	-	-	-	-
	0.9	-	-	-5	-14	-5	-14	7	-2	19	10	31	22	-	-	-	-	-	-
	0.8	-	-	-	-	-13	-31	-1	-19	11	-7	23	5	35	17	-	-	-	-
	0.7	-	-	-	-	-	-	-10	-42	2	-30	14	-18	26	-6	38	6	-	-
	0.6	-	-	-	-	-	-	-	-	-10	-59	2	-47	14	-35	26	-23	38	-11
	0.5	-	-	-	-	-	-	-	-	-	-	-24	-89	-12	-77	0	-65	12	-53
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-52	-140	-40	-128	-28	-116

Table 45 — DDR2-400/533 tDS1/tDH1 derating with single-ended data strobe

ΔtDS1, ΔtDH1 derating values for DDR2-400, DDR2-533 (All units in 'ps'; the note applies to the entire table)																			
		DQS Single-ended Slew Rate																	
		2.0 V/ns		1.5 V/ns		1.0 V/ns		0.9 V/ns		0.8 V/ns		0.7 V/ns		0.6 V/ns		0.5 V/ns		0.4 V/ns	
		ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1
DQ Slew rate V/ns	2.0	188	188	167	146	125	63	-	-	-	-	-	-	-	-	-	-	-	-
	1.5	146	167	125	125	83	42	81	43	-	-	-	-	-	-	-	-	-	-
	1.0	63	125	42	83	0	0	-2	1	-7	-13	-	-	-	-	-	-	-	-
	0.9	-	-	31	69	-11	-14	-13	-13	-18	-27	-29	-45	-	-	-	-	-	-
	0.8	-	-	-	-	-25	-31	-27	-30	-32	-44	-43	-62	-60	-86	-	-	-	-
	0.7	-	-	-	-	-	-	-45	-53	-50	-67	-61	-85	-78	-109	-108	-152	-	-
	0.6	-	-	-	-	-	-	-	-	-74	-96	-85	-114	-102	-138	-132	-181	-183	-246
	0.5	-	-	-	-	-	-	-	-	-	-	-128	-156	-145	-180	-175	-223	-226	-288
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-210	-243	-240	-286	-291	-351

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value to the ΔtDS and ΔtDH derating value respectively. Example: tDS (total setup time) = tDS(base) + ΔtDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of Vih(ac)min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of Vil(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value (See Figure 84 for differential data strobe and Figure 85 for single-ended data strobe.) If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 86 for differential data strobe and Figure 87 for single-ended data strobe)

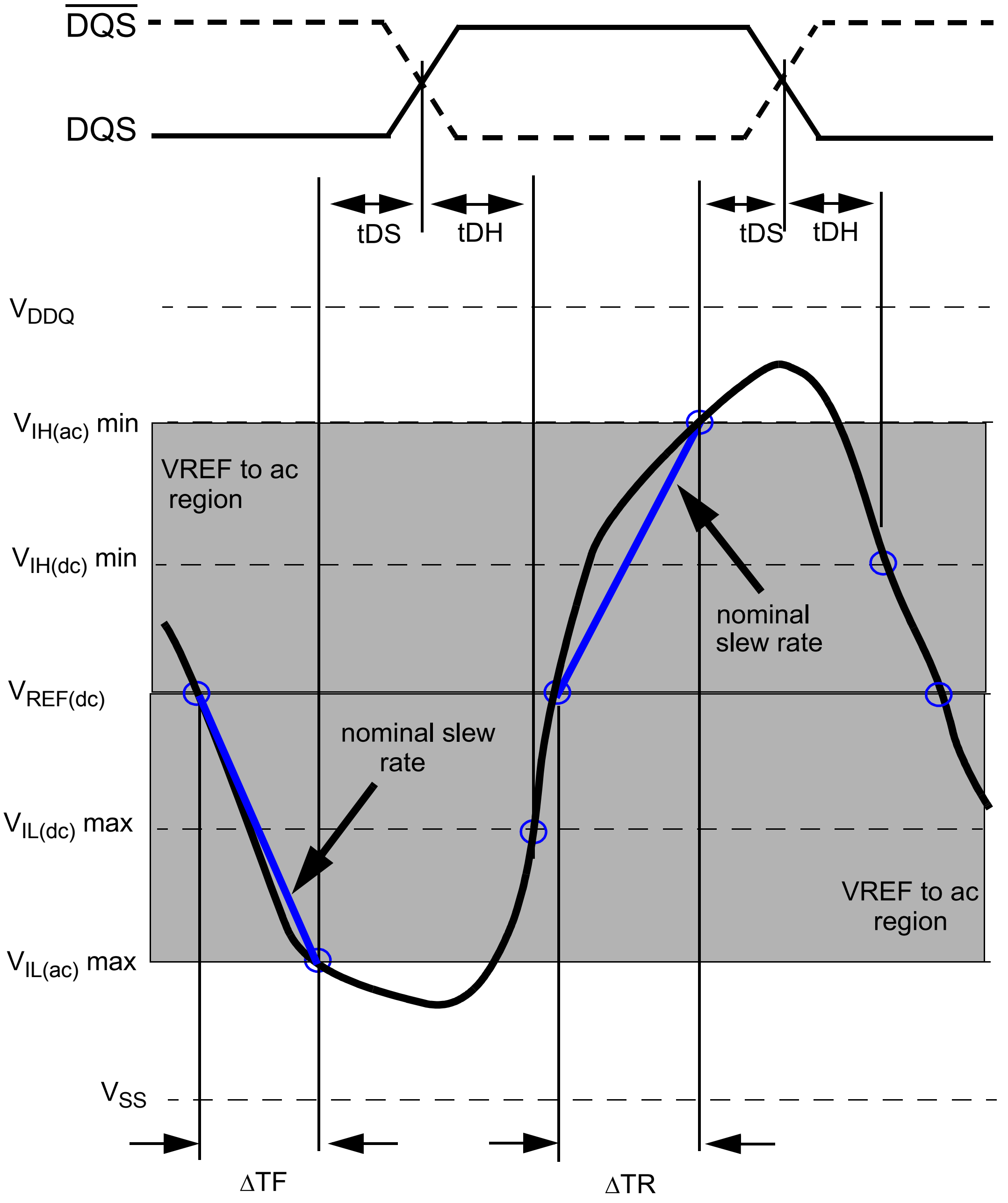
Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil(dc)max and the first crossing of $V_{REF(dc)}$. Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih(dc)min and the first crossing of $V_{REF(dc)}$. If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF(dc)}$ region', use nominal slew rate for derating value (see Figure 88 for differential data strobe and Figure 89 for single-ended data strobe) If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see Figure 90 for differential data strobe and Figure 91 for single-ended data strobe)

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL}$(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL}$(ac).

For slew rates in between the values listed in Tables 43, 44 and 45, the derating values may obtained by linear interpolation.

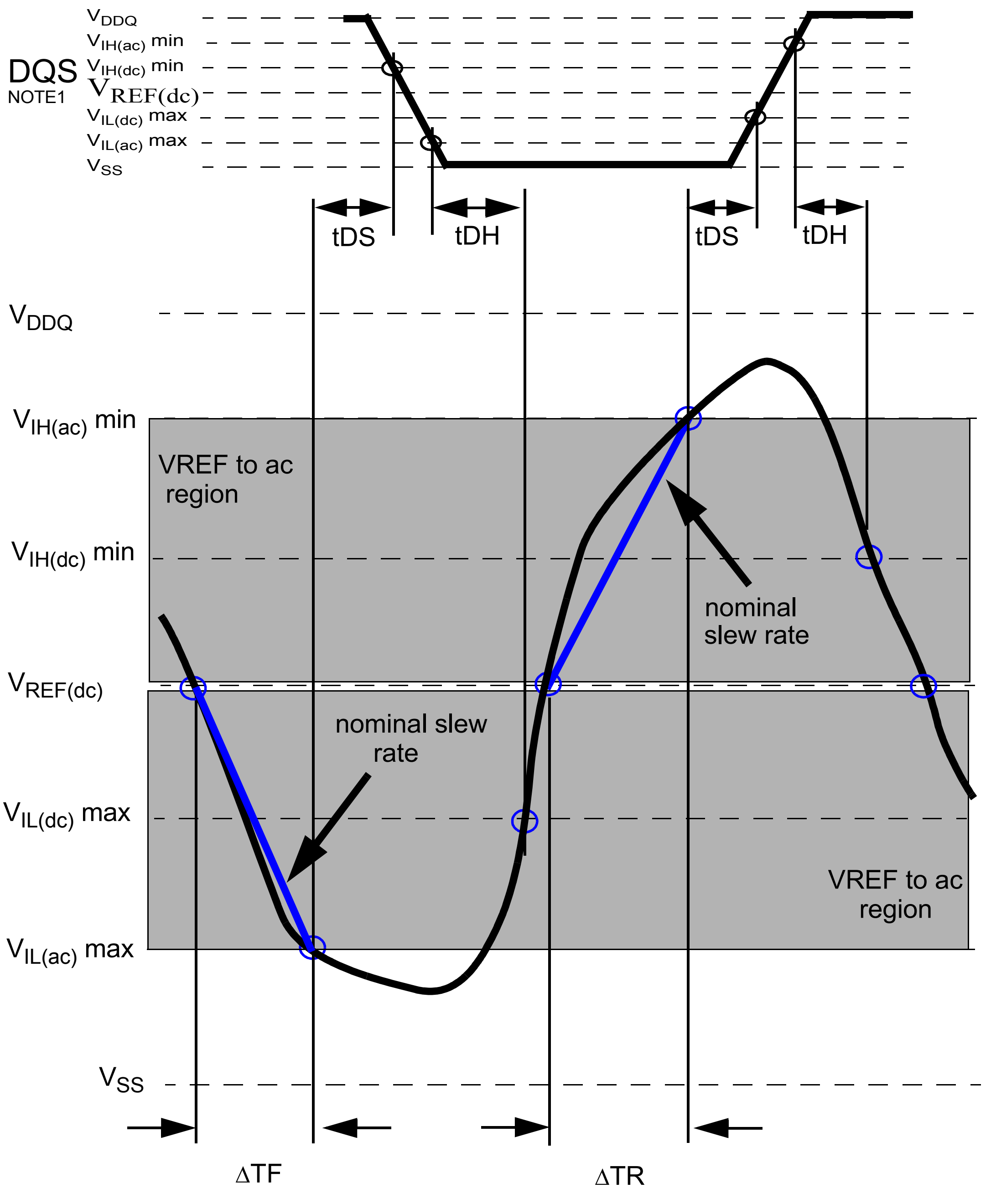
These values are typically not subject to production test. They are verified by design and characterization.

5 AC & DC operating conditions (cont'd)



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(dc)} - \text{Vil(ac)max}}{\Delta TF} \qquad \text{Setup Slew Rate Rising Signal} = \frac{\text{Vih(ac)min} - V_{REF(dc)}}{\Delta TR}$$

Figure 84 — Illustration of nominal slew rate for tDS (differential DQS, $\overline{\text{DQS}}$)



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(dc)} - Vil(ac)max}{\Delta TF} \qquad \text{Setup Slew Rate Rising Signal} = \frac{Vih(ac)min - V_{REF(dc)}}{\Delta TR}$$

NOTE 1 DQS signal must be monotonic between Vil(dc)max and Vih(dc)min.

Figure 85 — Illustration of nominal slew rate for tDS (single-ended DQS)

5 AC & DC operating conditions (cont'd)

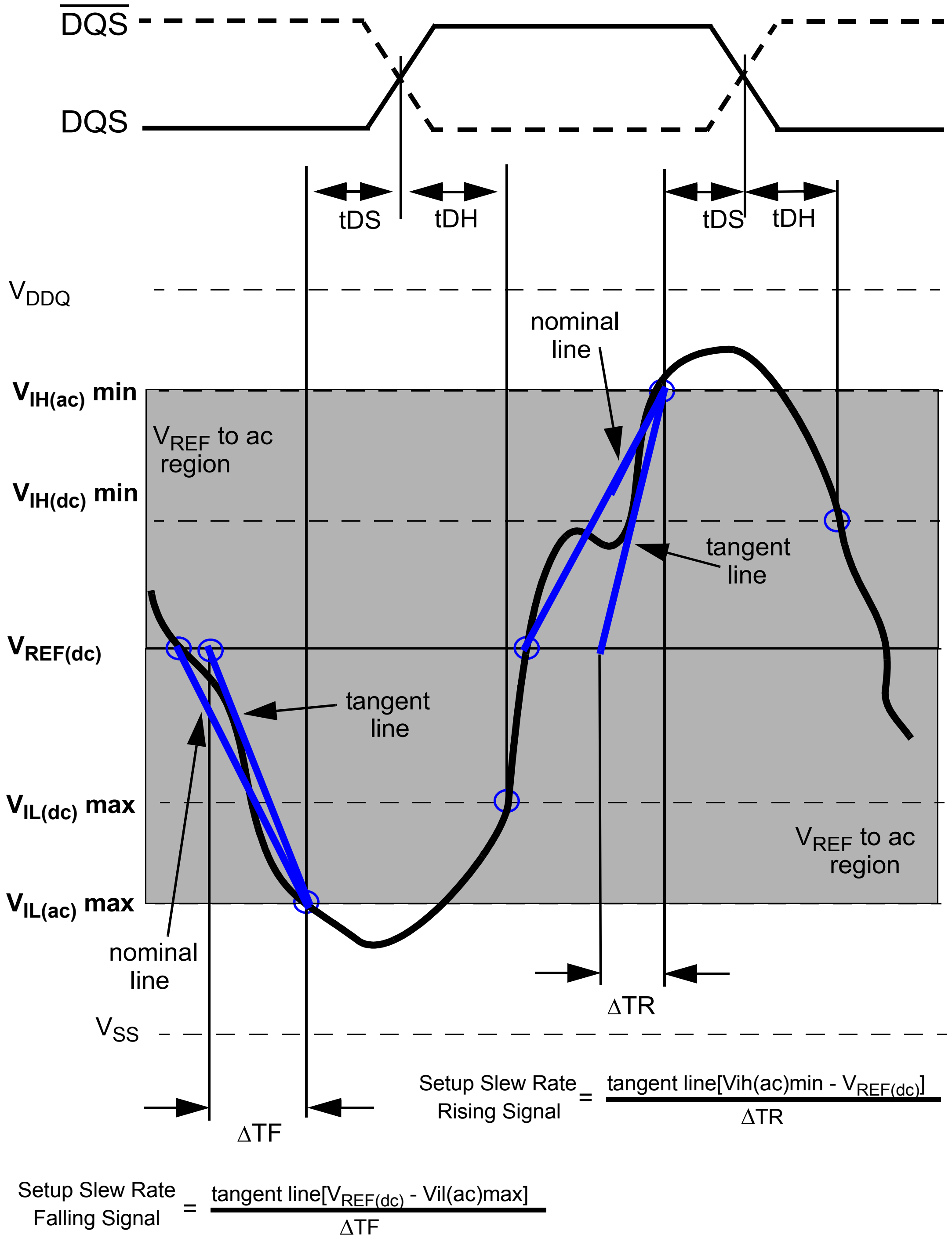
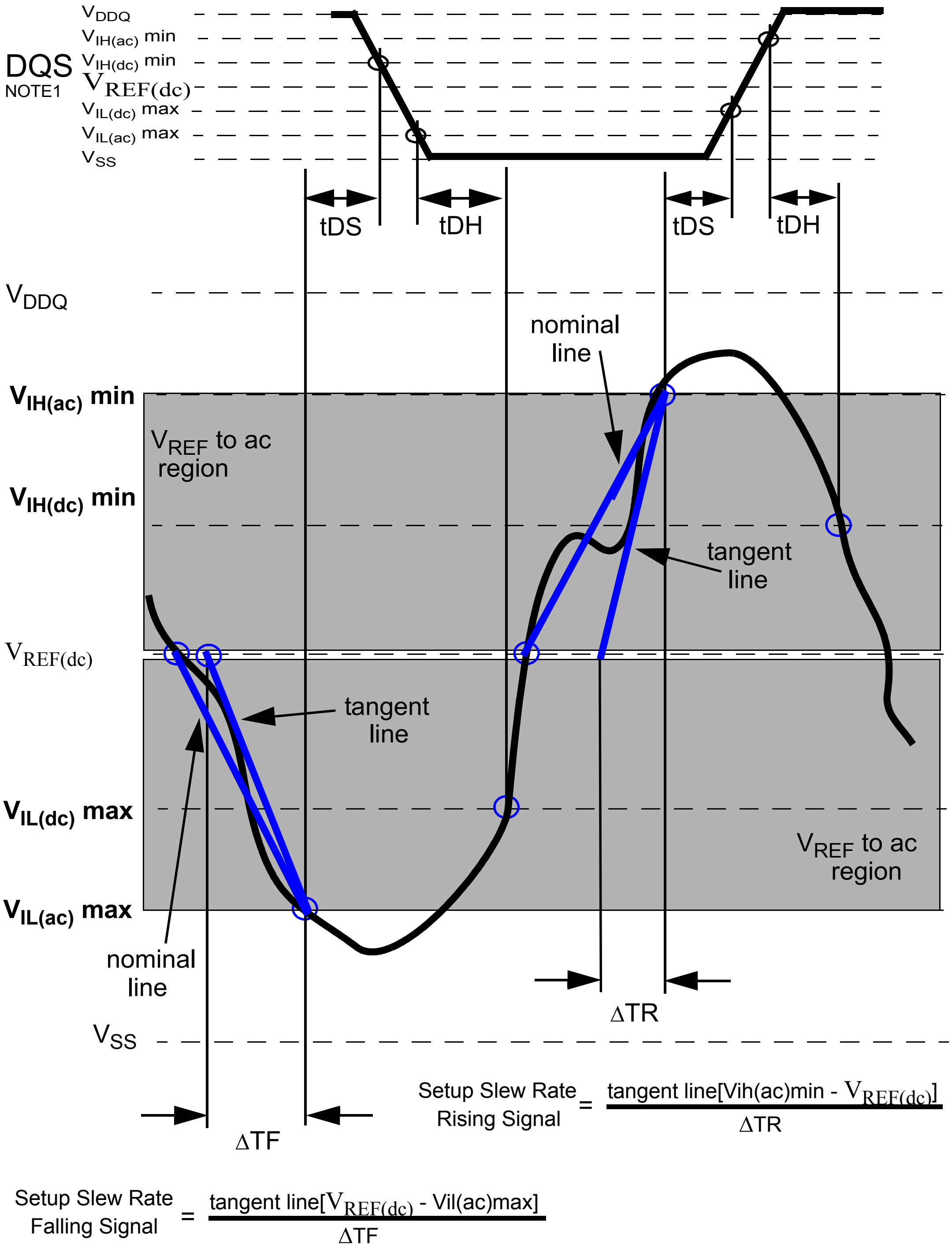


Figure 86 — Illustration of tangent line for tDS (differential DQS, $\overline{\text{DQS}}$)

5 AC & DC operating conditions (cont'd)



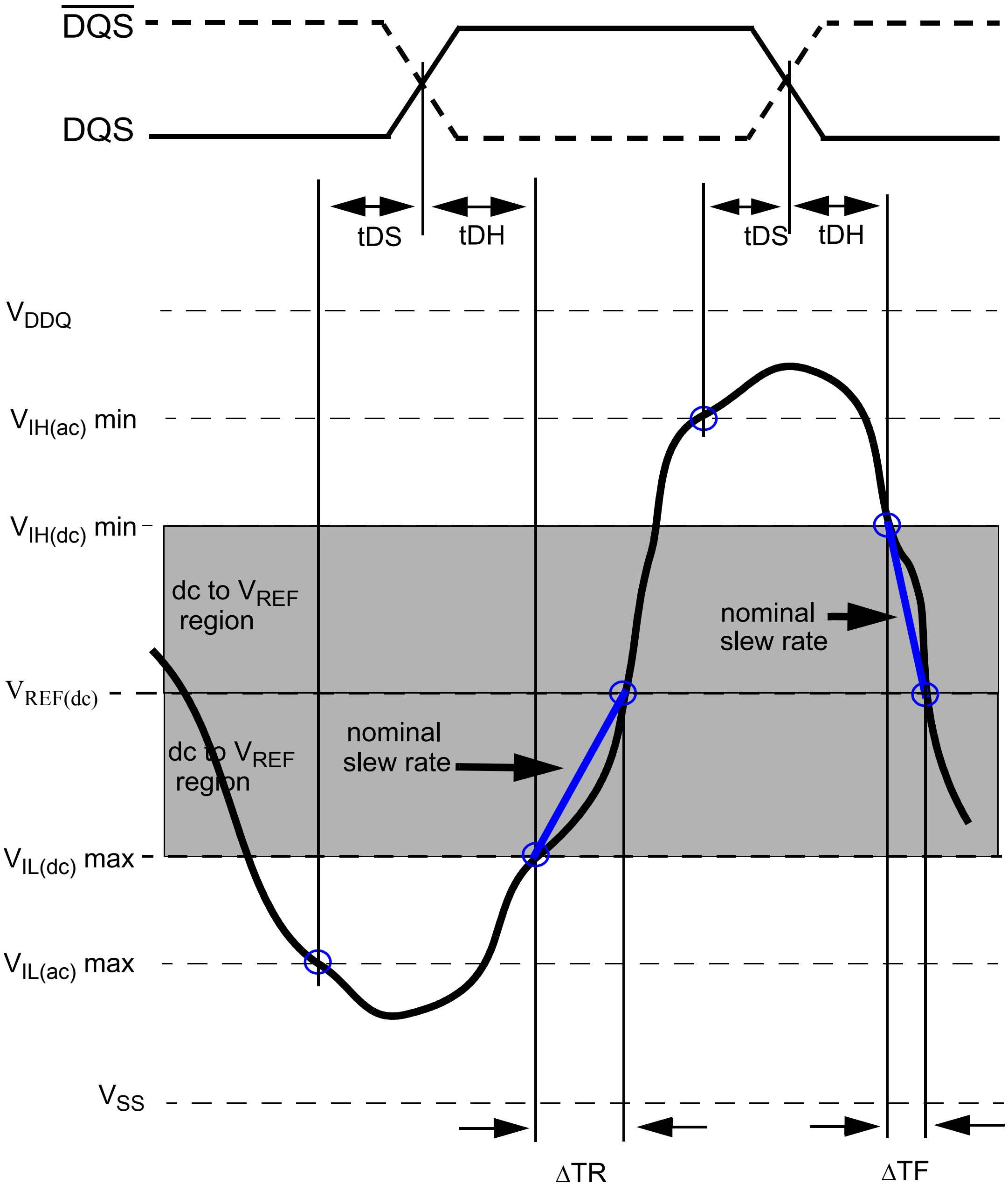
$$\text{Setup Slew Rate Rising Signal} = \frac{\text{tangent line}[V_{ih(ac)min} - V_{REF(dc)}]}{\Delta TR}$$

$$\text{Setup Slew Rate Falling Signal} = \frac{\text{tangent line}[V_{REF(dc)} - V_{il(ac)max}]}{\Delta TF}$$

NOTE DQS signal must be monotonic between Vil(dc)max and Vih(dc)min.

Figure 87 — Illustration of tangent line for tDS (single-ended DQS)

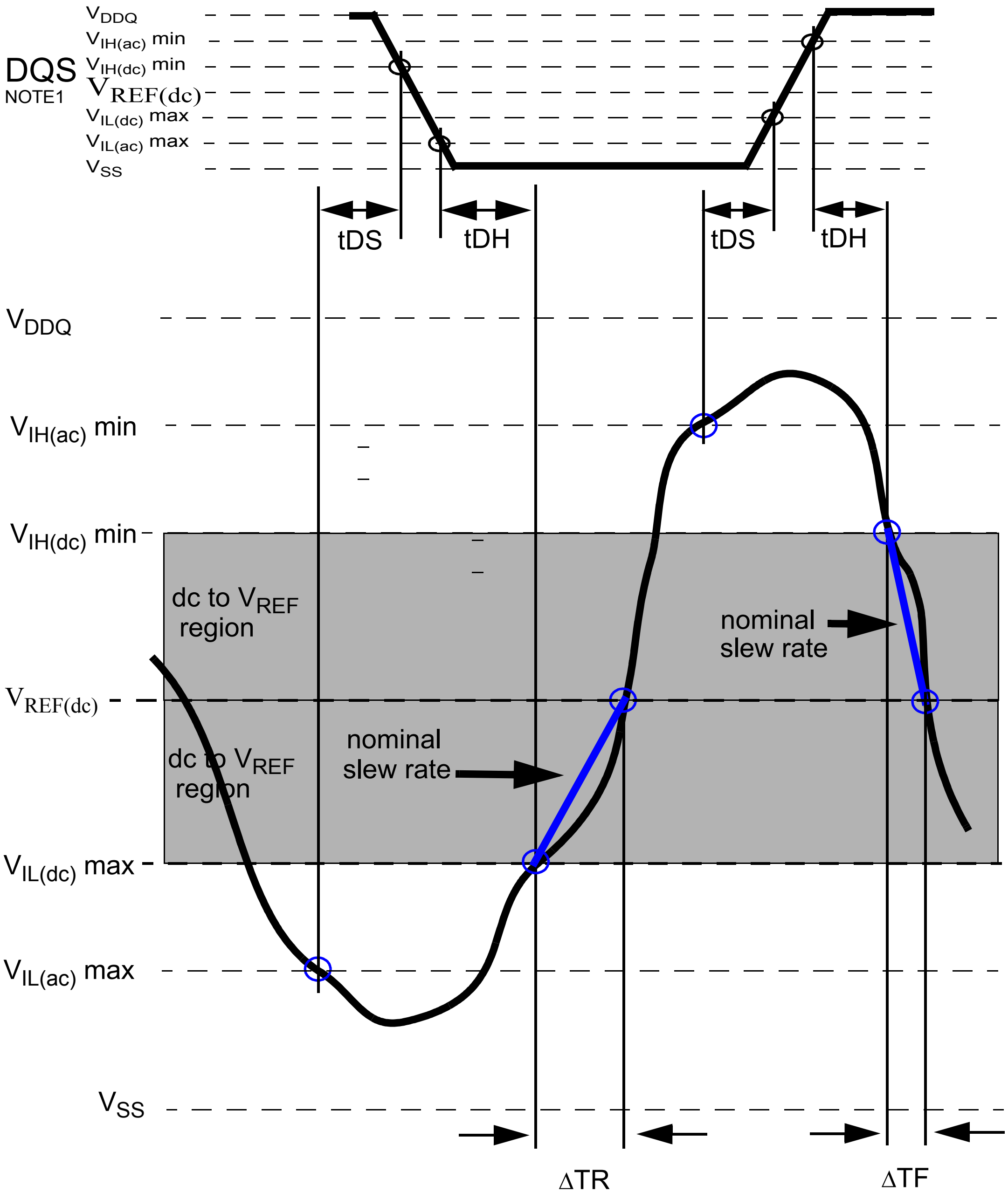
5 AC & DC operating conditions (cont'd)



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(dc)} - \text{Vil(dc)max}}{\Delta TR} \qquad \text{Hold Slew Rate Falling Signal} = \frac{\text{Vih(dc)min} - V_{REF(dc)}}{\Delta TF}$$

Figure 88 — Illustration of nominal slew rate for tDH (differential DQS, $\overline{\text{DQS}}$)

5 AC & DC operating conditions (cont’d)



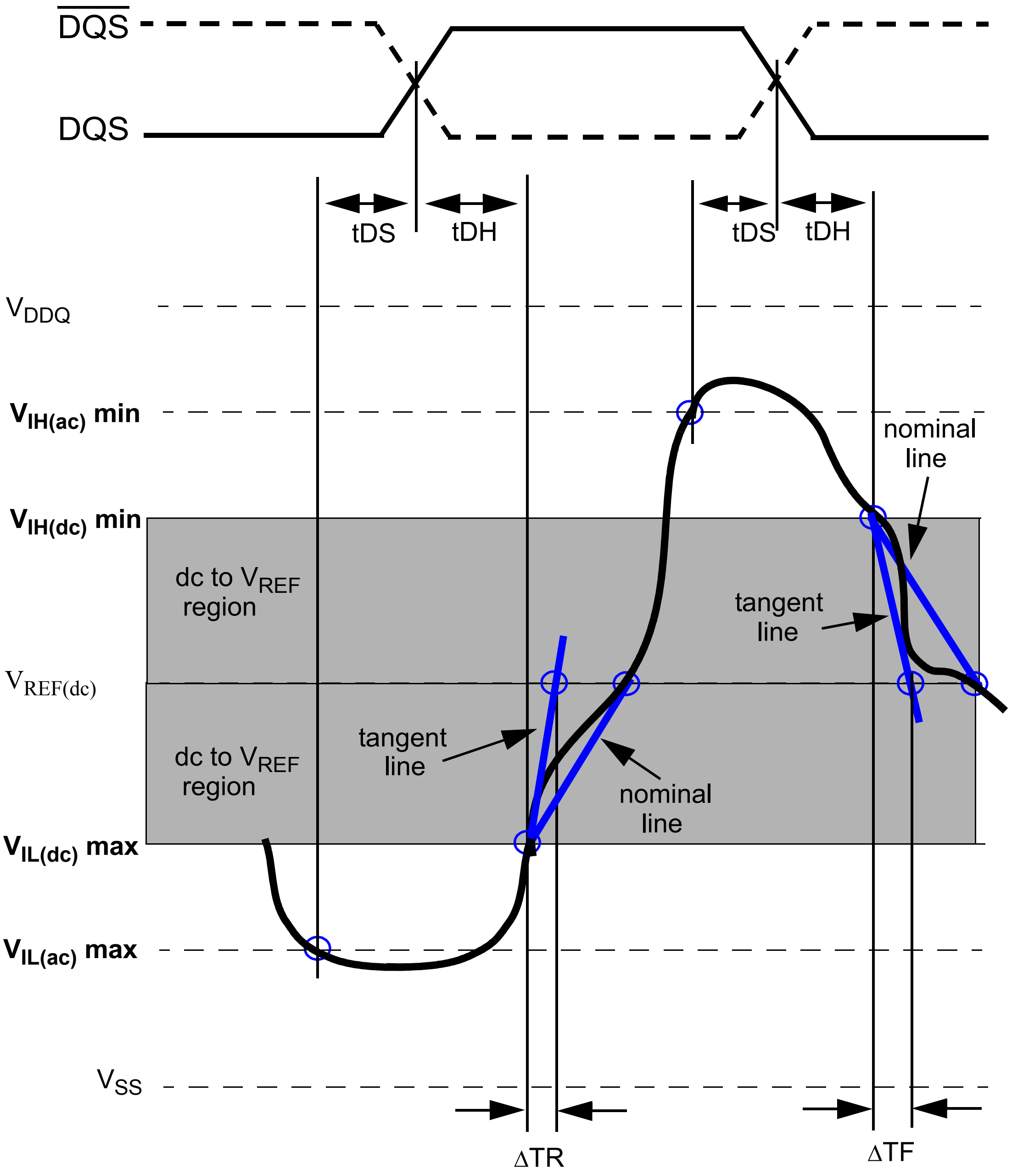
$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(dc)} - Vil(dc)max}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{Vih(dc)min - V_{REF(dc)}}{\Delta TF}$$

NOTE DQS signal must be monotonic between Vil(dc)max and Vih(dc)min.

Figure 89 — Illustration of nominal slew rate for tDH (single-ended DQS)

5 AC & DC operating conditions (cont'd)

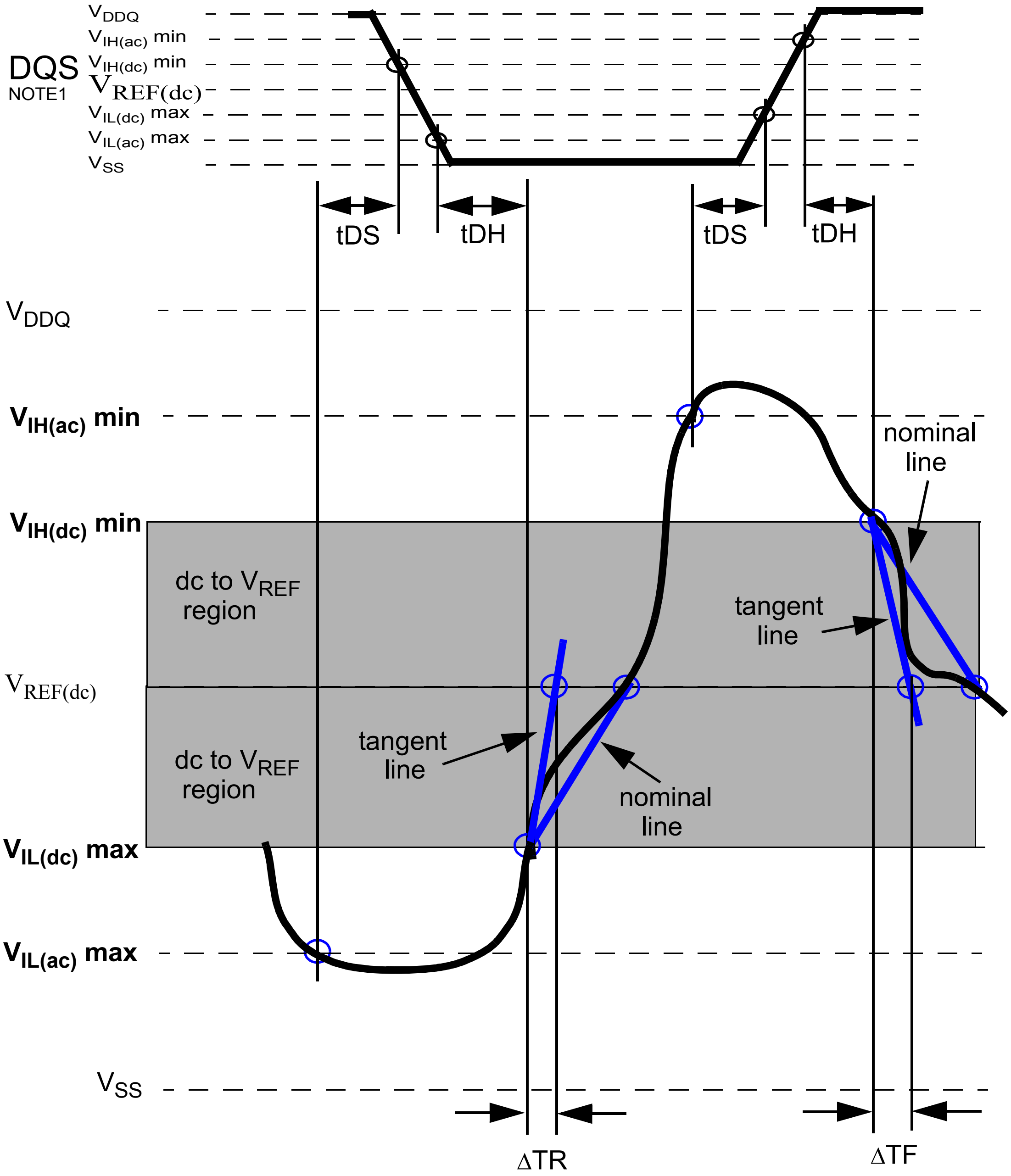


$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line } [\, V_{REF(dc)} - \text{Vil(dc)max} \,]}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line } [\, \text{Vih(dc)min} - V_{REF(dc)} \,]}{\Delta TF}$$

Figure 90 — Illustration tangent line for tDH (differential DQS, $\overline{\text{DQS}}$)

5 AC & DC operating conditions (cont'd)



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line } [V_{REF(dc)} - \text{Vil(dc)max}]}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line } [\text{Vih(dc)min} - V_{REF(dc)}]}{\Delta TF}$$

NOTE DQS signal must be monotonic between Vil(dc)max and Vih(dc)min.

Figure 91 — Illustration tangent line for tDH (single-ended DQS)

5 AC & DC operating conditions (cont'd)

Specific Note 9 tIS and tIH (input setup and hold) derating

Table 46 — Derating values for DDR2-400, DDR2-533.

tIS, tIH Derating Values for DDR2-400, DDR2-533									
		CK,$\overline{\text{CK}}$ Differential Slew Rate							
		2.0 V/ns		1.5 V/ns		1.0 V/ns			
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	Units	Notes
Command/Address Slew rate (V/ns)	4.0	+187	+94	+217	+124	+247	+154	ps	1
	3.5	+179	+89	+209	+119	+239	+149	ps	1
	3.0	+167	+83	+197	+113	+227	+143	ps	1
	2.5	+150	+75	+180	+105	+210	+135	ps	1
	2.0	+125	+45	+155	+75	+185	+105	ps	1
	1.5	+83	+21	+113	+51	+143	+81	ps	1
	1.0	0	0	+30	+30	+60	60	ps	1
	0.9	-11	-14	+19	+16	+49	+46	ps	1
	0.8	-25	-31	+5	-1	+35	+29	ps	1
	0.7	-43	-54	-13	-24	+17	+6	ps	1
	0.6	-67	-83	-37	-53	-7	-23	ps	1
	0.5	-110	-125	-80	-95	-50	-65	ps	1
	0.4	-175	-188	-145	-158	-115	-128	ps	1
	0.3	-285	-292	-255	-262	-225	-232	ps	1
	0.25	-350	-375	-320	-345	-290	-315	ps	1
	0.2	-525	-500	-495	-470	-465	-440	ps	1
	0.15	-800	-708	-770	-678	-740	-648	ps	1
	0.1	-1450	-1125	-1420	-1095	-1390	-1065	ps	1

5 AC & DC operating conditions (cont'd)

Table 47 — Derating values for DDR2-667, DDR2-800

ΔtIS and ΔtIH Derating Values for DDR2-667, DDR2-800									
		CK,$\overline{\text{CK}}$ Differential Slew Rate							
		2.0 V/ns		1.5 V/ns		1.0 V/ns			
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	Units	Notes
Command/Address Slew rate (V/ns)	4.0	+150	+94	+180	+124	+210	+154	ps	1
	3.5	+143	+89	+173	+119	+203	+149	ps	1
	3.0	+133	+83	+163	+113	+193	+143	ps	1
	2.5	+120	+75	+150	+105	+180	+135	ps	1
	2.0	+100	+45	+130	+75	+160	+105	ps	1
	1.5	+67	+21	+97	+51	+127	+81	ps	1
	1.0	0	0	+30	+30	+60	+60	ps	1
	0.9	-5	-14	+25	+16	+55	+46	ps	1
	0.8	-13	-31	+17	-1	+47	+29	ps	1
	0.7	-22	-54	+8	-24	+38	+6	ps	1
	0.6	-34	-83	-4	-53	+26	-23	ps	1
	0.5	-60	-125	-30	-95	0	-65	ps	1
	0.4	-100	-188	-70	-158	-40	-128	ps	1
	0.3	-168	-292	-138	-262	-108	-232	ps	1
	0.25	-200	-375	-170	-345	-140	-315	ps	1
	0.2	-325	-500	-295	-470	-265	-440	ps	1
	0.15	-517	-708	-487	-678	-457	-648	ps	1
	0.1	-1000	-1125	-970	-1095	-940	-1065	ps	1

For all input signals the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) value to the ΔtIS and ΔtIH derating value respectively. Example: tIS (total setup time) = tIS(base) + ΔtIS

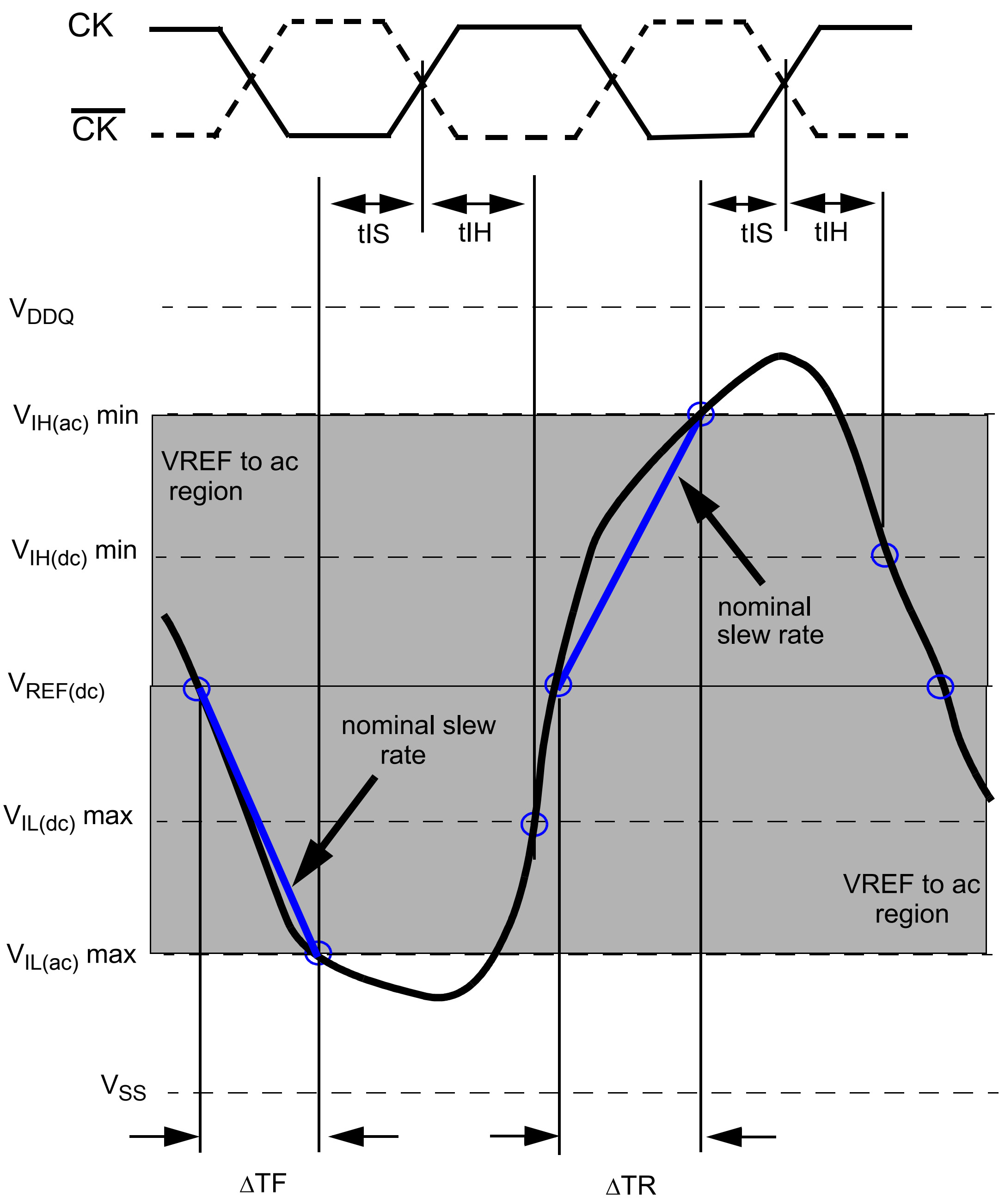
Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of Vih(ac)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of Vil(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value (see Figure 92). If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 93).

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil(dc)max and the first crossing of $V_{REF(dc)}$. Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih(dc)min and the first crossing of $V_{REF(dc)}$. If the actual signal is always later than the nominal slew rate line between shaded 'dc to $V_{REF(dc)}$ region', use nominal slew rate for derating value (see Figure 94). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see Figure 95).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL}$(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL}$(ac).

For slew rates in between the values listed in Tables 46 and 47, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(dc)} - \text{Vil(ac)max}}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{\text{Vih(ac)min} - V_{REF(dc)}}{\Delta TR}$$

Figure 92 — Illustration of nominal slew rate for tIS

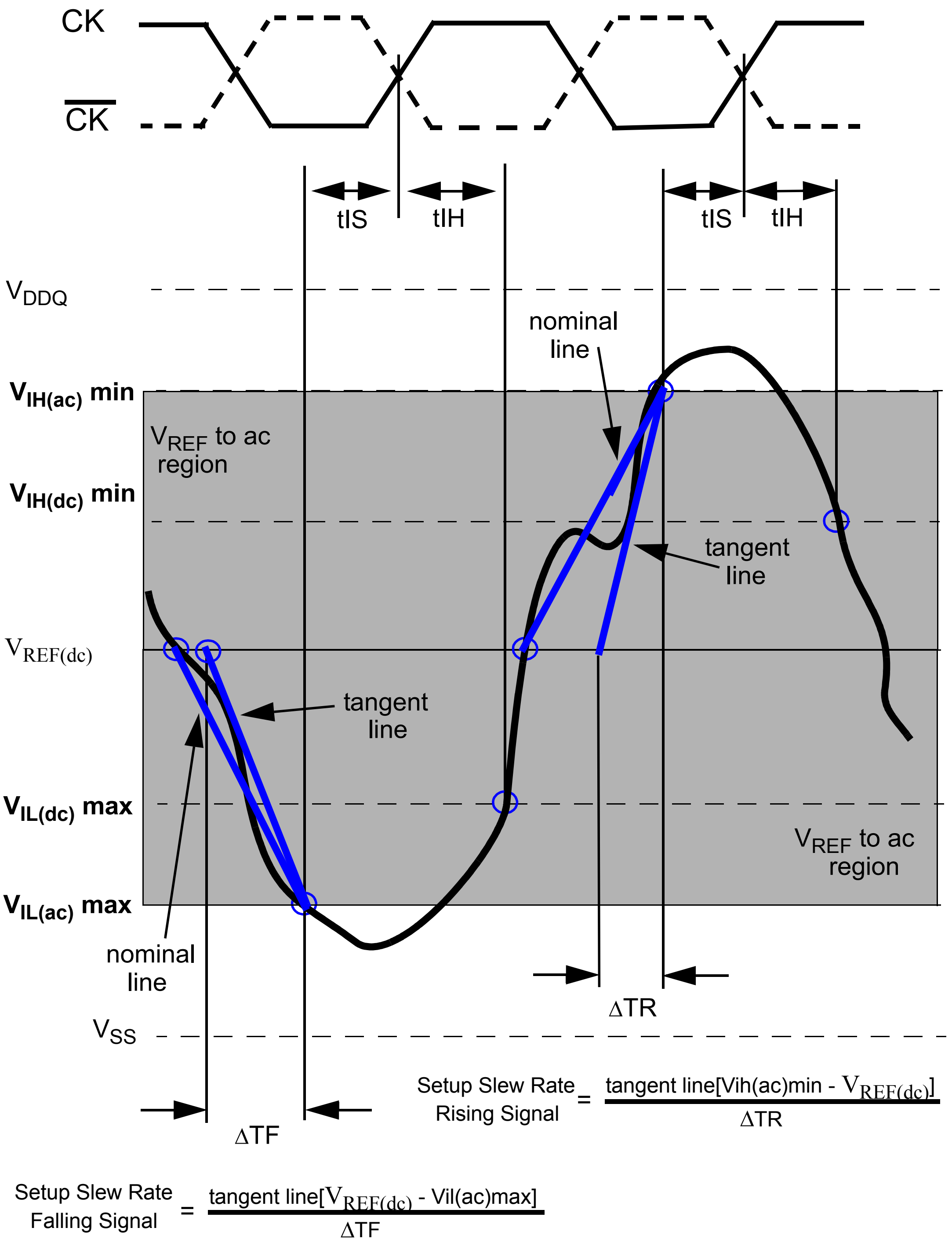
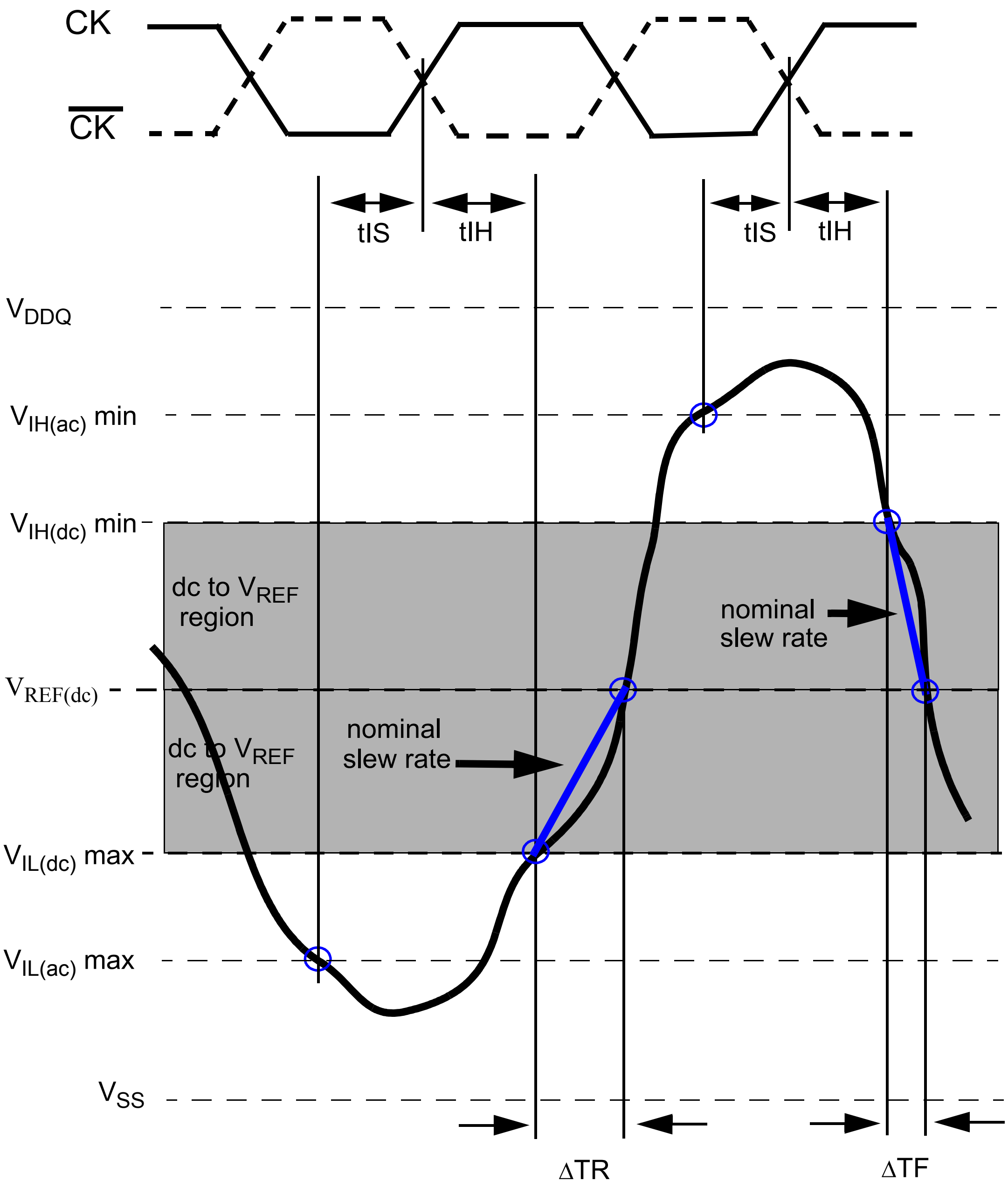


Figure 93 — Illustration of tangent line for tIS

5 AC & DC operating conditions (cont'd)

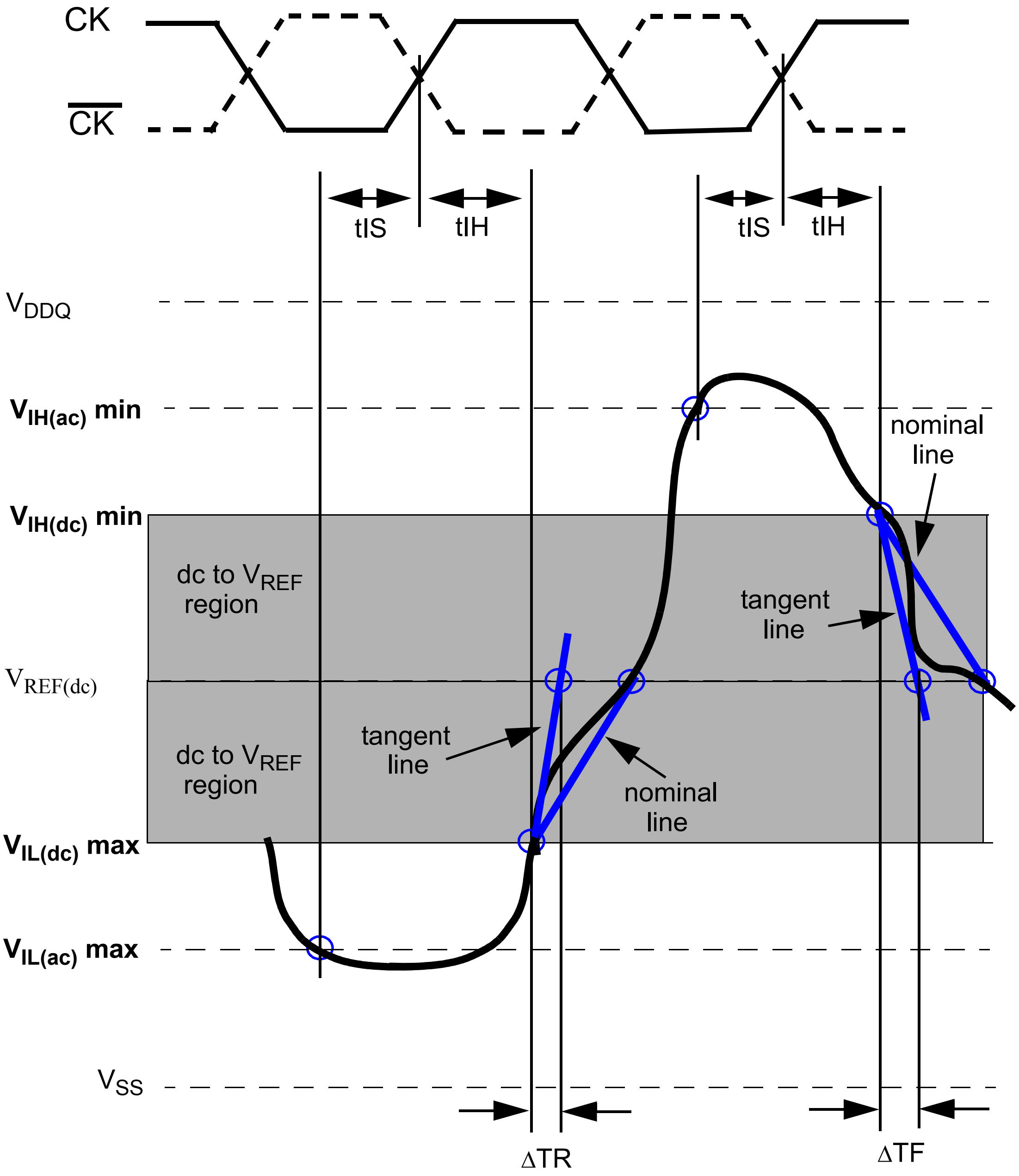


Hold Slew Rate Rising Signal $= \dfrac{V_{REF(dc)} - Vil(dc)max}{\Delta TR}$

Hold Slew Rate Falling Signal $= \dfrac{Vih(dc)min - V_{REF(dc)}}{\Delta TF}$

Figure 94 — Illustration of nominal slew rate for tIH

5 AC & DC operating conditions (cont'd)



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line } [V_{REF(dc)} - V_{il(dc)max}]}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line } [V_{ih(dc)min} - V_{REF(dc)}]}{\Delta TF}$$

Figure 95 — Illustration tangent line for tIH

5 AC & DC operating conditions (cont'd)

Specific Note 10 The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

Specific Note 11 MIN (tCL, tCH) refers to the smaller of the actual clock LOW time and the actual clock HIGH time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH). For example, tCL and tCH are = 50% of the period, less the half period jitter (tJIT(HP)) of the clock source, and less the half period jitter due to crosstalk (tJIT(crosstalk)) into the clock traces.

Specific Note 12 tQH = tHP – tQHS, where:

tHP = minimum half clock period for any given cycle and is defined by clock HIGH or clock LOW (tCH, tCL).
tQHS accounts for:

1) The pulse duration distortion of on-chip clock circuits; and
2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.

Specific Note 13 tDQSQ: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output slew rate mismatch between DQS / $\overline{\text{DQS}}$ and associated DQ in any given cycle.

Specific Note 14 tDAL = WR + RU{ tRP[ns] / tCK[ns] }, where RU stands for round up.

WR refers to the tWR parameter stored in the MRS. For tRP, if the result of the division is not already an integer, round up to the next highest integer. tCK refers to the application clock period.

Example: For DDR533 at tCK = 3.75ns with WR programmed to 4 clocks.

tDAL = 4 + (15 ns / 3.75 ns) clocks = 4 + (4) clocks = 8 clocks.

Specific Note 15 The clock frequency is allowed to change during self–refresh mode or precharge power-down mode. In case of clock frequency change during precharge power-down, a specific procedure is required as described in section 2.13.

Specific Note 16 ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from tAOND, which is interpreted differently per speed bin. For DDR2-400/533, tAOND is 10 ns (= 2 x 5 ns) after the clock edge that registered a first ODT HIGH if tCK = 5 ns. For DDR2-667/800, tAOND is 2 clock cycles after the clock edge that registered a first ODT HIGH counting the actual input clock edges.

Specific Note 17 ODT turn off time min is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from tAOFD, which is interpreted differently per speed bin. For DDR2-400/533, tAOFD is 12.5 ns (= 2.5 x 5 ns) after the clock edge that registered a first ODT LOW if tCK = 5 ns. For DDR2-667/800, if tCK(avg) = 3 ns is assumed, tAOFD is 1.5 ns (= 0.5 x 3 ns) after the second trailing clock edge counting from the clock edge that registered a first ODT LOW and by counting the actual input clock edges.

Specific Note 18 tHZ and tLZ transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (tHZ), or begins driving (tLZ) . Figure 96 shows a method to calculate the point when device is no longer driving (tHZ), or begins driving (tLZ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. tLZ(DQ) refers to tLZ of the DQ's and tLZ(DQS) refers to tLZ of the (U/L/R)DQS and $\overline{\text{(U/L/R)DQS}}$ each treated as single-ended signal.

Specific Note 19 tRPST end point and tRPRE begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (tRPST), or begins driving (tRPRE). Figure 96 shows a method to calculate these points when the device is no longer driving (tRPST), or begins driving (tRPRE) by measuring the

5 AC & DC operating conditions (cont'd)

signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

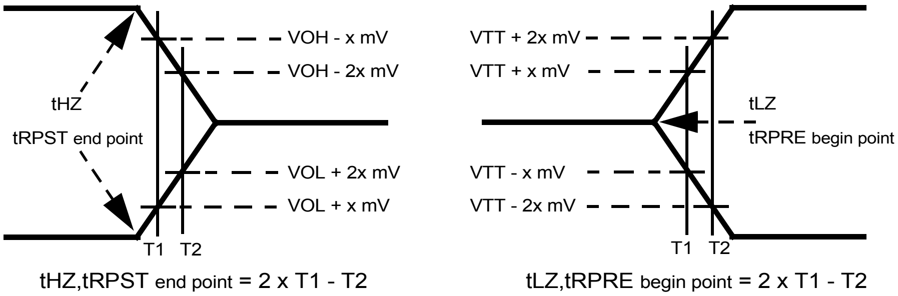


Figure 96 — Method for calculating transitions and endpoints

Specific Note 20 Input waveform timing tDS with differential data strobe enabled MR[bit10]=0, is referenced from the input signal crossing at the $V_{IH(ac)}$ level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the $V_{IL(ac)}$ level to the differential data strobe crosspoint for a falling signal applied to the device under test. DQS, $\overline{\text{DQS}}$ signals must be monotonic between Vil(dc)max and Vih(dc)min. See Figure 97.

Specific Note 21 Input waveform timing tDH with differential data strobe enabled MR[bit10]=0, is referenced from the differential data strobe crosspoint to the input signal crossing at the $V_{IH(dc)}$ level for a falling signal and from the differential data strobe crosspoint to the input signal crossing at the $V_{IL(dc)}$ level for a rising signal applied to the device under test. DQS, $\overline{\text{DQS}}$ signals must be monotonic between Vil(dc)max and Vih(dc)min. See Figure 97.

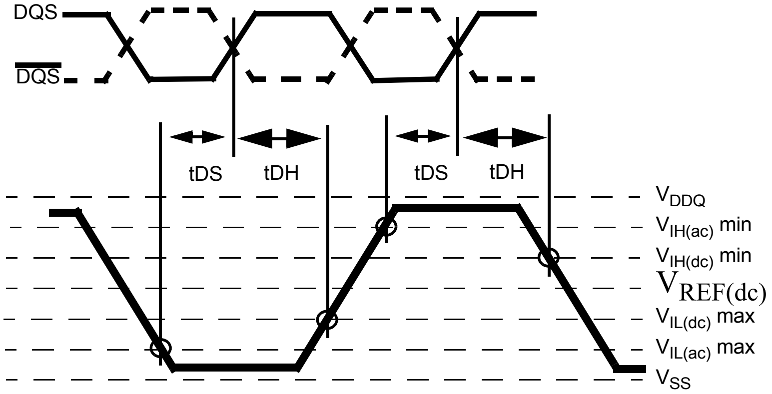


Figure 97 — Differential input waveform timing – tDS and tDH

Specific Note 22 Input waveform timing is referenced from the input signal crossing at the $V_{IH(ac)}$ level for a rising signal and $V_{IL(ac)}$ for a falling signal applied to the device under test. See Figure 98.

Specific Note 23 Input waveform timing is referenced from the input signal crossing at the $V_{IL(dc)}$ level for a rising signal and $V_{IH(dc)}$ for a falling signal applied to the device under test. See Figure 98.

5 AC & DC operating conditions (cont'd)

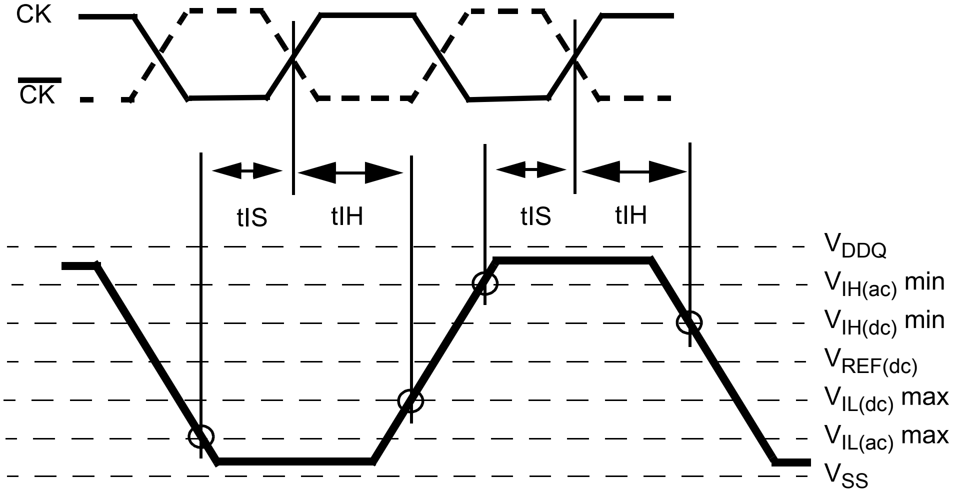


Figure 98 — Differential input waveform timing – tIS and tIH

Specific Note 24 tWTR is at lease two clocks (2 x tCK or 2 x nCK) independent of operation frequency.

Specific Note 25 Input waveform timing with single-ended data strobe enabled MR[bit10] = 1, is referenced from the input signal crossing at the VIH(ac) level to the single-ended data strobe crossing VIH/L(dc) at the start of its transition for a rising signal, and from the input signal crossing at the VIL(ac) level to the single-ended data strobe crossing VIH/L(dc) at the start of its transition for a falling signal applied to the device under test. The DQS signal must be monotonic between Vil(dc)max and Vih(dc)min.

Specific Note 26 Input waveform timing with single-ended data strobe enabled MR[bit10] = 1, is referenced from the input signal crossing at the VIH(dc) level to the single-ended data strobe crossing VIH/L(ac) at the end of its transition for a rising signal, and from the input signal crossing at the VIL(dc) level to the single-ended data strobe crossing VIH/L(ac) at the end of its transition for a falling signal applied to the device under test. The DQS signal must be monotonic between Vil(dc)max and Vih(dc)min.

Specific Note 27 tCKEmin of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + 2 x tCK + tIH.

Specific Note 28 If tDS or tDH is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.

Specific Note 29 These parameters are measured from a command/address signal (CKE, $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK/$\overline{\text{CK}}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

Specific Note 30 These parameters are measured from a data strobe signal ((L/U/R)DQS/$\overline{\text{DQS}}$) crossing to its respective clock signal (CK/$\overline{\text{CK}}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

Specific Note 31 These parameters are measured from a data signal ((L/U)DM, (L/U)DQ0, (L/U)DQ1, etc.) transition edge to its respective data strobe signal ((L/U/R)DQS/$\overline{\text{DQS}}$) crossing.

Specific Note 32 For these parameters, the DDR2 SDRAM device is characterized and verified to support tnPARAM = RU{tPARAM / tCK(avg)}, which is in clock cycles, assuming all input clock jitter specifications are satisfied.
For example, the device will support tnRP = RU{tRP / tCK(avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR2-667 5-5-5, of which tRP = 15ns, the device will support tnRP =

5 AC & DC operating conditions (cont’d)

RU{tRP / tCK(avg)} = 5, i.e. as long as the input clock jitter specifications are met, Precharge command at Tm and Active command at Tm+5 is valid even if (Tm+5 - Tm) is less than 15ns due to input clock jitter.

Specific Note 33 tDAL [nCK] = WR [nCK] + tnRP [nCK] = WR + RU {tRP [ps] / tCK(avg) [ps] }, where WR is the value programmed in the mode register set.

Specific Note 34 New units, ‘tCK(avg)’ and ‘nCK’, are introduced in DDR2-667 and DDR2-800.
Unit ‘tCK(avg)’ represents the actual tCK(avg) of the input clock under operation.
Unit ‘nCK’ represents one clock cycle of the input clock, counting the actual clock edges.
Note that in DDR2-400 and DDR2-533, ‘tCK’ is used for both concepts.
ex) tXP = 2 [nCK] means; if Power Down exit is registered at Tm, an Active command may be registered at Tm+2, even if (Tm+2 - Tm) is 2 x tCK(avg) + tERR(2per),min.

Specific Note 35 Input clock jitter spec parameter. These parameters and the ones in the table below are referred to as 'input clock jitter spec parameters' and these parameters apply to DDR2-667 and DDR2-800 only. The jitter specified is a random jitter meeting a Gaussian distribution.

Parameter	Symbol	DDR2-667		DDR2-800		Units	Notes
		min	max	min	max		
Clock period jitter	tJIT(per)	- 125	125	-100	100	ps	35
Clock period jitter during DLL locking period	tJIT(per,lck)	- 100	100	-80	80	ps	35
Cycle to cycle clock period jitter	tJIT(cc)	- 250	250	-200	200	ps	35
Cycle to cycle clock period jitter during DLL locking period	tJIT(cc,lck)	- 200	200	-160	160	ps	35
Cumulative error across 2 cycles	tERR(2per)	- 175	175	-150	150	ps	35
Cumulative error across 3 cycles	tERR(3per)	- 225	225	-175	175	ps	35
Cumulative error across 4 cycles	tERR(4per)	- 250	250	-200	200	ps	35
Cumulative error across 5 cycles	tERR(5per)	- 250	250	-200	200	ps	35
Cumulative error across n cycles, n = 6 ... 10, inclusive	tERR(6-10per)	-350	350	-300	300	ps	35
Cumulative error across n cycles, n = 11 ... 50, inclusive	tERR(11-50per)	-450	450	-450	450	ps	35
Duty cycle jitter	tJIT(duty)	- 125	125	-100	100	ps	35

Definitions:

- tCK(avg)

  tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window.

$$tCK(avg) = \left(\sum_{j=1}^{N} tCK_j \right) / N$$

$$where \qquad N = 200$$

- tCH(avg) and tCL(avg)

  tCH(avg) is defined as the average HIGH pulse width, as calculated across any consecutive 200 HIGH pulses.

5 AC & DC operating conditions (cont'd)

$$tCH(avg) = \left(\sum_{j=1}^{N} tCH_j\right) / (N \times tCK(avg))$$

$$where \qquad N = 200$$

tCL(avg) is defined as the average LOW pulse width, as calculated across any consecutive 200 LOW pulses.

$$tCL(avg) = \left(\sum_{j=1}^{N} tCL_j\right) / (N \times tCK(avg))$$

$$where \qquad N = 200$$

- tJIT(duty)

  tJIT(duty) is defined as the cumulative set of tCH jitter and tCL jitter. tCH jitter is the largest deviation of any single tCH from tCH(avg). tCL jitter is the largest deviation of any single tCL from tCL(avg).

  tJIT(duty) = Min/max of {tJIT(CH), tJIT(CL)}
  where,
  tJIT(CH) = {tCH_i- tCH(avg) where i=1 to 200}
  tJIT(CL) = {tCL_i- tCL(avg) where i=1 to 200}

- tJIT(per), tJIT(per,lck)

  tJIT(per) is defined as the largest deviation of any single tCK from tCK(avg).

  tJIT(per) = Min/max of {tCK_i- tCK(avg) where i=1 to 200}

  tJIT(per) defines the single period jitter when the DLL is already locked.
  tJIT(per,lck) uses the same definition for single period jitter, during the DLL locking period only.
  tJIT(per) and tJIT(per,lck) are not guaranteed through final production testing.

- tJIT(cc), tJIT(cc,lck)

  tJIT(cc) is defined as the difference in clock period between two consecutive clock cycles:

  tJIT(cc) = Max of $|tCK_{i+1} - tCK_i|$

  tJIT(cc) defines the cycle to cycle jitter when the DLL is already locked.
  tJIT(cc,lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.
  tJIT(cc) and tJIT(cc,lck) are not guaranteed through final production testing.

- tERR(2per), tERR (3per), tERR (4per), tERR (5per), tERR (6-10per) and tERR (11-50per)

  tERR is defined as the cumulative error across multiple consecutive cycles from tCK(avg).

$$tERR(nper) = \left(\sum_{j=1}^{i+n-1} tCK_j \right) - n \times tCK(avg)$$

$$where \left\{ \begin{array}{lll} n = 2 & for & tERR(2per) \\ n = 3 & for & tERR(3per) \\ n = 4 & for & tERR(4per) \\ n = 5 & for & tERR(5per) \\ 6 \le n \le 10 & for & tERR(6-10per) \\ 11 \le n \le 50 & for & tERR(11-50per) \end{array} \right.$$

Specific Note 36 These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times. (Min and max of SPEC values are to be used for calculations in the table below.)

Parameter	Symbol	min	max	Units
Absolute clock period	tCK(abs)	tCK(avg),min + tJIT(per),min	tCK(avg),max + tJIT(per),max	ps
Absolute clock HIGH pulse width	tCH(abs)	tCH(avg),min x tCK(avg),min + tJIT(duty),min	tCH(avg),max x tCK(avg),max + tJIT(duty),max	ps
Absolute clock LOW pulse width	tCL(abs)	tCL(avg),min x tCK(avg),min + tJIT(duty),min	tCL(avg),max x tCK(avg),max + tJIT(duty),max	ps

Example: For DDR2-667, tCH(abs),min = (0.48 x 3000 ps) - 125 ps = 1315 ps

Specific Note 37 tHP is the minimum of the absolute half period of the actual input clock. tHP is an input parameter but not an input specification parameter. It is used in conjunction with tQHS to derive the DRAM output timing tQH. The value to be used for tQH calculation is determined by the following equation;

tHP = Min (tCH(abs), tCL(abs)),
where,
tCH(abs) is the minimum of the actual instantaneous clock HIGH time;
tCL(abs) is the minimum of the actual instantaneous clock LOW time;

Specific Note 38 tQHS accounts for:

1) The pulse duration distortion of on-chip clock circuits, which represents how well the actual tHP at the input is transferred to the output; and
2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are independent of each other, due to data pin skew, output pattern effects, and p-channel to n-channel variation of the output drivers

Specific Note 39 tQH = tHP – tQHS, where:

tHP is the minimum of the absolute half period of the actual input clock; and
tQHS is the specification value under the max column.
{The less half-pulse width distortion present, the larger the tQH value is; and the larger the valid data eye will be.}
Examples:

5 AC & DC operating conditions (cont'd)

1) If the system provides tHP of 1315 ps into a DDR2-667 SDRAM, the DRAM provides tQH of 975 ps minimum.
2) If the system provides tHP of 1420 ps into a DDR2-667 SDRAM, the DRAM provides tQH of 1080 ps minimum.

Specific Note 40 When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(6-10per) of the input clock. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR2-667 SDRAM has tERR(6-10per),min = - 272 ps and tERR(6-10per),max = + 293 ps, then tDQSCK,min(derated) = tDQSCK,min - tERR(6-10per),max = - 400 ps - 293 ps = - 693 ps and tDQSCK,max(derated) = tDQSCK,max - tERR(6-10per),min = 400 ps + 272 ps = + 672 ps. Similarly, tLZ(DQ) for DDR2-667 derates to tLZ(DQ),min(derated) = - 900 ps - 293 ps = - 1193 ps and tLZ(DQ),max(derated) = 450 ps + 272 ps = + 722 ps. (Caution on the min/max usage!)

Specific Note 41 When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per) of the input clock. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR2-667 SDRAM has tJIT(per),min = - 72 ps and tJIT(per),max = + 93 ps, then tRPRE,min(derated) = tRPRE,min + tJIT(per),min = 0.9 x tCK(avg) - 72 ps = + 2178 ps and tRPRE,max(derated) = tRPRE,max + tJIT(per),max = 1.1 x tCK(avg) + 93 ps = + 2843 ps. (Caution on the min/max usage!)

Specific Note 42 When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(duty) of the input clock. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR2-667 SDRAM has tJIT(duty),min = - 72 ps and tJIT(duty),max = + 93 ps, then tRPST,min(derated) = tRPST,min + tJIT(duty),min = 0.4 x tCK(avg) - 72 ps = + 928 ps and tRPST,max(derated) = tRPST,max + tJIT(duty),max = 0.6 x tCK(avg) + 93 ps = + 1592 ps. (Caution on the min/max usage!)

Specific Note 43 When the device is operated with input clock jitter, this parameter needs to be derated by { - tJIT(duty),max - tERR(6-10per),max } and { - tJIT(duty),min - tERR(6-10per),min } of the actual input clock. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR2-667 SDRAM has tERR(6-10per),min = - 272 ps, tERR(6-10per),max = + 293 ps, tJIT(duty),min = - 106 ps and tJIT(duty),max = + 94 ps, then tAOF,min(derated) = tAOF,min + { - tJIT(duty),max - tERR(6-10per),max } = - 450 ps + { - 94 ps - 293 ps} = - 837 ps and tAOF,max(derated) = tAOF,max + { - tJIT(duty),min - tERR(6-10per),min } = 1050 ps + { 106 ps + 272 ps } = + 1428 ps. (Caution on the min/max usage!)

Specific Note 44 For tAOFD of DDR2-400/533, the 1/2 clock of tCK in the 2.5 x tCK assumes a tCH, input clock HIGH pulse width of 0.5 relative to tCK. tAOF,min and tAOF,max should each be derated by the same amount as the actual amount of tCH offset present at the DRAM input with respect to 0.5. For example, if an input clock has a worst case tCH of 0.45, the tAOF,min should be derated by subtracting 0.05 x tCK from it, whereas if an input clock has a worst case tCH of 0.55, the tAOF,max should be derated by adding 0.05 x tCK to it. Therefore, we have;

tAOF,min(derated) = tAC,min - [0.5 - Min(0.5, tCH,min)] x tCK
tAOF,max(derated) = tAC,max + 0.6 + [Max(0.5, tCH,max) - 0.5] x tCK
or
tAOF,min(derated) = Min(tAC,min, tAC,min - [0.5 - tCH,min] x tCK)
tAOF,max(derated) = 0.6 + Max(tAC,max, tAC,max + [tCH,max - 0.5] x tCK)
where tCH,min and tCH,max are the minimum and maximum of tCH actually measured at the DRAM input balls.

Specific Note 45 For tAOFD of DDR2-667/800, the 1/2 clock of nCK in the 2.5 x nCK assumes a tCH(avg), average input clock HIGH pulse width of 0.5 relative to tCK(avg). tAOF,min and tAOF,max should each be derated by the same amount as the actual amount of tCH(avg) offset present at the DRAM input with respect to 0.5. For example, if an input clock has a worst case tCH(avg) of 0.48, the tAOF,min should be derated by subtracting 0.02 x tCK(avg) from it, whereas if an input clock has a worst case tCH(avg) of 0.52, the tAOF,max should be derated by adding 0.02 x tCK(avg) to it. Therefore, we have;

tAOF,min(derated) = tAC,min - [0.5 - Min(0.5, tCH(avg),min)] x tCK(avg)
tAOF,max(derated) = tAC,max + 0.6 + [Max(0.5, tCH(avg),max) - 0.5] x tCK(avg)
or

tAOF,min(derated) = Min(tAC,min, tAC,min - [0.5 - tCH(avg),min] x tCK(avg))
tAOF,max(derated) = 0.6 + Max(tAC,max, tAC,max + [tCH(avg),max - 0.5] x tCK(avg))
where tCH(avg),min and tCH(avg),max are the minimum and maximum of tCH(avg) actually measured at the DRAM input balls.

Note that these deratings are in addition to the tAOF derating per input clock jitter, i.e. tJIT(duty) and tERR(6-10per). However tAC values used in the equations shown above are from the timing parameter table and are not derated. Thus the final derated values for tAOF are;

tAOF,min(derated_final) = tAOF,min(derated) + { - tJIT(duty),max - tERR(6-10per),max }
tAOF,max(derated_final) = tAOF,max(derated) + { - tJIT(duty),min - tERR(6-10per),min }

Annex A (informative) Differences between JESD79-2B and JESD79-2C

This table briefly describes most of the changes made to this standard, JESD79-2C, compared to its predecessor, JESD79-2B (January 2005). It should be used with both Version B and Version C at hand. Some editorial changes are not included.

Page	Description of Change
2	Per JCB-06-018 In Figure 2 — DDR2 SDRAM x8 Ballout Using MO-207 Modified note 5.
3	Per JCB-06-018 In Figure 3 — DDR2 SDRAM x16 Ballout Using MO-207 Modified the note.
4	Per JCB-06-018 In Figure 4 — Stacked/dual-die DDR2 SDRAM x4 Ballout Using MO-242 Modified the note.
5	Per JCB-06-018 In Figure 5 — Stacked/dual-die DDR2 SDRAM x8 Ballout Using MO-242 Modified the note.
6	Per JCB-06-018 Added Figure 6 — Quad-stacked/quad-die DDR2 SDRAM x4 Ballout Using MO-242
7	Per JCB-06-018 Added Figure 7 — Quad-stacked/quad-die DDR2 SDRAM x8 Ballout Using MO-242
8	Per JCB-06-018 Added Figure 8 — Quad-stacked/quad-die DDR2 SDRAM x16 Ballout Using MO-242
9	Per JCB-06-018 Added new Section 1.2 Quad-stacked/quad-die DDR2 SDRAM Internal Rank Associations (subsequent sections renumbered accordingly) Added Figure 9 — Quad-stacked/quad-die DDR2 SDRAM x4 Rank Association Added Figure 10 — Quad-stacked/quad-die DDR2 SDRAM x8 Rank Association Added Figure 11 — Quad-stacked/quad-die DDR2 SDRAM x16 Rank Association
12	Per JCB-05-021 In Figure 12 — DDR2 SDRAM Simplified State Diagram, • Added a Write command between Reading and Writing. • Added a WRA command between Reading and Writing With Autoprecharge. • modified the note. .
13	Per JCB-06-018 In Section 2.3.1, Power Up and Initialization, Rewrote Step a) of the Power-Up and Initialization Sequence.
15	Per JCB-05-018 In Figure 14 — DDR2 SDRAM Mode Register Set (MRS), Added note 3.
15	Per JCB-06-018 In Section 2.4.2, changed the term “extended mode register set (EMRS(#))” to “extended mode registers (EMR(#))”
17	Per JCB-06-018 In Figure 15 — EMR(1) Programming, Reorganized the figure, collecting the notes at the bottom of the page.

Annex A (informative) Differences between JESD79-2B and JESD79-2C (cont'd)

This table briefly describes most of the changes made to this standard, JESD79-2C, compared to its predecessor, JESD79-2B (January 2005). It should be used with both Version B and Version C at hand. Some editorial changes are not included.

Page	Description of Change
19	Per JCB-05-075 In Figure 16 — EMR(2) Programming, • Added A3 - DCC Enable. • Added note 4.
20	Per JCB-06-018 Added Section 2.4.2.6 EMR(3)
23	Per JCB-06-018 Added Section 2.4.5 ODT Related Timings
24	Per JCB-06-018 In Section 2.4.5.1 — MRS Command to ODT Update Delay, • Added Figure 22 — ODT Update Delay Timing - tMOD. • Added Figure 22 — ODT Update Delay Timing - tMOD. as Measured from Outside.
47	Per JCB-06-018 In Section 2.11— Power-Down, Expanded the last sentence in the third paragraph.
53	Per JCB-05-069 Added Section 2.14 SCC (Spread Spectrum Clocking)
53	Per JCB-06-018 In Table 12 — Command Truth Table, Referenced Note 9 for BAx and Axx in the column headings
53	Per JCB-06-018 In Table 12 — Command Truth Table, Referenced Note 8 for Self Refresh Entry
54	Per JCB-06-018 In Table 12 — Command Truth Table, Referenced Note 8 for Self Refresh Exit
54	Per JCB-06-018 In Table 12 — Command Truth Table , Added Note 9
55	Per JCB-06-018 In Table 13 — Clock Enable (CKE) Truth Table for Synchronous Transitions, Referenced Note 16 for Self Refresh
56	Per JCB-05-007 In Table 15 — Absolute Maximum DC Ratings, • Added Note 3. • Referenced Note 3 for all parameters except V_{IN}, V_{OUT}
57	Per JCB-05-117 Added reference to JEP-xx, DDR2 SDRAM Operating Temperature Application Note
60	Per JCB-06-018 In Table 25 — AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins, Added a column for DDR2-800..

Annex A (informative) Differences between JESD79-2B and JESD79-2C (cont'd)

This table briefly describes most of the changes made to this standard, JESD79-2C, compared to its predecessor, JESD79-2B (January 2005). It should be used with both Version B and Version C at hand. Some editorial changes are not included.

Page	Description of Change
60	Per JCB-05-002 In Table 25 — AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins, Changed the values in the first two rows from 0.9 V to 0.5 V..
62	Per JCB-05-006 In Table 29 — OCD Default Characteristics, Expanded Note 1.
62	Per JCB-06-018 In Table 29— OCD Default Characteristics, • Notes 1 and 2 from Figure 68, Output Slew Rate, were moved into Table 29 as Notes 7 & 8. • Added Note 9
62	Per JCB-05-006 Figure 68, Output Slew Rate, was removed, since the information is actually part of Table 29.
69	Per JCB-05-009 In Table 36 — IDD Specifications and Test Conditions, In IDD7, added "^{t}FAW = ^{t}FAW(IDD)".
70	Per JCB-05-009 In Table 37 — IDD Testing Parameters, • Added columns for DDR2-800 • Added a column, under DDR2-667, for Bin 5-5-5 • Under DDR2-533, removed the column for Bin 5-5-5 • Changed ^{t}RRD(IDD)-x4/x8 to ^{t}RRD(IDD)-1KB • Changed ^{t}RRD(IDD)-x16 to ^{t}RRD(IDD)-2KB • Added ^{t}FAW(IDD)-1KB • Added ^{t}FAW(IDD)-2KB • Added ^{t}RFC(IDD)-4Gb

Annex A (informative) Differences between JESD79-2B and JESD79-2C (cont'd)

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Page	Description of Change
71	Per JCB-05-009 In unnumbered heading, **Detailed IDD7** • In **IDD7: Operating Current: All Bank Interleave Read operation,** added tFAW(IDD) to the text • Changed **Timing Patterns for 4 bank devices x4/ x8/ x16** to **Timing Patterns for 4 bank devices with 1 KB or 2 KB page size** • Removed DDR2-533 5-4-4 • Added DDR2-533 3-3-3 • Added DDR2-667 5-5-5 • Added DDR2-667 5-5-5 • Added DDR2-800 6-6-6 • Added DDR2-800 5-5-5 • Added DDR2-800 4-4-4 • Changed **Timing Patterns for 8 bank devices x4/x8** to **Timing Patterns for 8 bank devices with 1 KB page size** • Added DDR2-667 all bins • Added DDR2-800 all bins • Changed **Timing Patterns for 8 bank devices x16** to **Timing Patterns for 8bank devices with 2 KB page size** • Added DDR2-667 all bins • Added DDR2-800 all bins
72	Per JCB-06-018 In Table 40 — DDR2 SDRAM Standard Speed Bins and tCK, tRCD, tRP, tRAS and tRC for Corresponding Bin, Added Notes 2-4.
73, 74	Per JCB-06-018 In Table 41 — Timing Parameters by Speed Grade (DDR2-400 and DDR2-533), • Added WL — Write command to DQS associated clock edge, • Added tMOD — MRS command to ODT update delay, • Added reference to Note 16 for tAOND, • for tAOFD, added reference to Notes 17 and 44 , • Added reference to Note 44 for tAOF.

Annex A (informative) Differences between JESD79-2B and JESD79-2C (cont’d)

This table briefly describes most of the changes made to this standard, JESD79-2C, compared to its predecessor, JESD79-2B (January 2005). It should be used with both Version B and Version C at hand. Some editorial changes are not included.

Page	Description of Change
75, 76	Per JCB-06-018, In Table 42 — Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), • Added WL — Write command to DQS associated clock edge • Added tMOD — MRS command to ODT update delay • For parameter tDQSQ — for DDR2-677, moved the value, 240, from the min column to the max column • For parameter tDQSQ — for DDR2-677, moved the value, 240, from the min column to the max column • For parameter tQSH — for DDR2-677, moved the value, 340, from the min column to the max column • Changed the unit “tCK” to “nCK” on the following parameters: tMRD, tCCD, tDAL, tXSRD, tXP, tXARD, tXARDS, tCKE, tAOND, tAOFD, tANPD, tAXPD • Added reference note 34 to column heading “Units” • Added reference notes to the following parameters parameter notes tCK(avg) 35, 36 (removed reference to note 15) tCH(avg) 35, 36 tCL(avg) 35, 36 tDQSS 30 tDSS 30 tDSH 30 tIS(base) 29 tIH(base) 29 tDS(base) 8, 31 tDH(base) 8, 31 tAC 40 tDQSCK 40 tHZ 40 tLZ(DQS) 40 tLZ(DQ) 40 tHP 37 (removed reference to notes 11 and 12) tQHS 38 (removed reference to note 12) tQH 39 tRPRE 41 tRPST 42 tRRD 32 tFAW 32 tWR 32 tDAL 33 (removed reference to note 14) tWTR 32 tRTP 32 tXSNR 32 tAOND 16 tAON 40 tAOFD 17, 45 tAOF 43, 45 tMOD 32 tOIT 32 •
75, 76	Per JCB-05-004, In Table 42 — Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), • For parameter tDQSQ — Added the DDR2-800 max value: 200 • For parameter tQSH — Changed the DDR2-800 max value from 400 to 300

Annex A (informative) Differences between JESD79-2B and JESD79-2C (cont'd)

This table briefly describes most of the changes made to this standard, JESD79-2C, compared to its predecessor, JESD79-2B (January 2005). It should be used with both Version B and Version C at hand. Some editorial changes are not included.

Page	Description of Change
75, 76	Per JCB-05-014, In Table 42 — Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), • Renamed parameter tCH to tCH(avg) • Renamed parameter tCL to tCL(avg)
75, 76	Per JCB-05-005, In Table 42 — Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), • For parameter tDS(base) — Added the DDR2-800 min value: 50 • For parameter tDH(base) — Added the DDR2-800 min value: 120
75, 76	Per JCB-05-015, In Table 42 — Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), • Renamed parameter tCK to tCK(avg) • Added the DDR2-800 max value: 8000
75, 76	Per JCB-05-070, In Table 42 — Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), • For parameter tIS(base) — Added the DDR2-800 min value: 175 • For parameter tIH(base) — Added the DDR2-800 min value: 250
77	Per JCB-06-018 General Notes 1 and 2 have been transposed.
79	Per JCB-05-003 In Specific Note 8, Replaced Table 43 DQS,$\overline{\text{DQS}}$ Differential Slew Rate, with two tables, 43 and 44, one for DDR2-400/533 and one for DDR2-667/800. Following tables are renumbered accordingly.
80	Per JCB-05-008 In Specific Note 8, Populated Table 45 DQS Single-ended Slew Rate.
84	Per JCB-05-064 Specific Notes 16, 17, and 18 expanded.
97-102	Per JCB-05-064 Specific Notes 29-45 added.

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